ALGOS
ALGorithms for Optimization and Simulation

An Efficient Low Power Multiple-value Look-up Table Targeting Quaternary FPGAs

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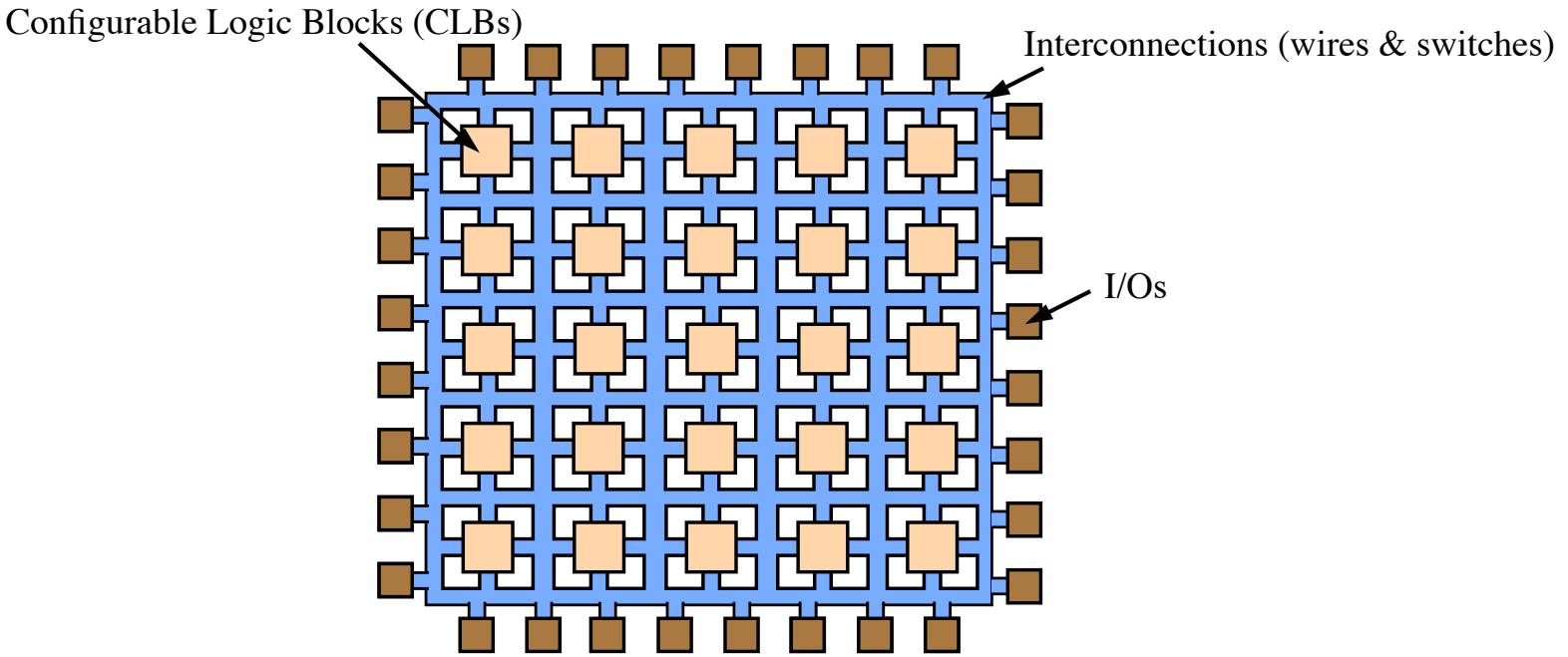
Talk Outline

- Motivation
- Binary vs Quaternary Lookup Tables
- New Quaternary-to-Binary Decoder
- Results
- Conclusions and Future Work

Motivation – Field Programmable Gate Arrays

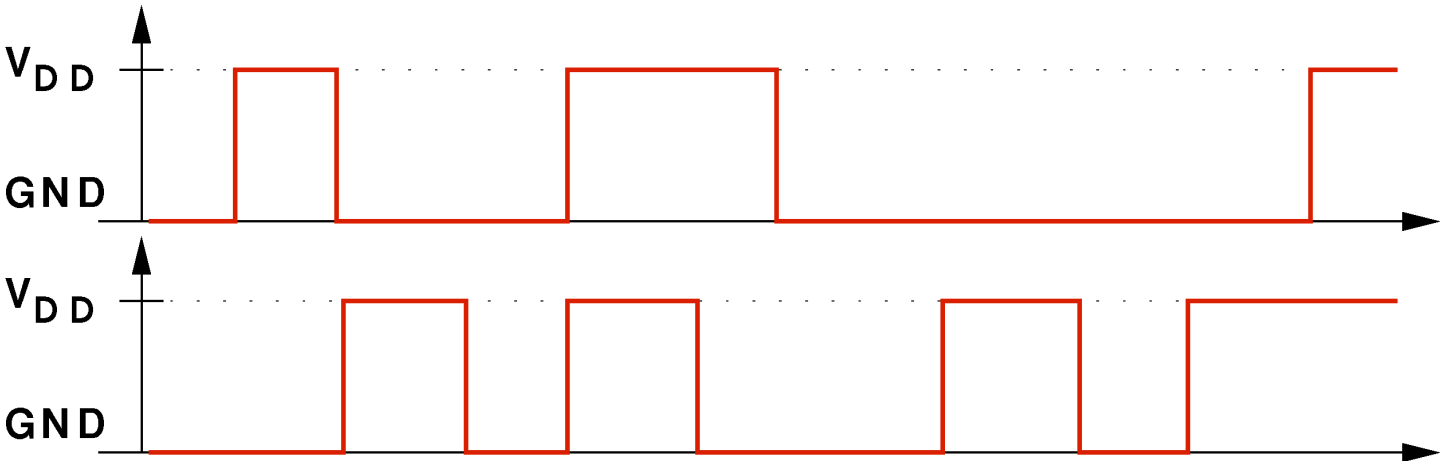
- Interconnections play crucial role in FPGAs
  - They severely impact on power and area *(Singh, Sadowska; 2002)*
  - Up to 90% chip area are interconnections *(Cunha, Boudinov, Carro; 2006)*



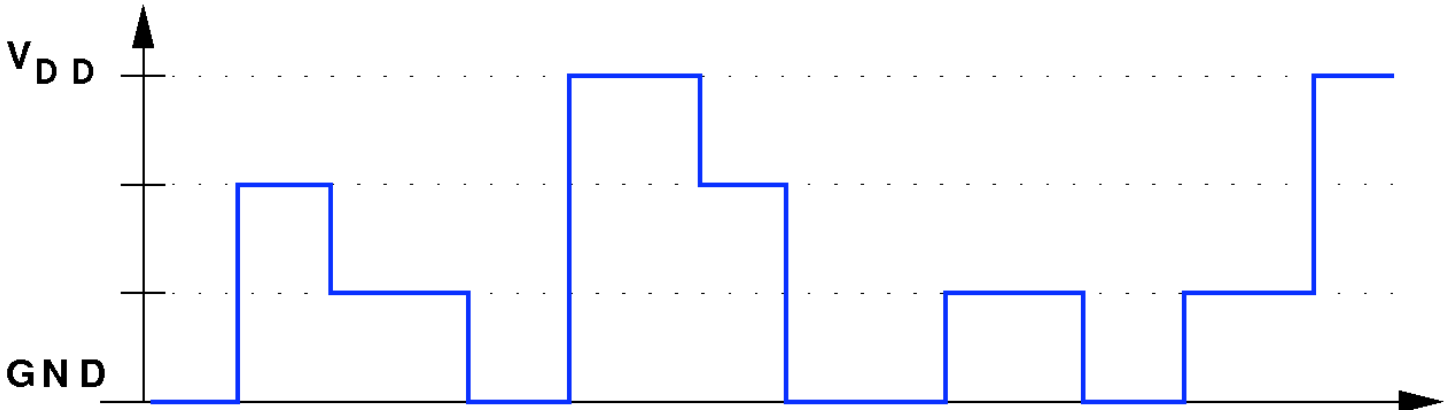
Major limiting factor for developing efficient FPGA designs!

Introduction – Multiple-Valued Logic (MVL)

- Multiple-valued Logic uses more than two logic values
  - **Binary Logic**



  - **MVL (quaternary)**



Introduction – Multiple-Valued Logic (MVL)

- Compacting the information with MVL
  - Reduced number of wires to represent the same information
  - Reduced number of logic blocks to operate over data
  - Reduced wire lengths to connect logic blocks
- As a consequence
  - Smaller ***Area*** due to interconnection reduction
  - ***Power consumption*** and ***delay*** *reduction*
    - *reduced load capacitance*
- Physical implementation of the interconnects are the same in the binary logic and the MVL
  - We are left with the **implementation of the logic blocks**

Multiple-Valued Logic – Early Work

- Multiple-valued logic is not new
  - 1993 FPGA (Zilic, Vranesic)
  - 1995 Multiplier (Hanyu, Kameyama)
  - 1998 Adder (Gonzalez, Mazumder)
  - 1998 Lookup tables (Sheikholeslami, Yoshimura, Gulak)

- Logic is implemented using current-mode devices
  - Excessive power consumption
  - Complex Design

A Voltage-Mode MVL Device

- A voltage-mode MVL device has been recently proposed
  - Data is represented by **quaternary** values
  - Deals with the power dissipation problem
  - Based on standard CMOS circuits
    - Requires transistors with different V_{th}s

(Cunha, Boudinov, Carro; 2006)

- Multiple V_{th}s demand process modifications
  - More process steps
  - Increased production costs

Contributions of This Work

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Implementation of a new MVL LUT

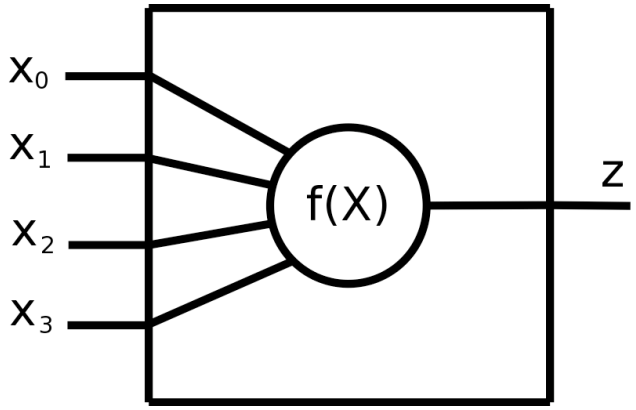
- Voltage-mode device
- No additional process steps are required
- Competitive with the binary LUTs

Binary & Quaternary Lookup Tables

BLUT

$$f : B^m \rightarrow B$$

$$X = (x_0, \cdots, x_i, \cdots, x_{m-1})$$



$$B = \{0, 1\}, m = 4$$

QLUT

$$g : Q^n \rightarrow Q$$

$$Y = (y_0, \cdots, y_i, \cdots, y_{n-1})$$

$$Q = \{0, 1, 2, 3\}, n = 2$$

$$|Q| = 2 \times |B|$$

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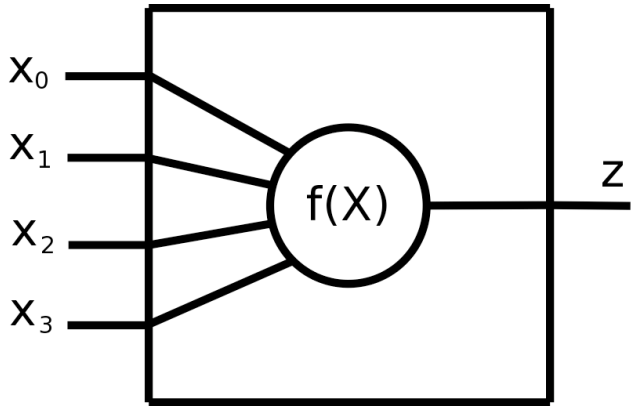

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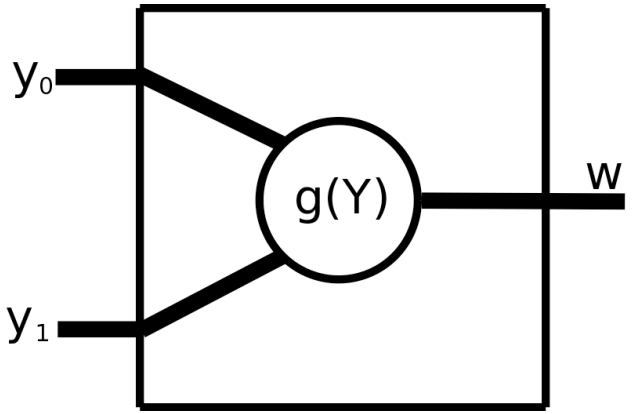

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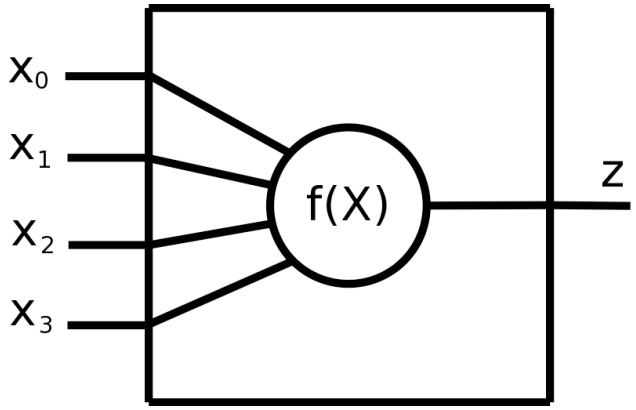

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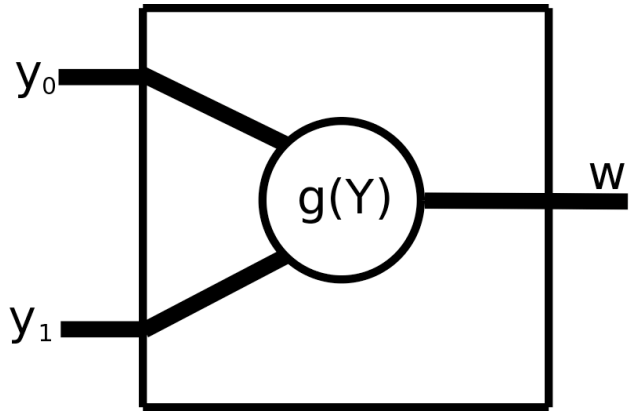

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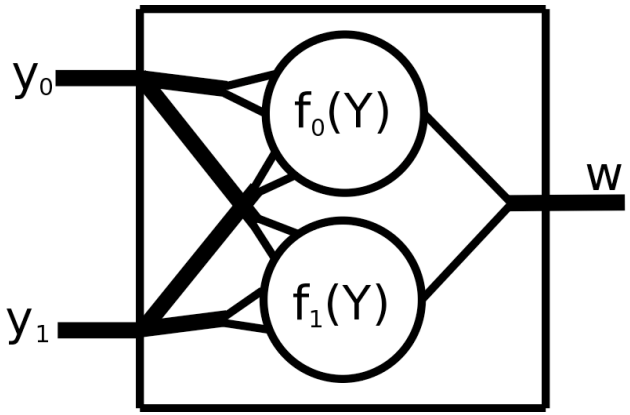
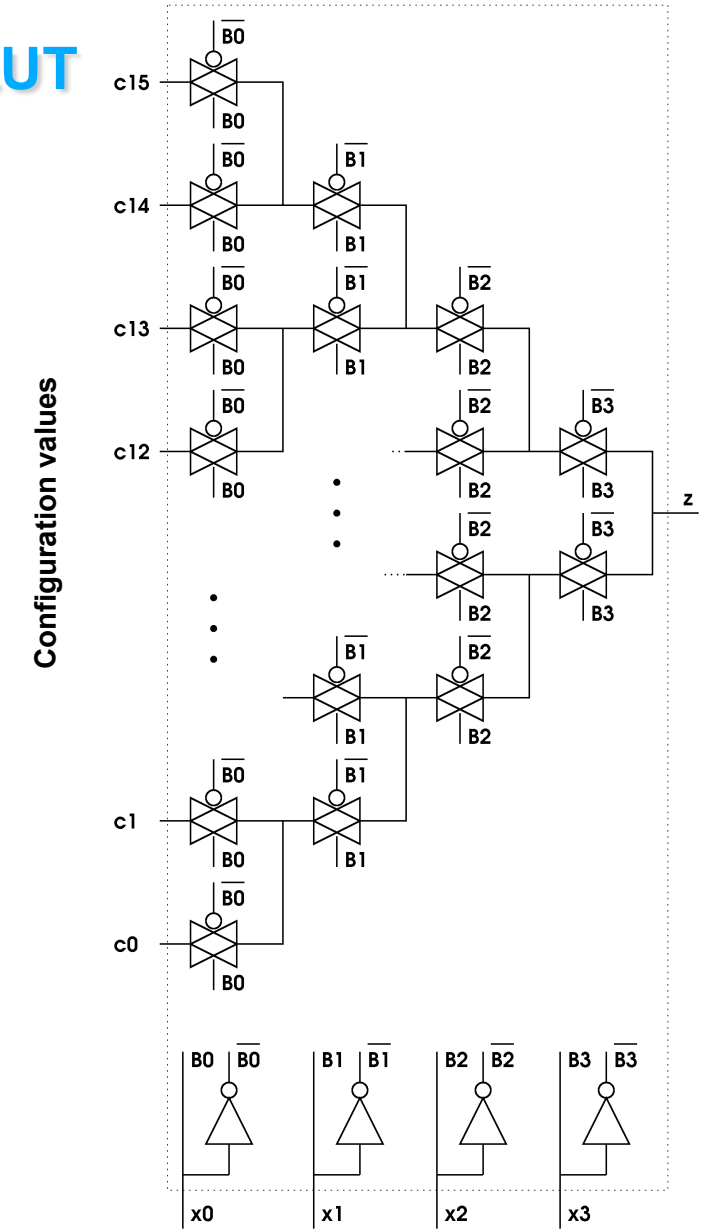


$$|Q| = 2 \times |B|$$

Binary & Quaternary LUTs Implementation

BLUT



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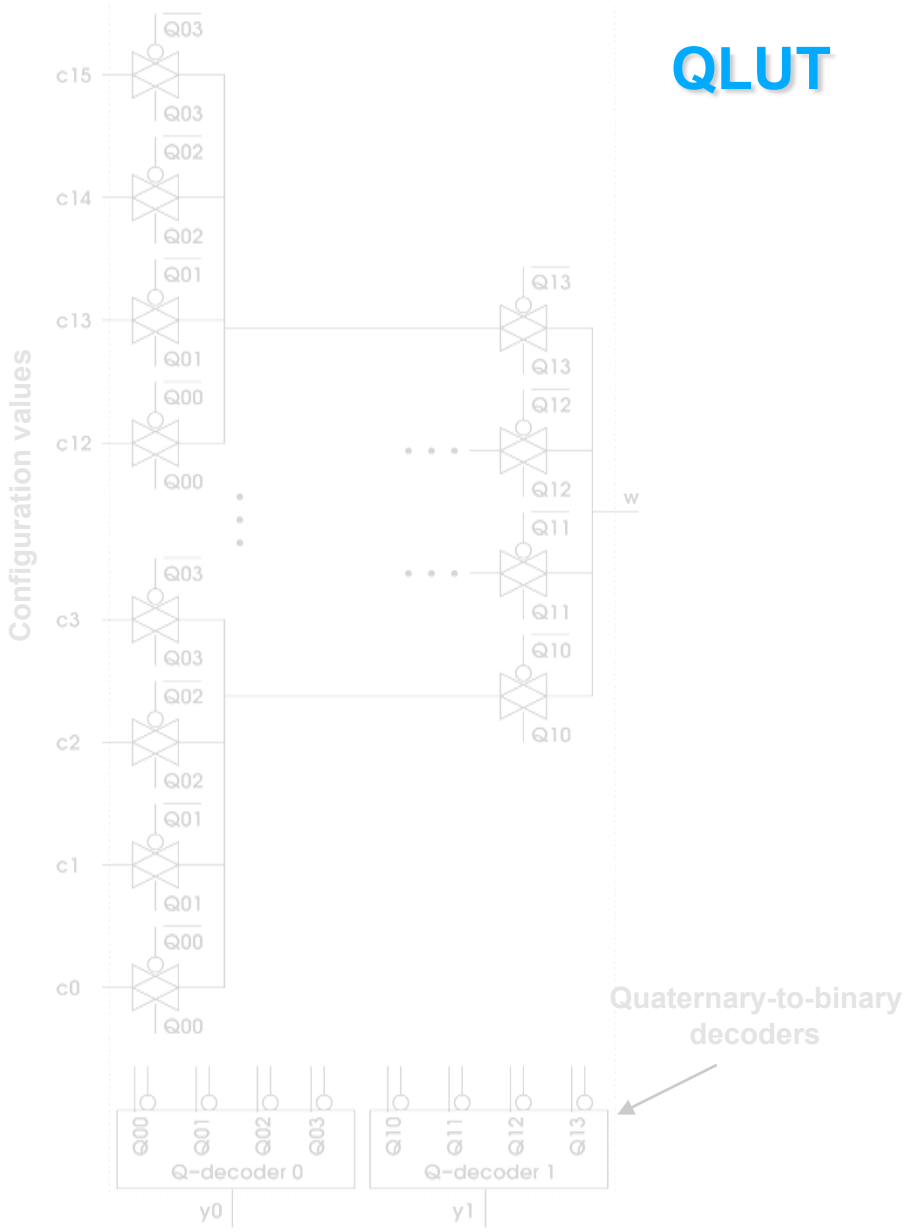

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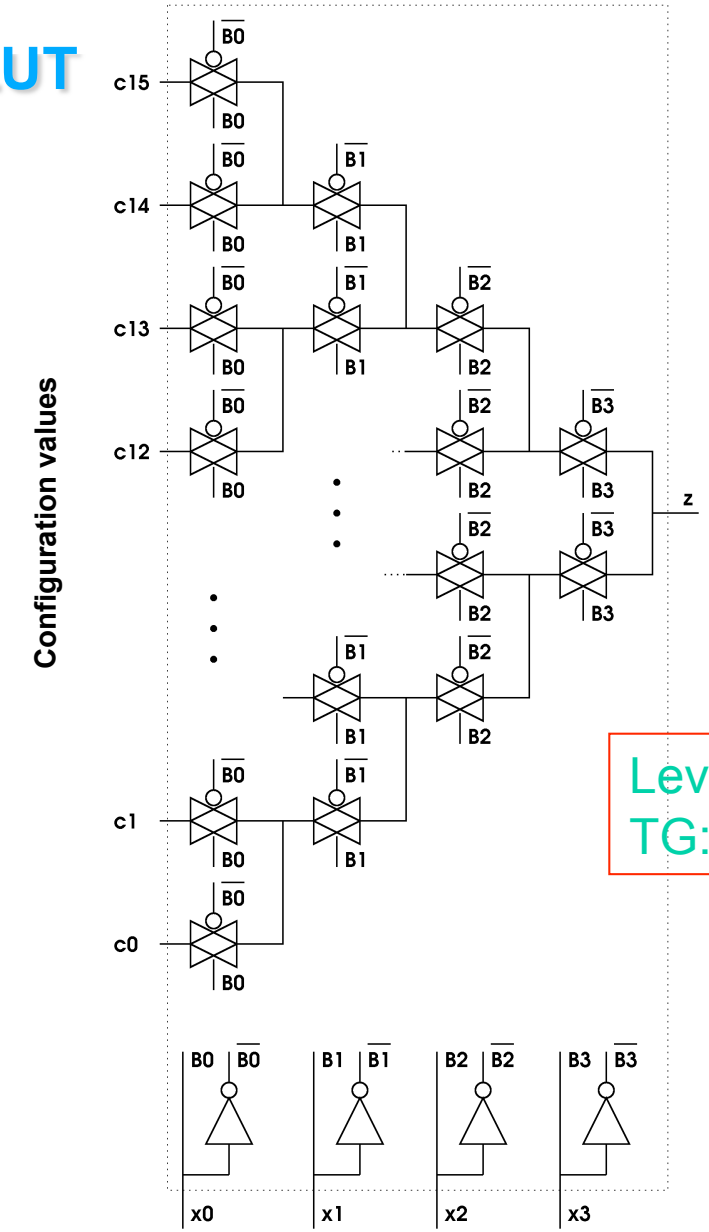
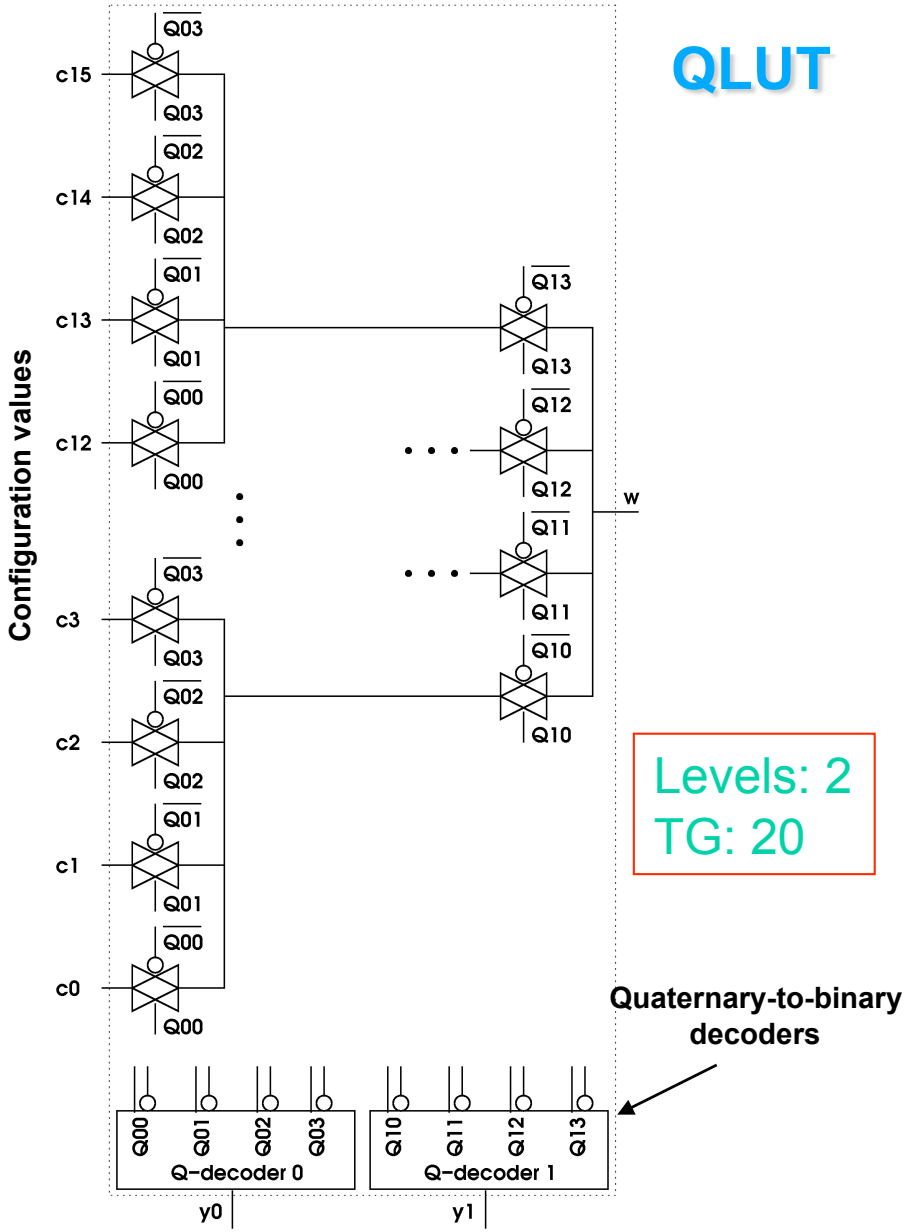


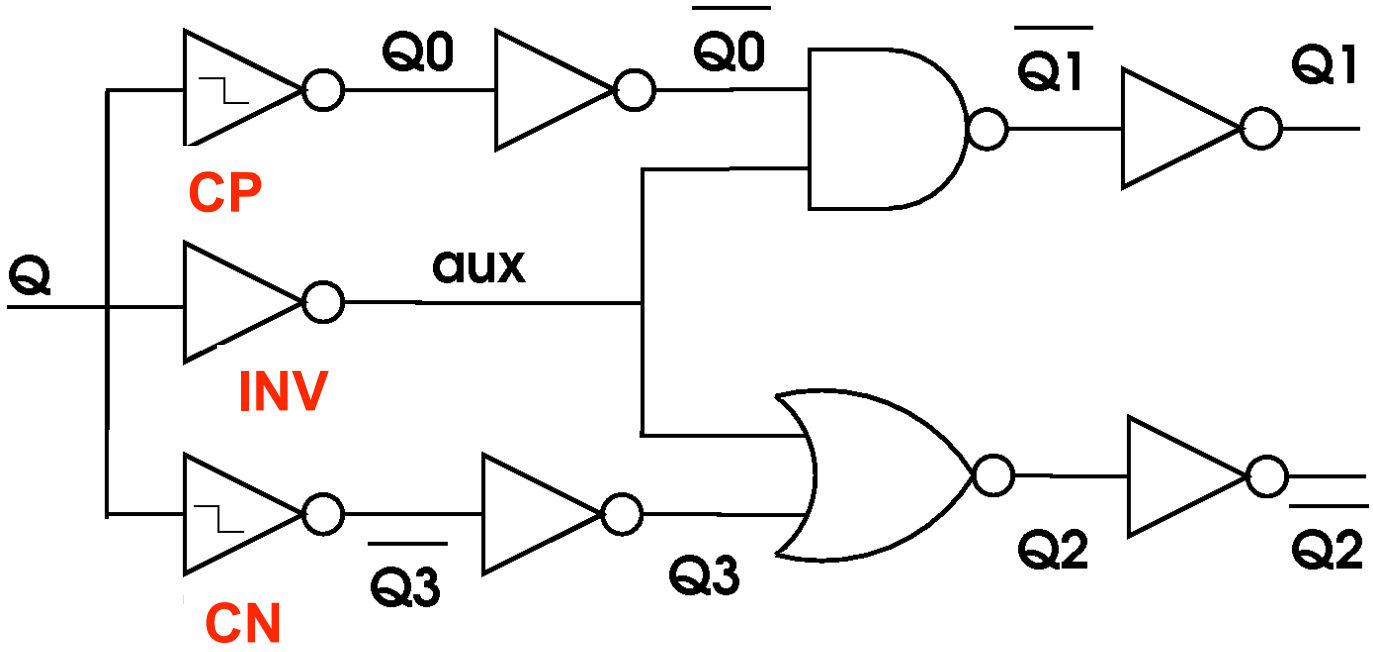
Levels: 4
TG: 30



Levels: 2
TG: 20

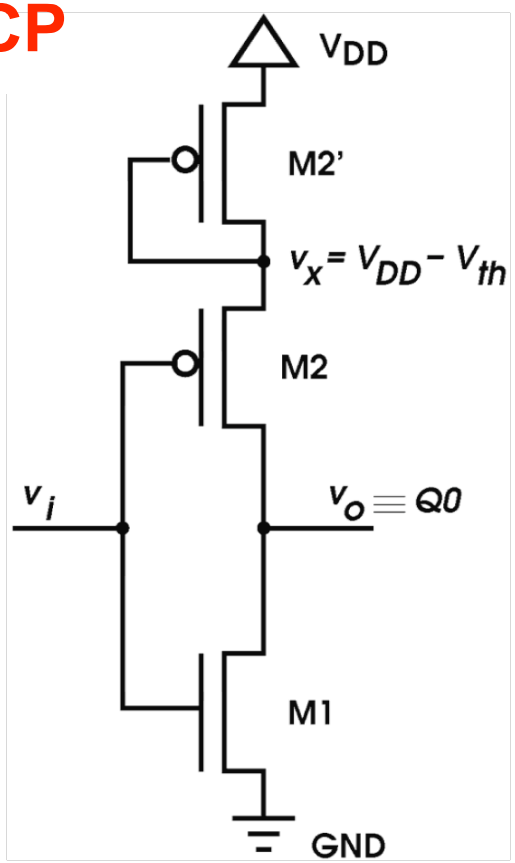
Quaternary-to-binary Decoder

Q	Q_0	Q_1	Q_2	Q_3
0_4	1_2	0	0	0
1_4	0	1_2	0	0
2_4	0	0	1_2	0
3_4	0	0	0	1_2



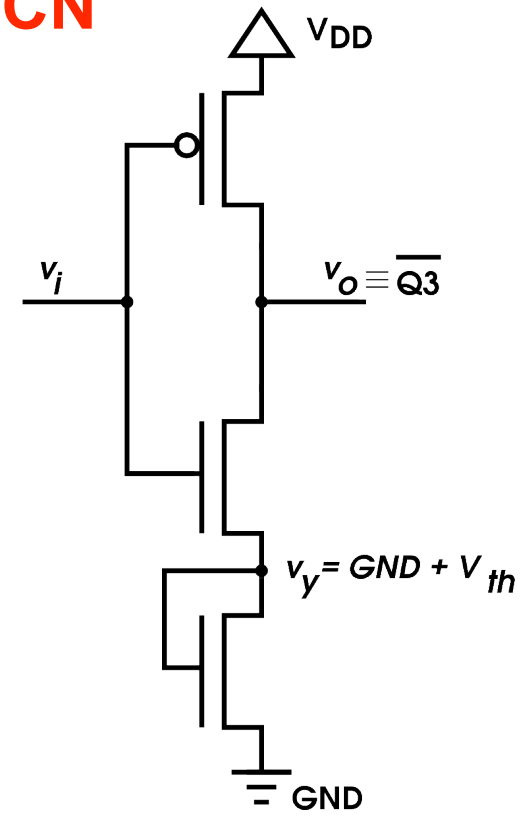
Quaternary Comparators

CP



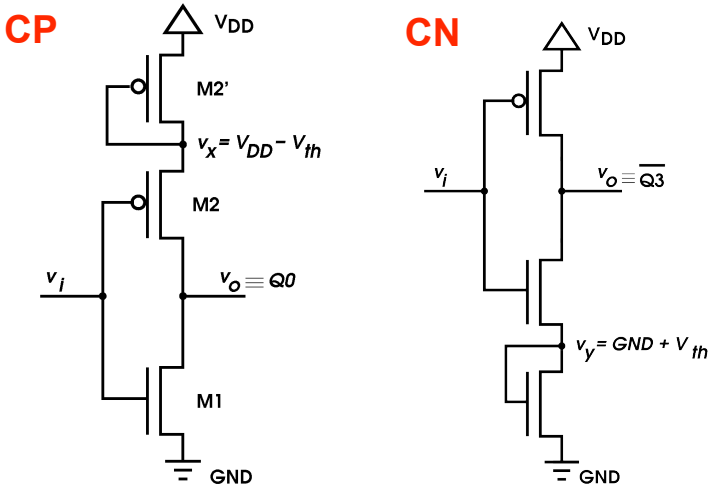
Output is GND when Vi >= ‘1’

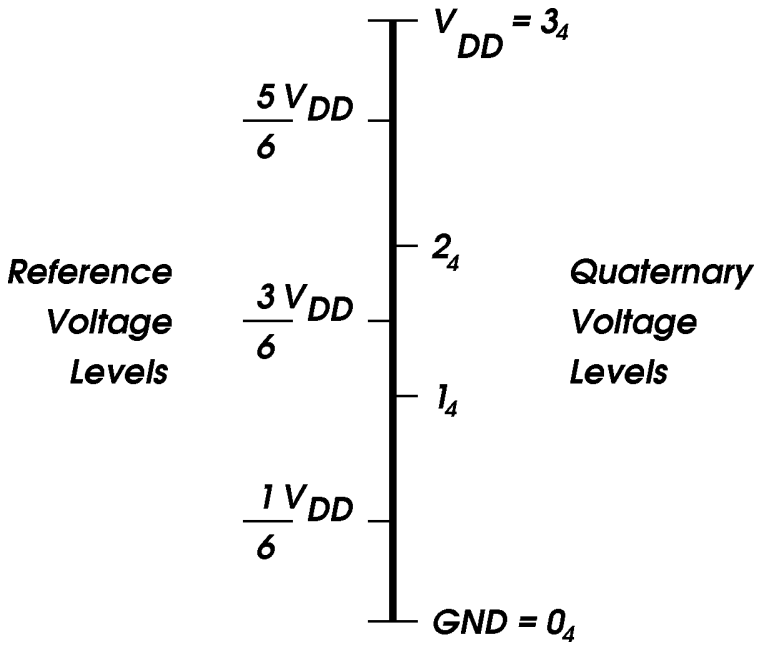
CN

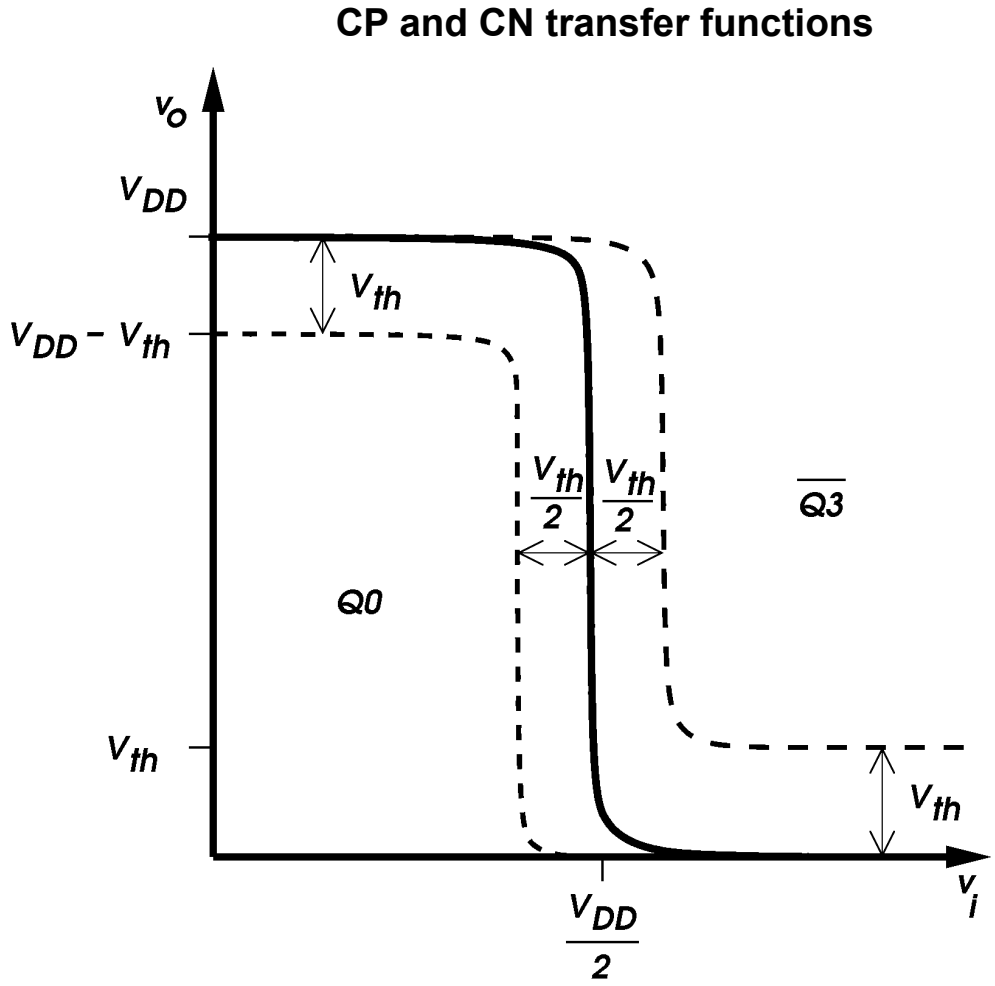


Output is GND when Vi > ‘2’

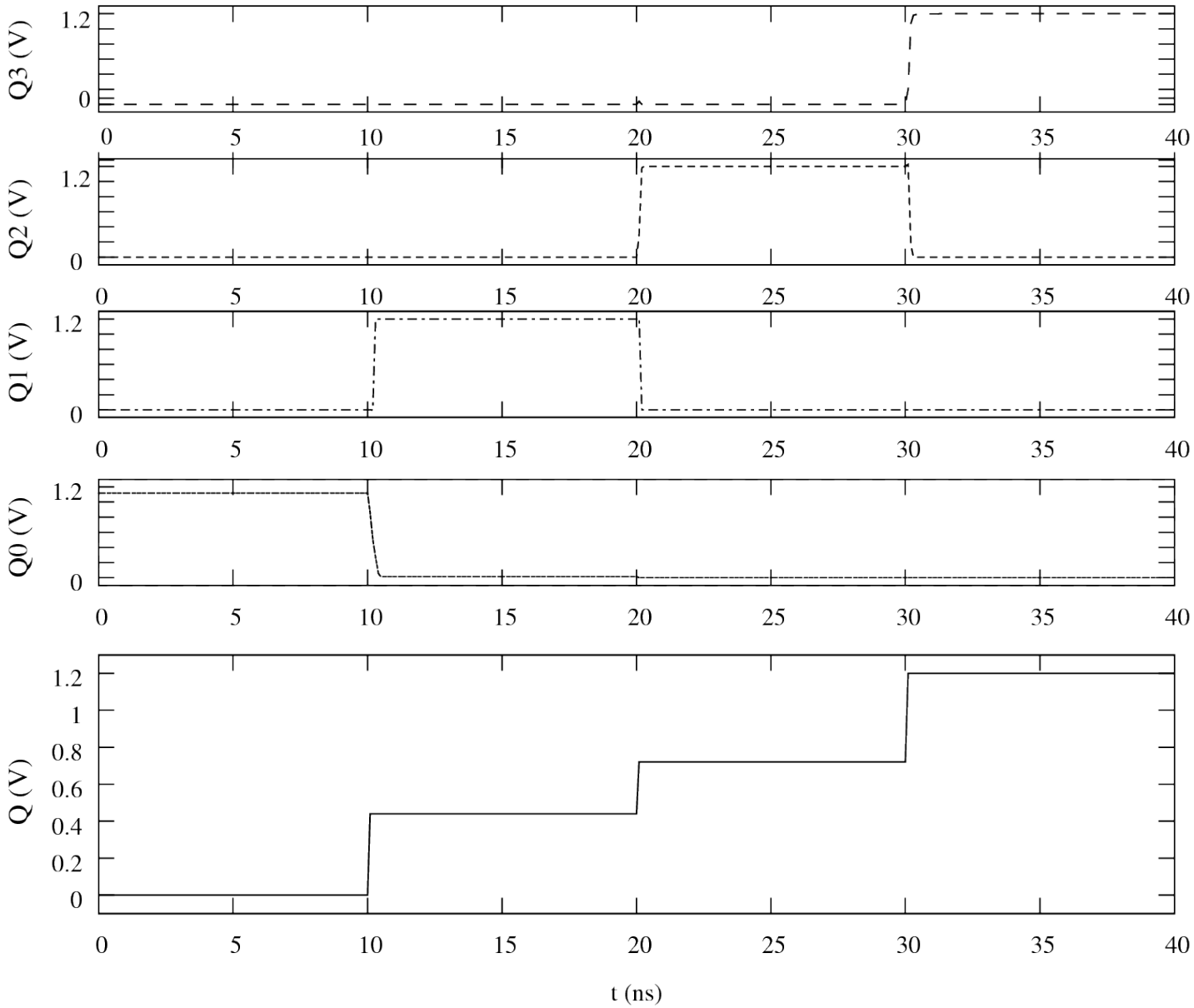
Quaternary Logic Levels



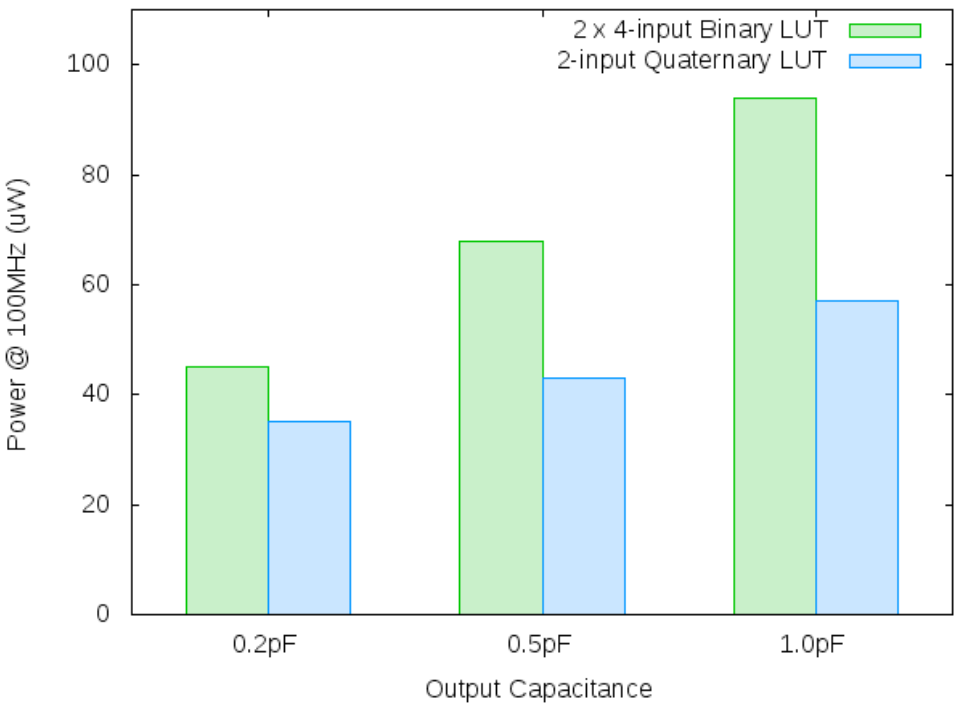


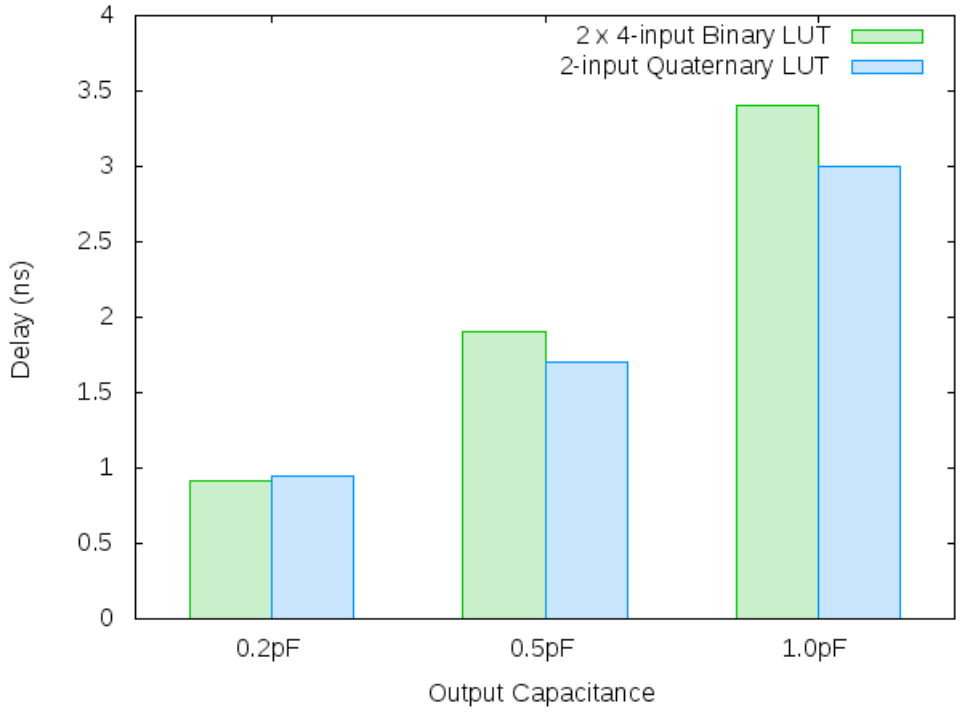


Q-decoder Signals Waveforms



Experimental Results

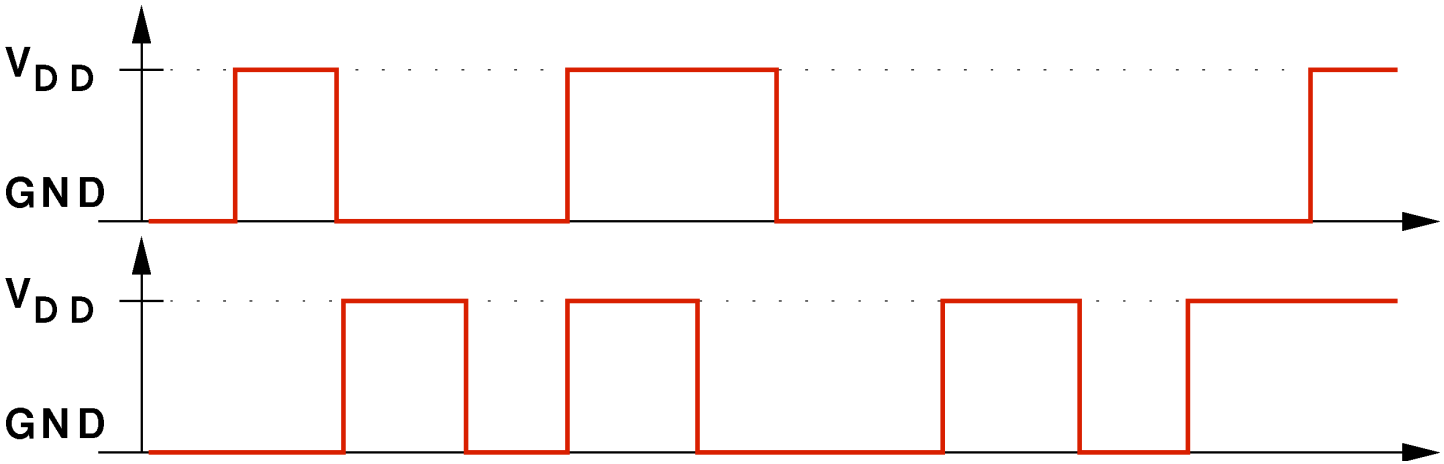




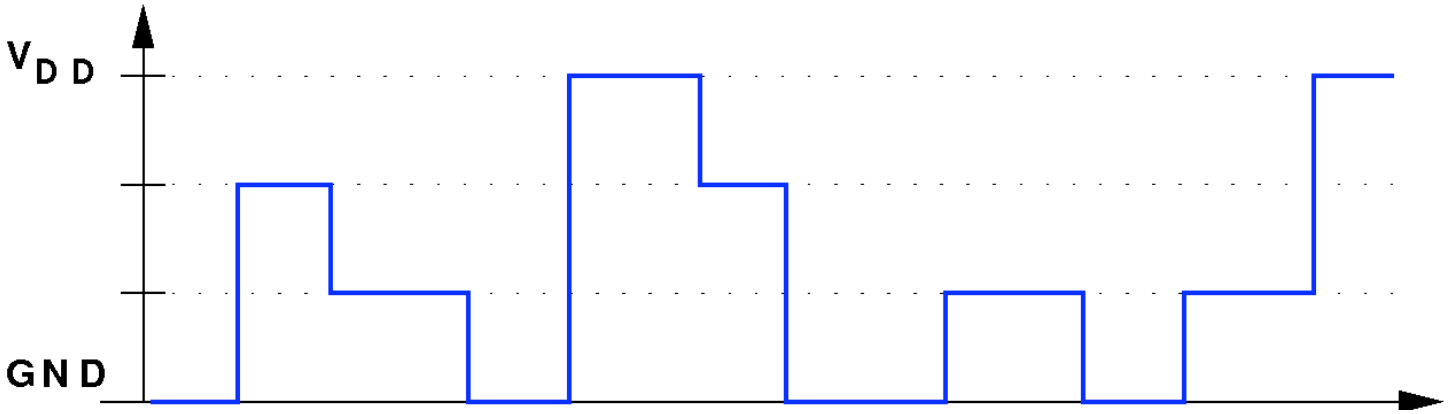
- UMC 130nm technology (Cadence Virtuoso)
- Vdd = 1.2V, Vth~400mV
- Quaternary LUTs present power gains ranging from 22% to 39%
- Larger gains for larger loads

Voltage Swing

- On average, the voltage swing is $V_{DD}/2$
  - **Binary Logic**

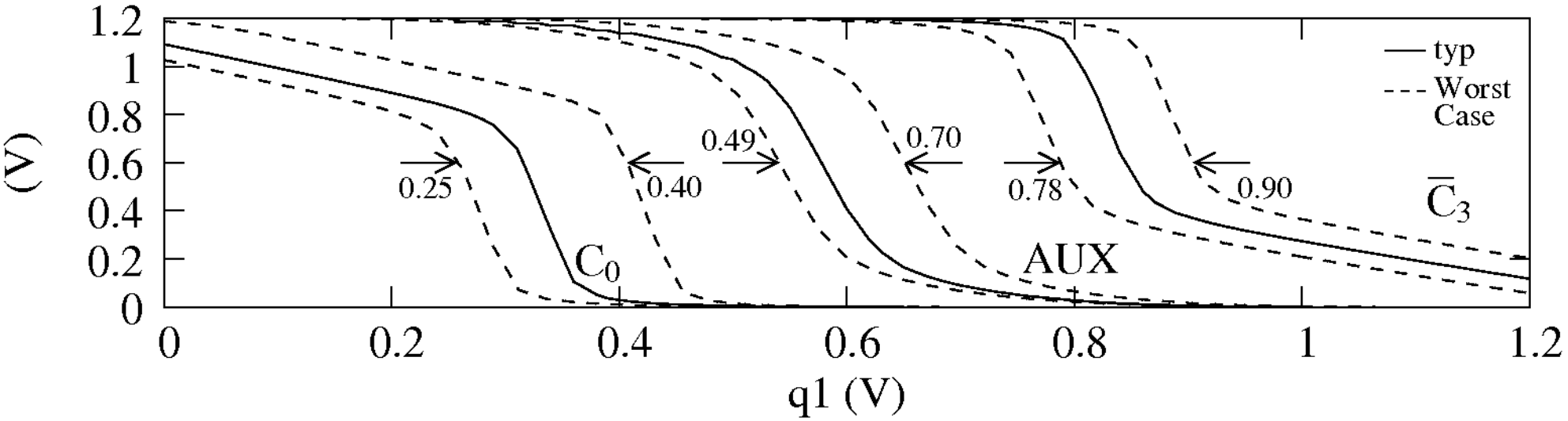


  - **MVL (quaternary)**



Process Variability and Noise Margin

- Process variability and reduced noise margin are important challenges on the development of MVL circuits
- We performed a Monte Carlo simulation
  - Considering random process and mismatch variations
  - Observed decision levels voltage variations were < 90mV
  - A 100mV gap between logic levels is still availble



Conclusions

- We propose a new design for a quaternary lookup table
  - This design allows for voltage discretization outside the reach of binary logic
- Results show that the proposed technique is competitive with binary FPGAs
- Fabricated chip using 130nm technology is under test
- We are developing a complete FPGA structure
  - Logic blocks, switch matrix, etc


Thank You !
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