Quaternary Logic Look-Up Table: an Alternative Circuit

INESC-ID Technical Report RT 2/2014

QCell - Configurable Logic Block Cell for Quaternary FPGAs

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INESC-ID / IST

February 2014

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Chapter 1

Introduction

Due to the technological advances on the field of integrated circuits, designers now face new challenges. Large area is no longer a constraint to achieve new and better circuits being the priority now to reach a good compromise between time delays, power consumption and area. Regarding FPGAs, these three factors are mainly limited by interconnections which occupy as much as 90% of the chip area.

A solution proposed in the past is the usage of multiple-value logic instead of binary logic [1]-[2]. The latest is the most used in digital circuits since it is very easy to implement and it represents the foundation of every computational calculus. On the other hand, multiple-value logic promises a large decrease on the number of interconnections since a single wire carrying a signal with N logic levels can replace $log_2 N$ wires carrying binary signals. Remembering what was said before, interconnections are the main limitation for the FPGAs performance and so the multi-value logic implementation has been very appealing to designers. The reason for not being already commonly used in circuits it is because with the implementations presented before, there is an excessive power consumption and some implementation complexities[3],[4], [5] and [6]. These drawbacks have prevented these systems from being until now a viable alternative to standard CMOS designs.

On [7], Diogo Brito proposed a quaternary look-up table that proved to be a viable alternative to the binary look-up tables achieving the desired results- less interconnections, less area and lower power consumption. Following this line of work, it's now proposed additional circuits that allow to compute various pre-set functions on the quaternary look-up table: a voltage generator to generate the four different voltage references needed for the representation of quaternary values and a interconnection matrix that connects this four levels of voltages to the quaternary look-up table's inputs.

Objectives

The objective of this work is to make a brief introduction to the multi-value logic and the quaternary FPGA state-of-the-art. Furthermore we also propose the research and implementation of additional structures needed to achieve a fully functional quaternary FPGA.

From [7] we have a functional QLUT which given two quaternary inputs- Q_A and Q_B- computes

a quaternary output. From here, the first stage is to investigate the more proficient way to connect a voltage generator to the quaternary look-up table already designed without compromising the results previously obtained on [7]. The second stage is to research a possible implementation for a voltage generator and then test it in order to ascertain its drawbacks and possible improvements. This circuit will enable the FPGA to generate and store the four voltage levels needed to compute the various pre-set functions.

Chapter 2

State-of-the-art

2.1 Quaternary Look-Up Table

On [7] it's presented the implementation of a quaternary look-up table depicted on Figure 2.1.

This design was implemented using a standard CMOS technology, a single supply voltage and a clock boosting technique to incorporate a 16 to 1 multiplexer and a dual quaternary decoder. One of the most important feature that was taken into account was the area usage since that, in order to perform more complex functions, this circuit needs to be replicated a millions of times in the FPGA. Another important aspect is that in FPGAs the node capacitance can be very high and so, to cover most load cases, the circuit was designed to support a maximum load of 10pF.

This circuit depicted on figure 2.1 has two quaternary inputs, Q_A and Q_B, which are then computed by the dual quaternary decoder into the QLUT's binary control signals, B_{00}-B_{33}. The multiplexer 16-to-1 consists of sixteen NMOS switches enhanced with a clock boosting technique. When one of the control signals is high, the corresponding QLUT's line- switch- is activated connecting the corresponding QLUT's quaternary input to the output.

The four voltage levels are represented on table 2.1.

Value	Voltage Value[V]
0	0
1	0.404
2	0.707
3	1.2

Table 2.1: The four voltage levels.

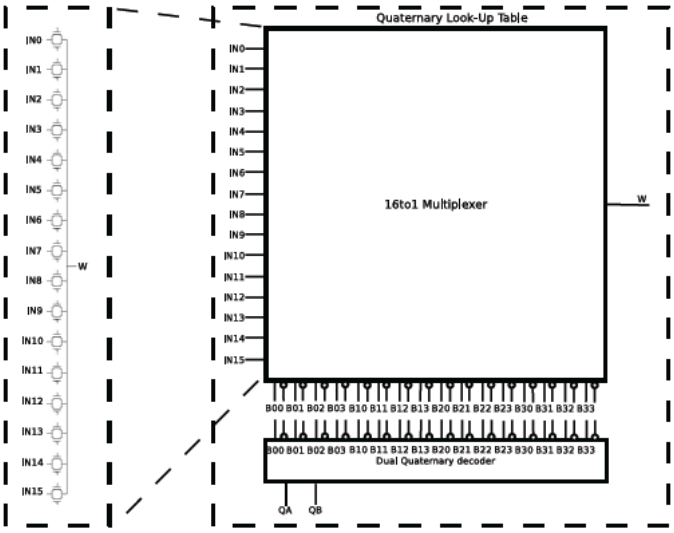


Figure 2.1: QLUT design

2.1.1 Dual Input Quaternary Decoder

The quaternary decoder, Figure 2.2, computes the two quaternary inputs into sixteen binary control signals and has the main advantage of using standard CMOS structures. It makes use of two self-referenced analog comparators, CP and CN, and logic gate inverters which are depicted in Figure 2.3. Using this structures the four voltage levels are detected since the comparators were design to detect and decode the quaternary input level and the self-reference voltages are 1/6V_{DD}, 3/6V_{DD} and 5/6V_{DD}.

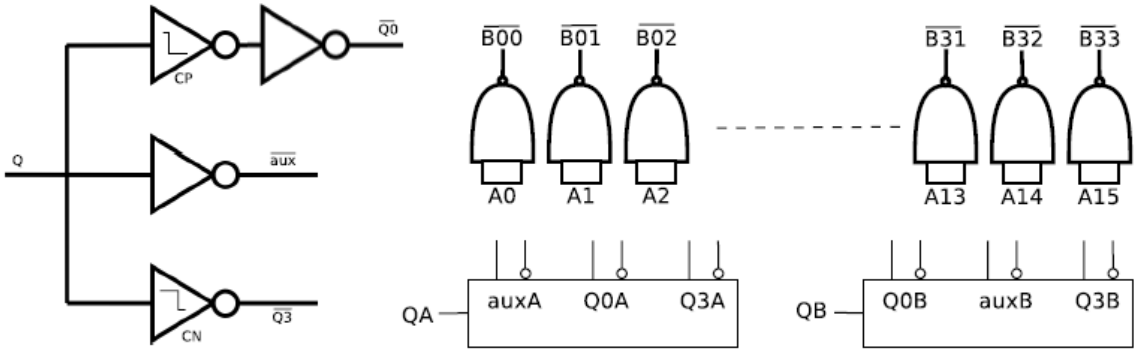


Figure 2.2: Q-decoder logic block diagram

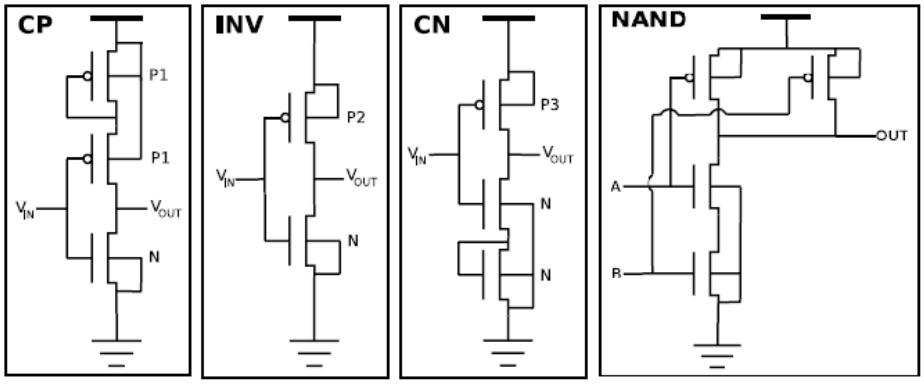


Figure 2.3: CP, INV, CN and NAND logic gates schematics

The quaternary decoder was implemented using NAND gates illustrated on figure 2.3. The inputs of the logic gates NANDs, `Ai`, are related to the truth table 2.2.

Q_A	Q_B	Logic Function	$Q_0(Q_A)$	Aux(Q_A)	$\overline{Q_3}$ (Q_A)	$Q_0(Q_B)$	Aux(Q_B)	$\overline{Q_3}$ (Q_B)	Control Signal
0	0	A0	1	1	1	1	1	1	B_{00}
1	0	A1	0	1	1	1	1	1	B_{01}
2	0	A2	0	0	1	1	1	1	B_{02}
3	0	A3	0	0	0	1	1	1	B_{03}
0	1	A4	1	1	1	0	1	1	B_{10}
1	1	A5	0	1	1	0	1	1	B_{11}
2	1	A6	0	0	1	0	1	1	B_{12}
3	1	A7	0	0	0	0	1	1	B_{13}
0	2	A8	1	1	1	0	0	1	B_{20}
1	2	A9	0	1	1	0	0	1	B_{21}
2	2	A10	0	0	1	0	0	1	B_{22}
3	2	A11	0	0	0	0	0	1	B_{23}
0	3	A12	1	1	1	0	0	0	B_{30}
1	3	A13	0	1	1	0	0	0	B_{31}
2	3	A14	0	0	1	0	0	0	B_{32}
3	3	A15	0	0	0	0	0	0	B_{33}

Table 2.2: Active output in function of the decoded quaternary inputs

	Power (µW)	Rise Time (ps)	Fall Time (ps)
Min.	17.23	26.52	23.64
Max.	38.28	90.52	86.54
Avg.	23.98	57.16	56.57

Table 2.3: Monte Carlo simulation results

On the table 2.3 are depicted the QLUT's results on Monte Carlo simulations.

2.1.2 Multiplexer 16-to-1

This part of the circuit was first implemented using standard CMOS transmission gates but, in order to achieve more competitive results, it was then modified to use a clock boosting technique.

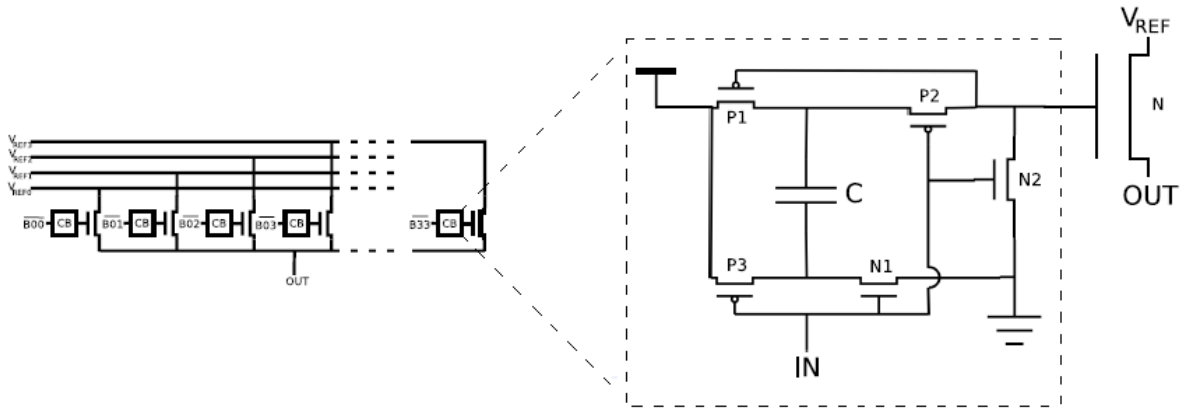


Figure 2.4: Multiplexer block diagram and clock boosting circuit schematic

To develop the multiplexer, the circuit on the right (figure 2.4) is replicated 16 times as depicted on the left of the Figure 2.4.

The clock boosting circuit is a custom circuit designed to have a small capacitance, because the input is an inverter of minimum dimensions. This alone proved to be an advantage from the first design, because having a small capacitance at the input allowed the decoder to be of minimal dimensions which in turn reduced the area.

This circuit works in two phases, when `IN=0`, transistors P1, N1 and N2 are `ON` which makes the transistor N to be turned `OFF` and the capacitor is charged to V_{DD}. This capacitor is dominant regarding the load so it only needs to be fully charged once at powering up since its charge loss will be small. In the second stage, when `IN=1`, P3 and P2 are `ON` which also switches transistor N `ON` connecting the corresponding input to the output.

Chapter 3

Methodologies

As it was referred in section 1, in order to supply the QLUT with the four voltage levels needed we require a voltage generator and a circuit to connect these two blocks. On the sections 3.1 and 3.2 we present the solutions researched for each block.

3.1 Interconnection's Matrix

3.1.1 First Proposed Solution

The first solution found is the most obvious one. It consists on adding a 64-to-16 multiplexer, before the Look-up Table, which would select a pre-set voltage for each of the QLUT's inputs according to the control values stored previously on registers.

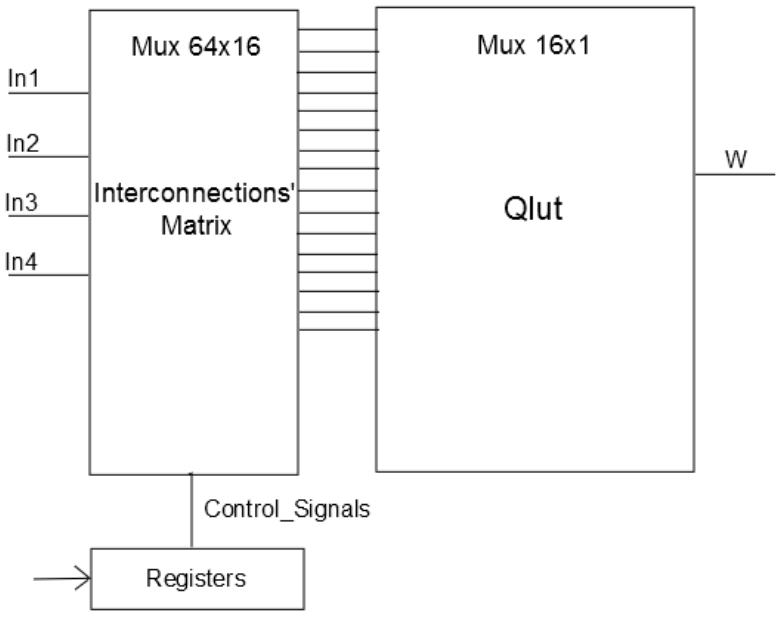


Figure 3.1: Simplified interconnection's matrix block diagram

This approach, although being the easiest to implement, has several disadvantages. First of all, instead of having one switch between the voltage supply and the output capacitor, it has an additional switch which increases the output impedance causing delays on the capacitor's charging. Taking into account that the circuit's area is an important aspect to evaluate, this approach would also fall short on the objectives previously defined. The new multiplexer would incorporate 64 standard CMOS switches which would represent an increase in area and it would just be an extension of the Look-Up table's multiplexer.

Because of the reasons enlisted above, it was concluded that this would not be the best implementation to use and so it was discarded.

3.1.2 Second Proposed Solution

The second implementation taken into consideration is to use a 16x1 RAM with 16 latches capable of storing quaternary voltage values instead of using the Quaternary Look-Up table already designed. This memory would be programmed at start-up with the values needed which would simplify the control routines.

This approach was discarded because the circuit's response time would be limited by the memory's reading cycle time. This would result in loosing the desired competitiveness regarding the existing implementations.

3.2 QLUT with a Voltage Generator Incorporated

Since all the circuits researched for the interconnection's matrix were proving to have more disadvantages than expected it was concluded that a detour from conventional approaches had to be made.

Taking into account the Digital-to-Analog Converter designed in [8], a new line of research was available. On figure 3.2 we have a circuit with a switch, a comparator and a capacitor and the idea is to charge the capacitor to a certain voltage level until the desired value is reached. This is achieved by having a comparator that keeps the switch `ON` until the value of the capacitor's charge reaches the defined value for comparison When this value is reached the comparator turns the switch `OFF`. The voltage value for comparison can be modified by changing the threshold voltage of the comparators' transistors and the capacitor's charge time depends on its capacitance and on the switch's resistance.

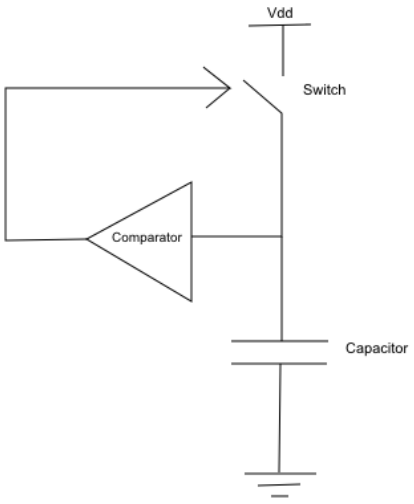


Figure 3.2: Simplified voltage generator block diagram

The circuit on figure 3.2 is only capable of charging but using the same concept it is possible to replicate the charging circuit and turning it into a discharging circuit by using the implementation on figure 3.3.

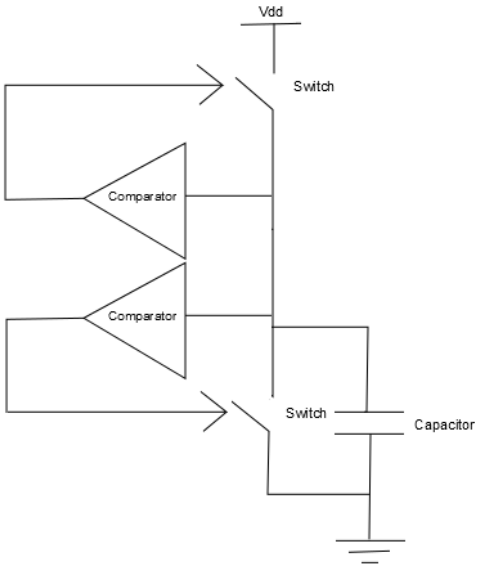


Figure 3.3: Simplified voltage generator block diagram with discharge circuit

Taking the diagram of figure 3.3 into consideration, a possible solution for the voltage generator is achieved. This voltage generator can be incorporated directly into the QLUT, because remembering figure 2.4 the multiplexer 16-to-1 represents a switch matrix which is the same as the switches included on the voltage generator.

The implementation of the voltage generator on the QLUT is depicted in figure 3.4.

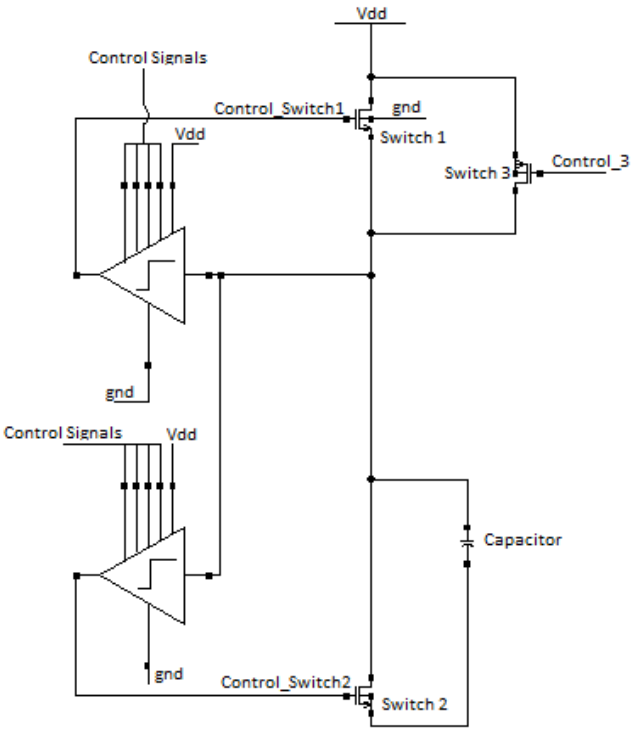


Figure 3.4: Qlut with voltage generator block diagram

With this implementation the capacitor is able to charge and discharge and so it is possible to replace the sixteen switches from the previous QLUT with the circuit of figure 3.4. In doing so, we have a new QLUT capable of generating its output dynamically and simultaneously we reduce the overall circuit's dimensions since there is no need to have a interconnections matrix and a 16-to-1 multiplexer.

In order to define the voltage value to be stored we have to change the comparator's value for comparison. This is achieved by using binary control signals, stored at start-up in latches, which will activate or deactivate some of the comparator's transistors.

Each of the QLUT's components will be explained in more detail on the sections that follow.

3.2.1 Comparators

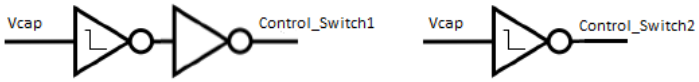
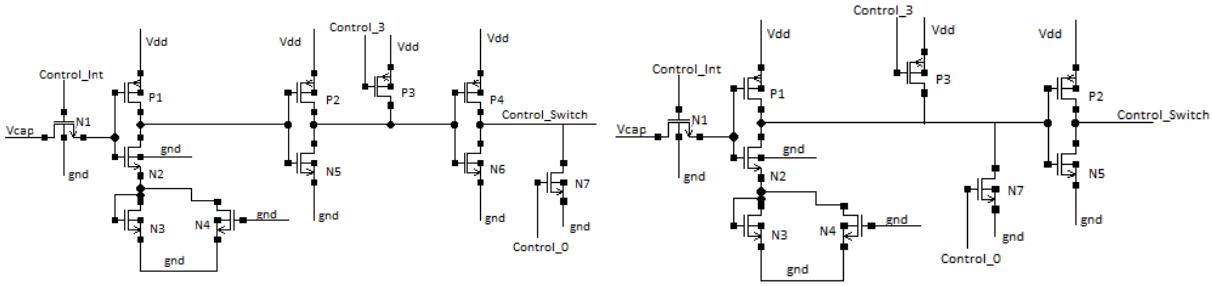


Figure 3.5: Comparators' block diagrams



(a) Charging Comparator Block diagram

(b) Discharging Comparator Block diagram

Figure 3.6: Comparators' Block diagrams

As it was said before, in order to change the value for comparison we need to change the transistors' threshold voltage. This is achieved by implementing a circuit controlled by binary signals which choose which transistors are active at each time. Regarding the values `0`(0V) and `3`(1.2V), there is no need for a comparison because, like in the binary case, we only have to force the switch `ON` or `OFF` during the charge or discharge.

After some DC simulations, the transistors' size are depicted on table 3.1.

Charge Comparator		
Transistor	length[nm]	Width[μm]
N1	120	20
N2	120	35
N3	120	42
N4	120	5.6
N5	120	2.72
N6	120	0.160
N7	120	0.260
P1	120	5.6
P2	120	9.36
P3	120	0.550
P4	120	0.550

Table 3.1: Charge Comparator's transistors' dimensions.

The charge and discharge of the capacitor cannot happen at the same time since this would cause a short-circuit between the ground and V_{dd} which would increase the power consumption. To prevent this

situation it was applied a hysteresis on the comparators.

The comparators' comparison values are the ones presented on table 3.2.

Comparator	Value Compared [V]
Charge	0.420
	0.708
Discharge	0.490
	0.787

Table 3.2: Comparators' values for comparison.

With the discrepancy on the values of the table 3.2 we also prevent the switches to be switching `ON` and `OFF` continuously which would result in fluctuations on the capacitor's voltage and would also increase the power consumption.

Both comparators are equal in design apart from the fact that the discharge comparator has one less inverter and some differences on the transistors' dimensions. Taking the example of the figure 3.6 and it's notation, the changes made on the dimensions are depicted on the table 3.3.

Discharge Comparator		
Transistor	length[nm]	Width[μm]
N2	120	10.6
N3	120	7
N7	120	5

Table 3.3: Discharge Comparator's transistors' dimensions.

3.2.2 Charge and Discharge Switches

Instead of having the switches incorporated with the clock boosting circuit from the previous QLUT, we now have three simple switches. The clock boosting switches removal was made, because the comparators used to control these switches are too slow compared to them. This causes the capacitor to charge/discharge to a voltage value higher/lower than it should. Due to this, the charge switch was replaced by a NMOS switch controlled by the charge comparator and the same was done for the discharge circuit.

The charging switch, Switch 1, was connected as seen on figure 3.4 in order to damp the charging ratio.

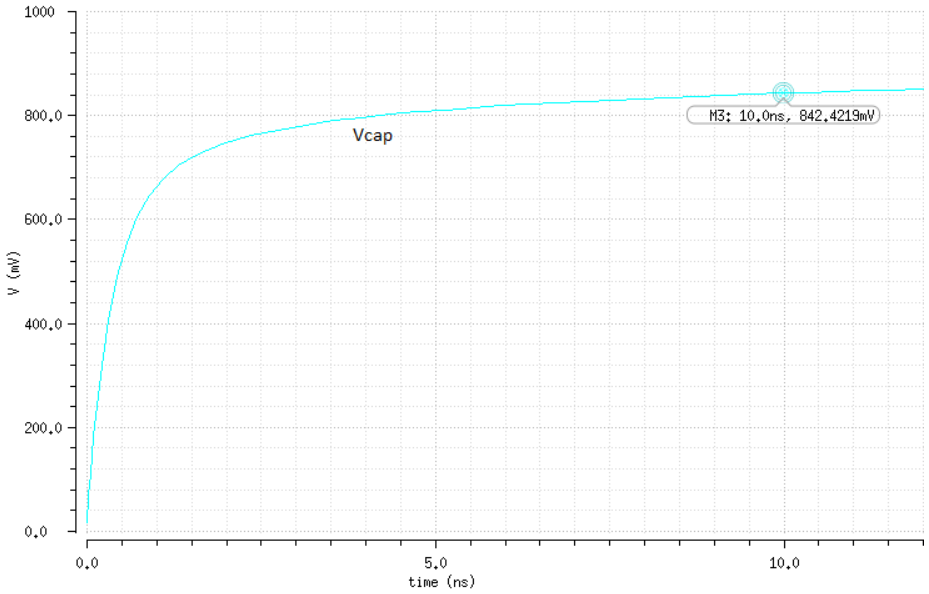


Figure 3.7: Charging of a comparator using a voltage follower NMOS switch

Due to it's characteristic, figure 3.7, the switch 1 slows down the charging for capacitor's voltage values near V_{cap}=$V_{dd} - V_t$. This switch can't be used to charge the capacitor with V_{dd}, because, considering the transistor on the saturation zone, we have 3.1.

$$I_D = 0 \Rightarrow I_D = k(V_{GS} - V_t)^2 = 0 \tag{3.1}$$
$$V_{GS} - V_t = 0 \Leftrightarrow V_G - V_S = 0 \Leftrightarrow V_S = V_{dd} - V_t$$

So theoretically, the capacitor can only charge until $V_{cap} = V_{dd} - V_t$ at most. The solution was to insert an additional PMOS switch in parallel which is only active when it's needed to charge the capacitor with V_{dd}.

The transistors' dimensions are presented on table 3.4.

Switches	length[nm]	Width[μm]
1 (NMOS)	120	30
2 (NMOS)	120	16
3 (PMOS)	120	34.4

Table 3.4: Dimensions of the switches transistors.

3.2.3 Control Signals

In order to control the capacitor's stored voltage value, we need four control signals.

The Control_0 turns the charging switch OFF and the discharge switch ON making the capacitor discharge. The Control_Int makes both comparators fix the stored voltage value in 0.726V and, if combined with the Control_1 fixes the voltage value in 0.438V. The Control_3 turns the Switch 3 ON while maintaining all the others OFF enabling the charge of the capacitor to V_{dd}.

Output value	Control_0 [V]	Control_Int [V]	Control_1 [V]	Control_3 [V]
0	1.2	0	0	1.2
1	0	1.2	1.2	1.2
2	0	1.2	0	1.2
3	0	0	0	0

Table 3.5: Control Signals' values.

Chapter 4

Preliminary Results

To test the circuit's response to the various charging and discharging situations, a transient analysis was made. On the figures 4.1, 4.2 and 4.3 are depicted the capacitor's charging from 0 to the other possible values.

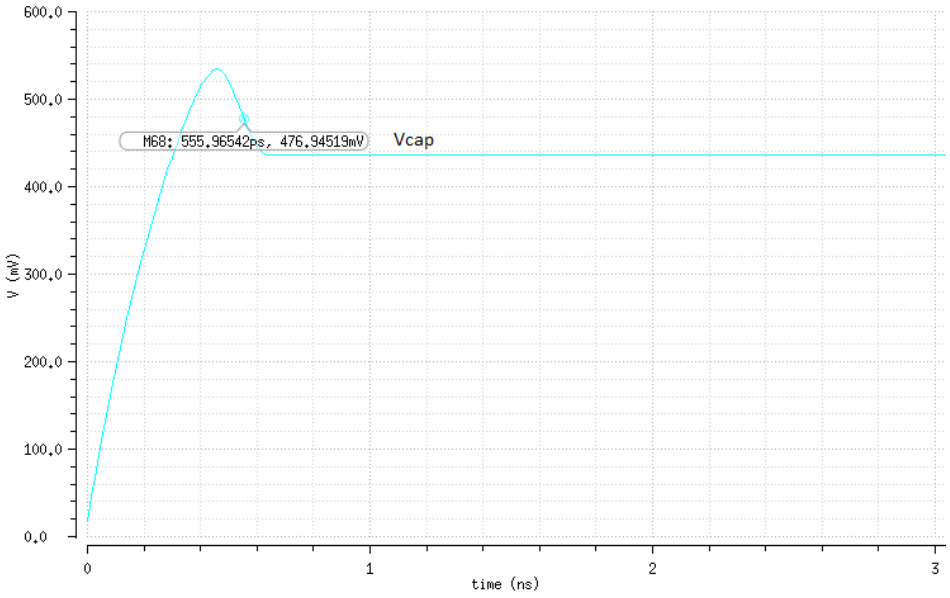


Figure 4.1: Capacitor's charging from the value 0 to 1

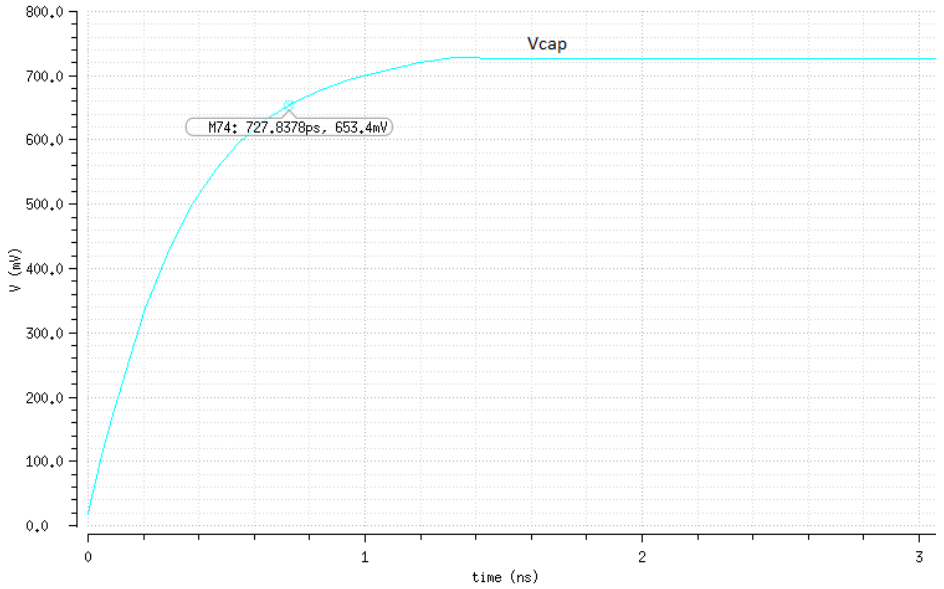


Figure 4.2: Capacitor's charging from the value 0 to 2

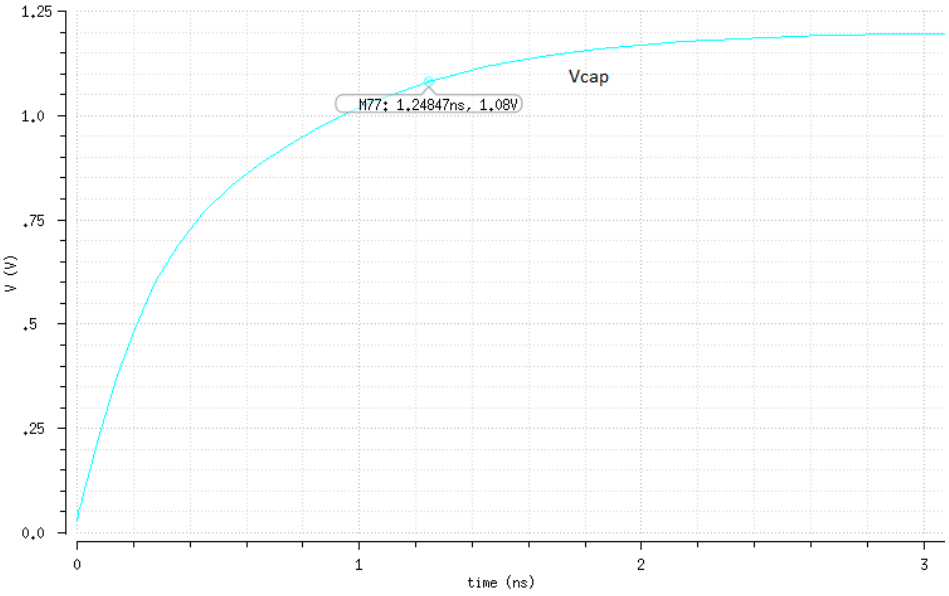


Figure 4.3: Capacitor's charging from the value 0 to 3

Charging			
Value	Theoretical Voltage [V]	Rise Time [ns]	Voltage stored [V]
0-1	0-0.404	0.630	0.436
0-2	0-0.707	0.697	0.726
0-3	0-1.2	1.21	1.2

Table 4.1: Capacitor's charging from 0 to the other values.

The Rise time results were calculated by measuring the time it takes for the signal to go from 10% to 90% of its final value.

Considering both the figures and the table 4.1, it is possible to conclude that, from a time perspective, all the capacitor's charging are within the time stipulated in [7], 1.5ns regarding a capacitor of 10pF.

On the figure 4.1 we can see a voltage peak with an amplitude of more than 0.500V. This happens because, the comparators are still slower than the charging and discharging switches and so the capacitor is charging too much and the discharging switch turns ON to fix the voltage value. This process causes a delay on the circuit's time response and that's why the circuit's charging times for the values 1 and 2 are similar.

The remaining charging results are depicted on the appendix A.

While testing the capacitor's discharge, the following results were obtained:

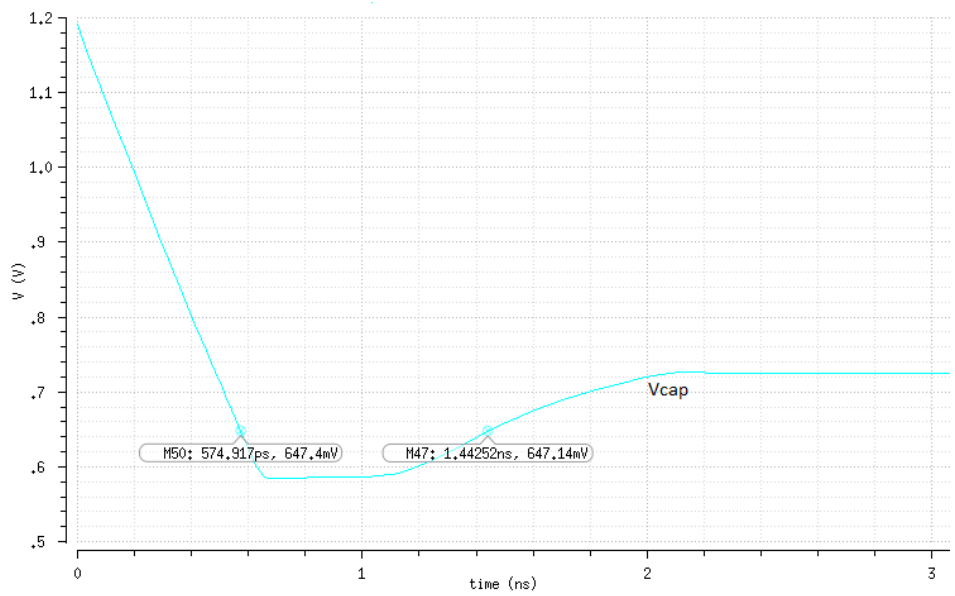


Figure 4.4: Capacitor's discharging from the value 3 to 2

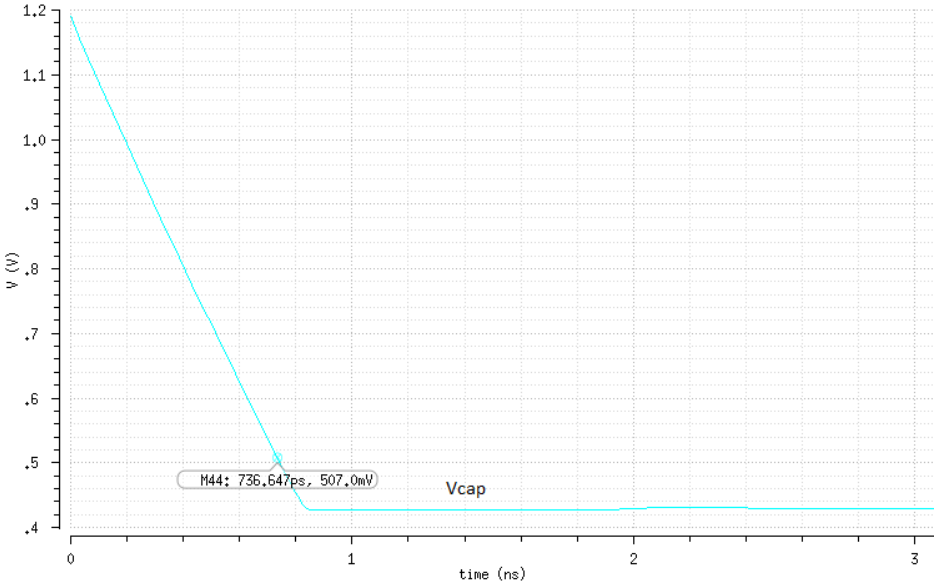


Figure 4.5: Capacitor's discharging from the value 3 to 1

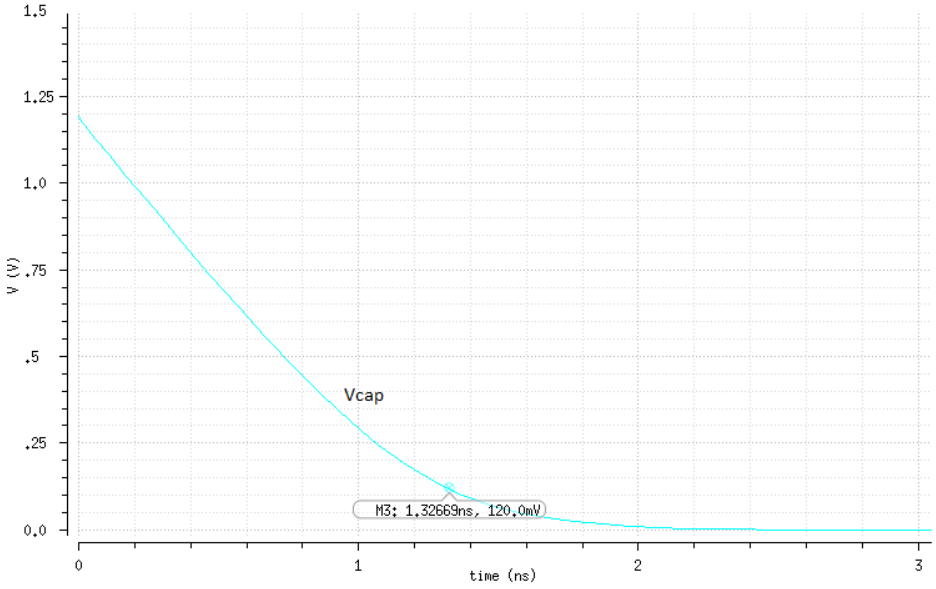


Figure 4.6: Capacitor's discharging from the value 3 to 0

Discharging			
Value	Theoretical Voltage [V]	Fall Time [ns]	Voltage stored [V]
3-2	1.2-0.707	0.523	0.725
3-1	1.2-0.404	0.669	0.430
3-0	1.2-0	1.25	0

Table 4.2: Capacitor's discharging from the value 3 to the other values.

The Fall time results were calculated by measuring the time it takes for the signal to go from 90% to 10% of its initial value.

On figure 4.4 we can see that, once again, the discharging switch's control is too slow and so the

capacitor discharges too much which activates the charging switch to achieve the desired voltage value. This situation is the one that poses the worst circuit's response. As it happened before, the fact that the capacitor needs to discharge and then charge once again causes a time penalty and the circuit's response time it's close to the time limit imposed.

The remaining discharging results are on the appendix B.

Future Work

Taking into account the results obtained in the section 4, the first improvement to be implemented will be to fix the situations where the switches' control is too slow to prevent a charge after a discharge or vice-versa. After this the circuit will be submitted to further testing.

The other blocks to be developed will be an auxiliary memory to store the control signals for every operation and the needed decoders. A first approach will be to implement two decoders where one will select the memory's line according to one of the two quaternary entrances (Q_A or Q_B) and the other one will select the column to activate according to the other quaternary entrance. For the memory, it will be implemented a 16 Latches circuit with each containing the four control signals needed.

Appendix A

Charging Results

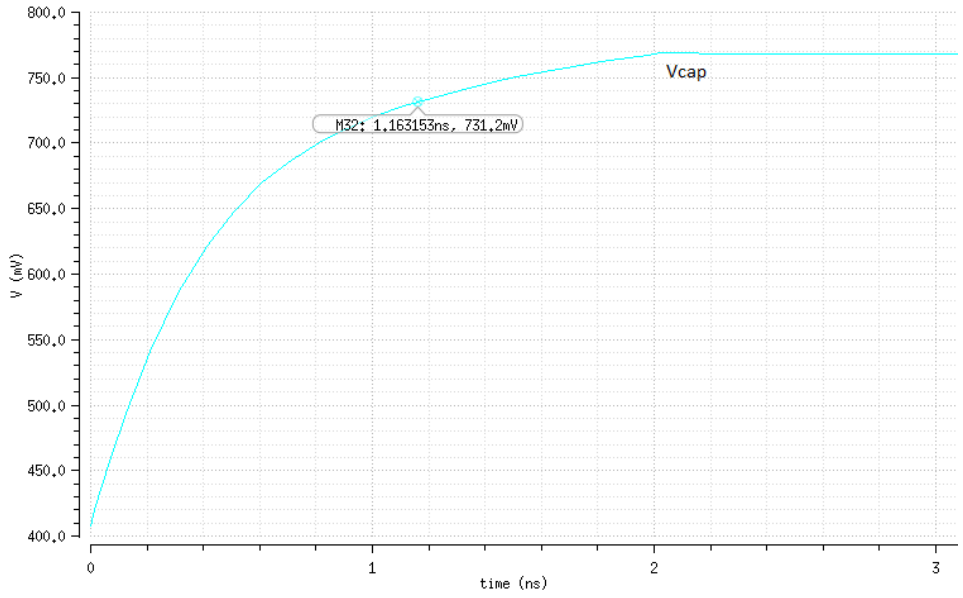


Figure A.1: Capacitor's charging from the value 1 to 2

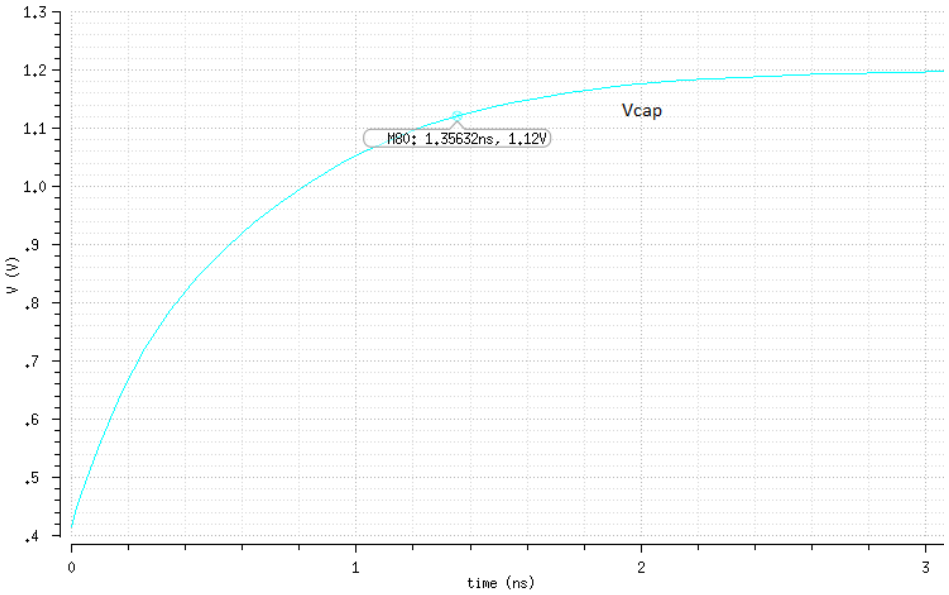


Figure A.2: Capacitor's charging from the value 1 to 3

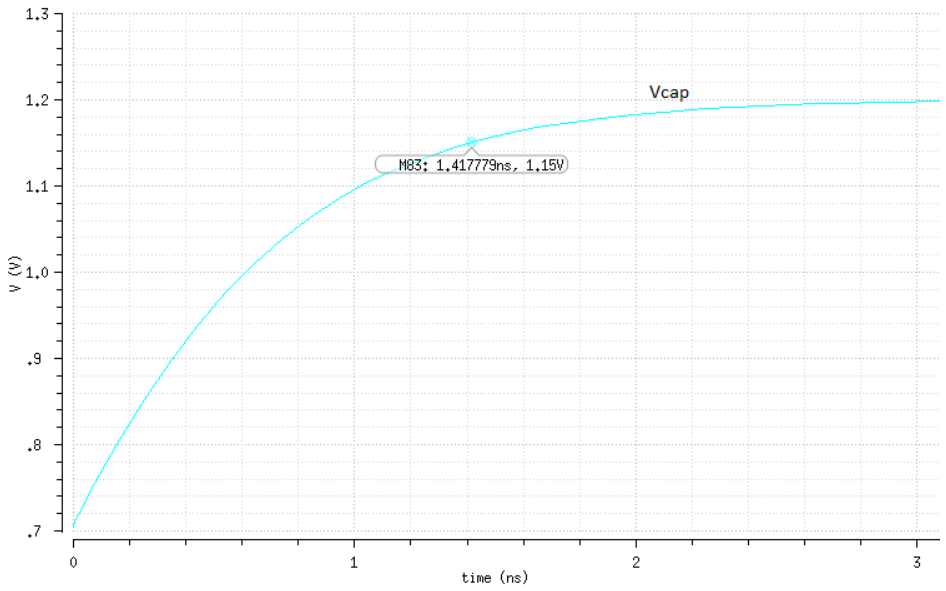


Figure A.3: Capacitor's charging from the value 2 to 3

Charging			
Value	Theoretical Voltage [V]	Rise Time [ns]	Voltage stored [V]
1-2	0.404-0.707	0.718	0.726
1-3	0.404-1.2	1.3	1.2
2-3	0.707-1.2	1.35	1.2

Table A.1: Capacitor's remaining charging situations.

Appendix B

Discharging Results

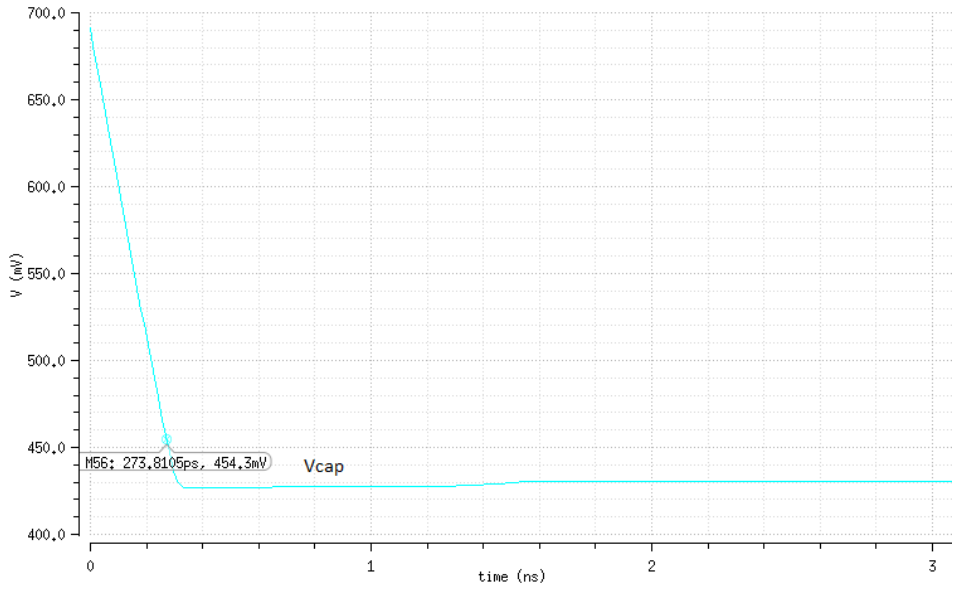


Figure B.1: Capacitor's discharging from the value 2 to 1

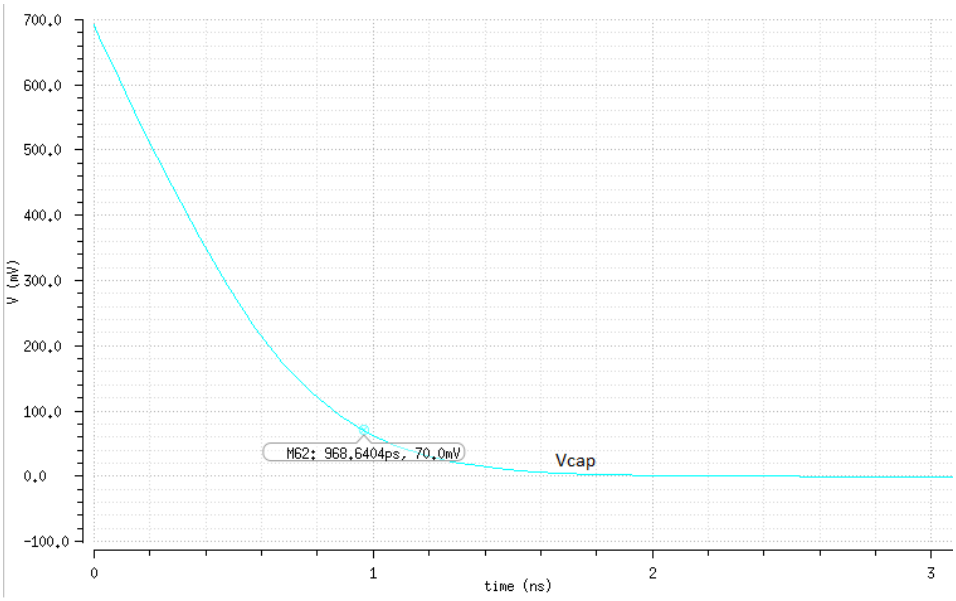


Figure B.2: Capacitor's discharging from the value 2 to 0

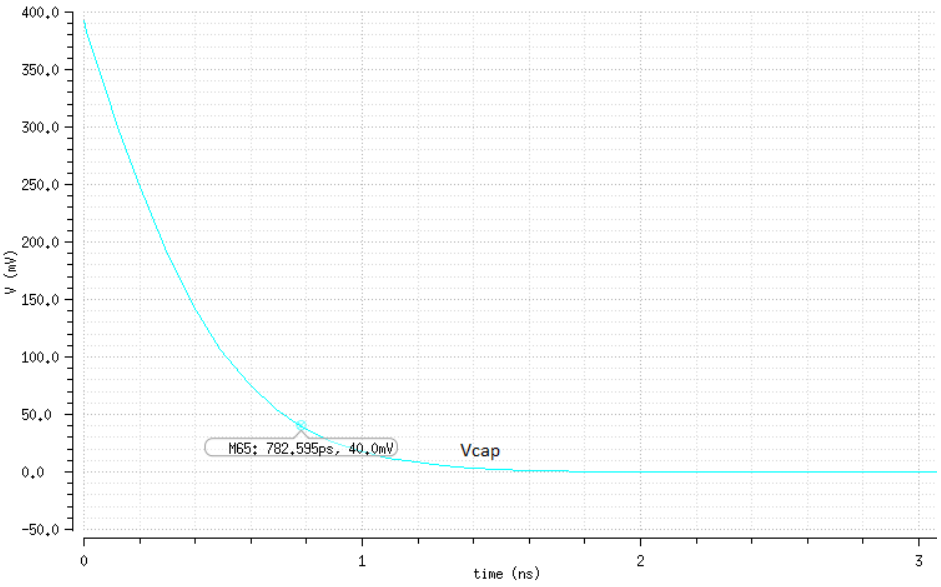


Figure B.3: Capacitor's discharging from the value 1 to 0

Discharging			
Value	Theoretical Voltage [V]	Fall Time [ns]	Voltage stored [V]
2-1	0.707-0.404	0.226	0.430
2-0	0.707-0	0.900	0
1-0	0.404-0	0.742	0

Table B.1: Capacitor's remaining discharging situations.

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