Smart Card Interface

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ESPRIT III Project # 6043 "QuickChips"

Task 2–5.1

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1 Introduction

This document contains all the relevant information used in the development of the "Smart Card Interface" circuit.

This circuit intents to demonstrate the QuickChips design methodology, using the design environment installed at INESC. The manufacturing and test of this circuit, should also demonstrate the capability of the mini-fab installed at INESC and the overall QuickChips project.

The circuit was described using a synthesizable subset of VHDL that, after being simulated for functionality check, was mapped to the IMS Gate Forest 1.2 micron technology, using the Synopsys synthesis tool. After a logic simulation the circuit was placed and routed using the IMS GF4 master wafer.

This document is organized as follows:

- Section 2 describes the circuit functionality and its normal operation mode.
- Section 3 describes the internal structure of the circuit.
- Section 4 presents the file organization used to describe the circuit in VHDL.
- Section 5 describes the synthesis results of VHDL circuit description.
- Section 6 mentions the simulations performed to check the circuit.
- Section 7 presents the details of the circuit layout.