MIC30
A Telecom Circuit Design
to
Test the CAD-VTQL Interface Constraints

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1 Introduction

This report summarizes the experience in the design of a gate array used to test the DWL machine and give some insight for the CAD-VTQL interface constraints.

A version of a telecommunication circuit has been re-designed with the current Lasarray Library and CAD interface.

2 Description of the Circuit

The circuit chosen for the test was a previously designed and fabricated telecommunication circuit. This integrated circuit is currently working in an equipment used by a Portuguese telecommunication company.

The circuit, named MIC30, is fully digital and is part of a PCM multiplex equipment operating at 2048 Kbits/s. It has the following inputs: a system clock and reset, a serial input line, a selection for the present or the previous byte of information and an option to select how the system will acquire synchronization. The bit stream received in the serial line are arranged in frames as defined in [1]. The circuit must receive the frames, of 256 bits each and provides the following functions:

- Detection the first byte as the frame alignment byte for synchronization of the system
- Output in parallel the remaining bytes of information read
- Generation of the position in the frame of the current output byte
- Generation of signals to synchronize emission with reception

The implementation of this circuit included as basic functional blocks serial to parallel converters, multiplexers, counters, a “comparator” and a finite state machine to control the system synchronization. The overall system has about 800 equivalent gates.

3 The Design of the Circuit

As this circuit had already been implemented in another technology the documented schematic was used as the entry point for the design.

The system used was the Lasarray Design System MENU V4.2a running in a IBM-PC compatible station with a dedicated board. After the choice of the chip type for the integrated circuit, in our case XLD5000, the designer must go through the following steps: schematic entry and conversion, model compilation, simulation and test generation and physical layout.

The schematic entry was made using the OrCAD program with the Lasarray library. This means there was a manual technology conversion from the existing cells in the original schematic, to the cells in the current Lasarray library.

The next step is the model compilation, here the package type was chosen and the pad assignment was defined. For the MIC30 a ceramic Dual Inline Package (DIP) with 28 pins was chosen.

Two types of simulation have been done. One, before the physical layout just to verify the correct functionality of the circuit, and another after the layout taking into account the more real delays between the connections.

The physical layout, which consists in the placement and routing of the cells was done in a completely automatic way creating a CIF file. This file was afterwards processed to generate the data for the exposure with the DWL machine.

4 Conclusions and Future Work

We have used the design of a real telecommunication circuit, MIC30, to provide some insight about the constraints of the CAD-VTQL interface, as well as to test the DWL machine.

The exposure of MIC30 with the DWL machine was successfully done and two chips have been fabricated. The chips functionality and performance will be checked in a tester machine.

Future work will include the integration of the DWL machine in the design system described in [2]. This involves the development of an interface that automatically transfers the CIF files to the DWL machine.

A Schematics

In this appendix the most representative schematics of MIC30 are presented.

- Top-level schematic with the pads (MIC30)
- The shift register (SR)
- A counter (CO9)
- The finite state machine (UC)
- Two multiplexers (MUX5 and MUX1)

B Layouts

The layouts of the circuit are showed just with the metal-2 layer.

References

[1] CCITT. *Yellow Book, Fascicule III.3*, 1981. Recommendation G.732.

[2] José Carlos Monteiro. A restricted version of the cad design system (front end tools). QuickChips Deliverable 10, INESC, 1991.