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Power Reduction in BIST by Exploiting Don't Cares in Test Patterns

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Abstract —

For a significant number of electronic systems used in safety-critical applications circuit testing is performed periodically. For these systems, power dissipation due to Built-In Self Test (BIST) can represent a significant percentage of the overall power dissipation. One possible solution to address this problem consists of test pattern reordering with the purpose of reducing the amount of power dissipated during circuit testing. By reordering test patterns one is able to find test sequences for which power dissipation is minimized. Moreover, a key observation is that test patterns are in general expected to exhibit don't cares, which can naturally be exploited during test pattern reordering. In this paper we describe efficient algorithms for test pattern reordering in the presence of don't cares. Preliminary experimental results amply confirm that the power savings due to test pattern reordering using don't cares can be significant.

1. Introduction

This paper addresses the problem of reducing power dissipation during Built-In Self Test (BIST). In applications where BIST is applied periodically, BIST power reduction techniques can significantly contribute to overall power reduction. It is well-known that power dissipation during circuit testing can be achieved by reordering the testing sequence [2]. However, existing approaches explicitly assume completely specified test patterns. In general, however, test patterns need not be completely specified. Indeed, incompletely specified test patterns can play a key role in BIST design [1]. The purpose of this paper is to describe techniques for BIST power reduction in the presence of don't cares. Experimental evidence obtained on a significant number of benchmark circuits clearly shows that exploiting don't cares in test patterns can lead to very significant savings in overall power dissipation.

2. Model and Algorithms

Let $\{T_1, T_2, \ldots, T_m\}$ be a given sequence of *completely specified* test patterns. The problem of power reduction during BIST can be formulated as the identification of a permutation $\langle i_1, \ldots, i_m \rangle$ such that the power of applying a sequence of test patterns $\langle T_{i_1}, T_{i_2}, \ldots, T_{i_m}, T_{i_1} \rangle$ is minimal over all possible permutations. In the model we derive below we explicitly assume that power dissipation is proportional to the Hamming distance between test patterns. Even though this assumption does not necessarily hold true in general, it is amply validated by the experimental results given in Section 3.

The problem of power reduction can naturally be reduced to the traveling salesman problem (TSP). Indeed, by viewing each test pattern as a vertex in a graph, and the Hamming distance between each pair of test patterns as the weight between those two vertices in the graph, then the sequence that minimizes power dissipation during BIST corresponds to a tour of least weight in the graph, i.e. the solution to the TSP. Consequently, different polynomial-time approximation algorithms can be used [4].

This simple model explicitly assumes that test patterns are completely specified. Hence, if test patterns have unspecified bits, then the straightforward reduction to the TSP no longer holds true. Indeed, edge weights in the graph representation of the test pattern reordering problem can now be viewed as conditional values, that depend on the final value of bits unspecified in each test pattern. To solve this new optimization problem we propose the following heuristic procedure which is based on TSP approximation schemes:

1. Use a dedicated algorithm for computing a test set where each test pattern contains don't cares [3].
2. Apply a heuristic procedure for identifying an initial tour. Several different heuristics are described below.
3. For the initial tour, compute the tour cost by specifying don't care bits which minimize the distance between consecutive test patterns.
4. Use the 2-opt local-search approximation algorithm for the TSP [4] to reorder the test patterns.
5. At each step of the 2-opt algorithm, and while the total tour cost is being reduced, repeat step 3.

Benchmark	O	H1	H2	H3	H4	H5
9symml	46.9	-3.3	-2.4	3.9	-1.2	3.0
c17	-25.1	32.6	12.9	47.0	9.1	35.6
cht	12.4	30.9	38.2	33.6	34.4	11.5
cm138a	29.9	22.7	29.9	30.2	33.5	26.4
cm150a	19.6	38.5	40.3	53.3	42.8	50.1
cm163a	19.3	71.8	75.2	79.3	42.7	70.2
cmb	41.7	38.6	37.3	39.0	34.6	32.1
cordic	29.5	66.7	67.2	69.6	67.1	65.1
majority	26.7	-2.9	9.1	4.8	-1.9	1.9
mux	16.8	44.1	44.8	52.6	44.2	52.0
sao2	42.5	17.5	23.4	21.0	13.7	13.4
c432	26.3	64.1	58.4	56.3	59.1	59.5
c880	11.9	49.6	53.9	50.9	49.4	52.3

Table 1: Power reduction due to exploiting don't cares

The following initial ordering heuristics have been implemented:

1. Random ordering.
2. Decreasing order of don't cares in each test pattern.
3. Apply heuristic 2. Afterwards, greedily select the next test pattern as one that minimizes the distance from the current test pattern.
4. For each bit position set don't care bits to the bit that occurs more often. Afterwards order the test vectors approximating Gray coding.
5. Same as heuristic 4., but without ordering the test vectors. Afterwards, the Christofides TSP approximation algorithm [4] is used for defining an initial tour.

3. Experimental Results

The results of applying the different variations of the algorithm to several benchmark circuits are shown in Table 1. Column labeled **O** denotes the percentage power savings from an unordered test set (obtained with ATALANTA [5]) to a test set ordered with the Christofides approximation algorithm [4]. In this case test patterns are completely specified.

The key experiment consisted of using MTP [3] to generate test sets with a large number of don't cares. Afterwards, the algorithm described in this paper was applied. The obtained experimental results are shown in Table 1, where different initial ordering heuristics (**H1** to **H5**) were used. Note that the percentage power savings shown are relative to the already *ordered* completely specified test set, which in general already represents an improvement over the initially *unordered* completely specified test set obtained with ATALANTA. As can readily be concluded the attained power savings can be significant.

4. Conclusions

In this paper we propose a model and algorithm for test pattern reordering in the presence of don't cares. An immediate application is the reduction of dissipated power during BIST. Even though we describe a simple heuristic approach for solving this problem, preliminary experimental results indicate that very significant savings in dissipated power can be achieved by applying the proposed procedure.

Additional research work entails the introduction of a more detailed model, intended to accurately predict power dissipated during transitions between test patterns, and studying alternative algorithmic solutions.

References

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