Quaternary Logic Lookup Table in Standard CMOS

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***Abstract*— Interconnections are increasingly the dominant contributor to delay, area and energy consumption in CMOS digital circuits. Multiple-valued logic can decrease the average power required for level transitions and reduces the number of required interconnections, hence also reducing the impact of interconnections on overall energy consumption. In this paper, we propose a quaternary lookup table (LUT) structure, designed to replace or complement binary LUTs in field programmable gate arrays. The circuit is compatible with standard CMOS processes, with a single voltage supply and employing only simple voltage-mode structures. A clock boosting technique is used to optimize the switches resistance and power consumption. The proposed implementation overcomes several limitations found in previous quaternary implementations published so far, such as the need for special features in the CMOS process or power-hungry current-mode cells. We present a full adder prototype based on the designed LUT, fabricated in a standard 130-nm CMOS technology, able to work at 100 MHz while consuming 122 μW. The experimental results demonstrate the correct quaternary operation and confirm the power efficiency of the proposed design.**

***Index Terms*— Field-programmable gate array (FPGA), lookup table (LUT), multiple-valued logic (MVL), quaternary logic, standard CMOS technology.**

I. Introduction

IN CONVENTIONAL binary CMOS digital circuits, static power consumption is tightly related to leakage currents, and dynamic power consumption is determined by (1), where C is the capacitance of the nodes being driven and V_{DD} is the power supply voltage

$$P_D \propto CV_{DD}^2. \tag{1}$$

The CMOS process has evolved by shrinking the transistors (thus reducing C) and employing lower supply voltages (lower V_{DD}), therefore saving power and integrating more functionality into the same area. However, capacitance C also includes the routing capacitance associated with the wires connecting the logic gates. It has been reported that routing is exceeding transistors contributions for latency and power dissipation of designs in modern CMOS processes [1]. This is particularly compelling in modern field-programmable gate arrays (FPGAs), where the power spent in routing may reach up to 70% of the overall consumption [2]. Due to its reconfigurability, FPGAs play an important role in modern digital systems design, as they allow an earlier time-to-market and reduced engineering change order costs when compared with application-specific integrated circuits (ASICs).

An approach to mitigate the impact of interconnections is to use multiple-valued logic (MVL) [3], hence, more information can be carried in each wire, reducing the routing network. Therefore, a single wire carrying a signal with N logic levels can replace $\lfloor \log_2 N \rfloor$ wires carrying binary signals. Reducing the routing leads to a direct reduction of the line capacitances and the overall circuit area. Therefore, this enables increasing the maximum operation frequency and reducing the power consumption. Moreover, logic levels become closer to each other, further reducing the average power needed for level transitions. The new power consumption can be determined by (2), where V_{av} is the average voltage distance between logic levels

$$P_D \propto CV_{DD}V_{av}. \tag{2}$$

A more detailed analysis of the energy consumption in quaternary (base 4 representation) buses and a comparison to their binary counterparts is shown in [4]. However, in spite of these advantages, it is known that the use of MVL comes at the price of having relatively lower noise margin than the binary, therefore its use is commonly not trusted. While there is still large and foreseeable room for power optimization exploiting the shrinking and supply voltage reduction of CMOS devices, MOSFET shrinking is expected to saturate as transistors approach atomic dimensions, imposing a fundamental barrier. Furthermore, supply voltage reduction is limited by practical boundaries; the transistors threshold voltage (V_{th}) cannot be reduced proportionally to the power supply voltage as it leads to an increasing leakage current, therefore increasing the static consumption of CMOS circuits. The exposed limitations encourage the exploration of circuit and system-level techniques to achieve higher energy efficiency. This may include dropping conventional noise margins of binary levels and, therefore, dealing with less-comfortable noise margins of the MVL logic should be considered. However, previously reported implementations of MVL either present high power consumption, due to current-mode circuit elements [5]–[7],

Manuscript received June 17, 2013; revised December 8, 2013; accepted February 3, 2014. Date of publication March 19, 2014; date of current version January 30, 2015. This work was supported by the National Funds through FCT-Fundação para a Ciência e Tecnologia under Project PEst-OE/EEI/LA0021/2013 and Project QCell EXPL/EEI-ELC/1016/2012.

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Digital Object Identifier 10.1109/TVLSI.2014.2308302

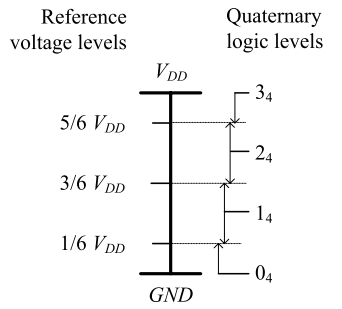


Fig. 1. Quaternary logic and reference voltages levels.

or require nonstandard multithreshold CMOS technologies [8]. These drawbacks have prevented MVL from being competitive when compared with binary logic.

This paper proposes a novel view of MVL circuits through the design of a look up table (LUT) based on the quaternary representation that exploits simple voltage-mode standard CMOS circuits and optimized switches using a simplified clock boosting (CB) technique. The proposed MVL LUT can replace or complement conventional binary logic, since the designed circuit is simple, efficient and we can combine both; i.e., they use the same implementation/fabrication technology. We have implemented and fabricated a circuit in a standard 130-nm CMOS technology, requiring a single supply voltage of 1.2 V. We present experimentally measured results to support the proposed ideas.

This paper is organized as follows. In Section II, we review the basic concepts of quaternary logic and LUTs. Then, in Section III the quaternary LUT (QLUT) topology and circuits are proposed, together with some design guidelines. In Section IV, the QLUT circuits dimensioning is described and the simulation results are presented. In Section V, a full adder prototype based on the proposed QLUT is developed. Section VI presents the experimental results obtained for the fabricated circuit followed by a brief discussion. Finally, Section VII summarizes and concludes this paper.

II. Quaternary Logic and LUTs

A quaternary variable can assume four different logic levels. Assuming a rail-to-rail voltage range and equal noise margins for the four logic levels, three different reference voltage values are required, $1/6V_{\mathrm{DD}}$, $3/6V_{\mathrm{DD}}$, and $5/6V_{\mathrm{DD}}$, to determine a quaternary value. This is shown in Fig. 1. Since a quaternary variable (Q) is able to carry twice as much information as a binary variable (B), we have the following relation:

$$|Q| = 2 \times |B|. \tag{3}$$

Therefore, two binary variables may be grouped into one quaternary variable without information loss, merging two nodes into one. It should be noted that there is no direct conversion of binary to quaternary logic gates in conventional CMOS, since the binary circuits use the available power rails to represent the binary symbols. For quaternary logic there are two more intermediate levels, which cannot be obtained directly using the same techniques. On the other hand, viable implementations of quaternary circuits have already been

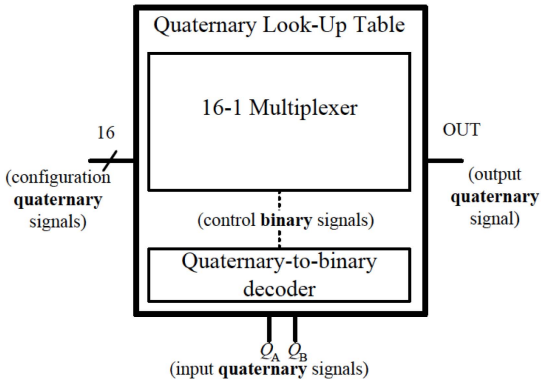


Fig. 2. Proposed quaternary LUT.

achieved for LUTs, as demonstrated in [9]. A LUT is an array indexing operator, where the output is mapped by the input, based on the configuration memory. The configuration values are initially stored in the LUT configuration memory, and according to the input, the logic value in the addressed position is assigned to the output. By properly programming the LUT configuration memory, the LUT can implement any logic function with the given number of inputs and outputs, making it very practical to implement reconfigurable hardware, such as FPGAs.

A quaternary function implemented by a QLUT is defined as $g : Q^k \rightarrow Q$, over a set of quaternary input variables $Y = (y_0, \ldots, y_{k-1})$, where the values of a variable y_i and the function $g(Y)$ are defined in $Q = \{0, 1, 2, 3\}$. In general, if l is the number of logic levels, the total number of different functions $|F|$ that can be implemented in a LUT is given by

$$|F| = l^{|n \times l^k|} \tag{4}$$

where n is the number of outputs and k is the number of inputs. For a LUT with a single output ($n = 1$), the number of different functions for binary ($l = 2$) and quaternary ($l = 4$) representations is given, respectively, by

$$|F_2| = 2^{2^k} = 4^k \quad |F_4| = 4^{4^k} = 256^k. \tag{5}$$

The number of possible functions that may be represented in a quaternary LUT is much larger than in a binary LUT with the same number of inputs and outputs. Therefore, apart from reducing the total number of connections, MVL also leads to a reduction of the total number of gates when compared with a binary implementation.

III. Proposed QLUT Topology and Implementation

The proposed 2-input 1-output QLUT is shown in Fig. 2. For this given QLUT complexity, 16 quaternary configuration inputs are necessary, one for each possible combination of the two quaternary inputs. The configuration word defines the reconfigurable quaternary function. In practice, the input signals are used to select which one of the configuration inputs is connected to the output. The proposed QLUT is composed of two main blocks: a 16-1 multiplexer using an array of switches, that establishes a low-resistance path between one configuration input and the output according to the input values; and a quaternary-to-binary decoder, consisting of a

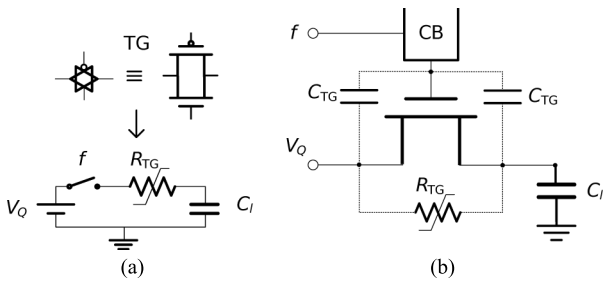


Fig. 3. (a) Multiplexer path RC model. (b) CB switch.

2-bit analog-to-digital (ADC) frontend followed by combinational logic used to generate the control signals feeding the multiplexer. These blocks are described in the following sections.

A. 16-1 Multiplexer

Due to the quaternary nature of its inputs, the 16-1 multiplexer shown in Fig. 2 may be thought of as an analog multiplexer. The output is assumed to be of a capacitive nature and its value is defined by the interconnection network to which the QLUT output is connected. For a binary FPGA this value can go up to tens of pF [10]. Although, the use of quaternary logic allows to reduce the number of wires, leading to a compact layout, reducing the routing capacitance. We used the typical value for a binary FPGA (10 pF), since it allows us to consider that maintaining the same number of wires, we can increase the functionality within the FPGA.

The multiplexer path is usually implemented by transmission gates (TGs), which can be modeled by a simple RC circuit, as shown in Fig. 3. The charging time is proportional to the RC time constant, and since the capacitance is already constrained, the only way to reduce propagation delay is to decrease the switch resistance. The straightforward approach to reduce the switch resistance is to increase the transistors width. On the other hand, this increases the gate capacitance, leading to a power increase to turn it on. Moreover, TGs are known to behave worse when the signals are far from the supply rails [11]. This is particularly severe for the intermediate levels in quaternary signals, since there is a reduced overdrive voltage on the MOS transistors. We evaluated two techniques to implement the multiplexer switches, the use of a CMOS TG, Fig. 3(a), and the use of a single nMOS transistor controlled by a CB circuit, Fig. 3(b), which was the implemented solution, justified in detail in Section III-A.

A common approach for a 2-input QLUT is to employ two switches in series inside the multiplexer as used in [9], shown in Fig. 4(a). In this paper, we propose to use a single switch, as shown in Fig. 4(b), yielding in a reduced resistance path and consequently improving the QLUT speed, at the price of increasing slightly the decoder complexity and of an additional CB circuit to control a single nMOS switch.

B. Clock Boosting Switch

The CB circuit is obtained by reasoning on the high level models shown in Fig. 5(a), where the two operation phases of the technique are depicted: in phase 1, the capacitor C is charged to V_{DD}, and the switch (an nMOS transistor) is open since its gate is connected to ground; in phase 2, C is disconnected from the voltage supply, maintaining its charge, while the bottom plate is referenced to V_{DD}. Therefore, the switch gate voltage is raised to $2V_{DD}$. This high level circuit is usually implemented simply by replacing the switches by TGs and relying on a clock generator circuit to control its phases, which, depending on the implementation, may have to be nonoverlapped.

Fig. 5(b) shows the high level model of the proposed circuit, which is similar to the model in Fig. 5(a) except that two of switches are identified as an inverter, reducing the number of elements and eliminating the two phase clock generation circuitry. This inverter can be used to delay the signal while simultaneously implementing the nonoverlapping clock used to control the other switches. The complete circuit can now be reduced to the circuit in Fig. 5(c) [12] that works as follows: assuming that the capacitor C is initially discharged and clk_1 is set to logic 1 (V_{DD}), N_1 turns on and connects node B to ground, while P_1 turns off and ensures a high impedance path between the nodes A and B. Simultaneously, P_2 is on and gradually charges the capacitor (and node A) to V_{DD}. When clk_1 commutes to a logic 0 (ground), N_1 turns off; the inverter ties the capacitor bottom plate to V_{DD} and P_2 turns off; node A rises to $2V_{DD}$ and P_1 is turned on connecting node B to $2V_{DD}$ as wanted.

In practice, a slightly lower voltage is obtained due to charge redistribution with the transistor N_{SW} gate capacitance. This small voltage drop prevents the transistor from working under a gate voltage close to the maximum voltage allowed for the technology (2.7 V), avoiding premature aging effect on this large transistor. In addition, since we are applying a higher voltage than supply to the drain-source of the transistor N_1, we are also compromising its long term use. However, a solution for this problem is to use an nMOS in series with N_1, avoiding the drain-source voltage to be higher than V_{DD}, in each transistor. It should also be noted that a full charge of this capacitor only occurs once at powering up, from then on the capacitor only loses charge due to charge distribution with the switch gate capacitance.

C. Quaternary-to-Binary Decoder

The 2-bit quaternary-to-binary decoder allows the use of a single row of switches to drive the input configuration signals to the output of the QLUT. To do so, it is necessary to generate 16 control signals, to be applied in the clk1 inputs of each switch, shown in Fig. 5(c). These switches are employed to connect one quaternary configuration input to the output. To generate the required control signals, the quaternary variables are decoded into binary, allowing the use of binary logic gates. Thus, an ADC frontend is necessary, considering the analog nature of the quaternary signals. We have implemented inverting self-referenced comparators, shown in Fig. 6, where Q_i is a quaternary input of the QLUT. The main advantage of this structure, also used in [9], over previously proposed implementations is that it only uses standard CMOS structures. Fig. 7 shows the ADC frontend, where the binary signals

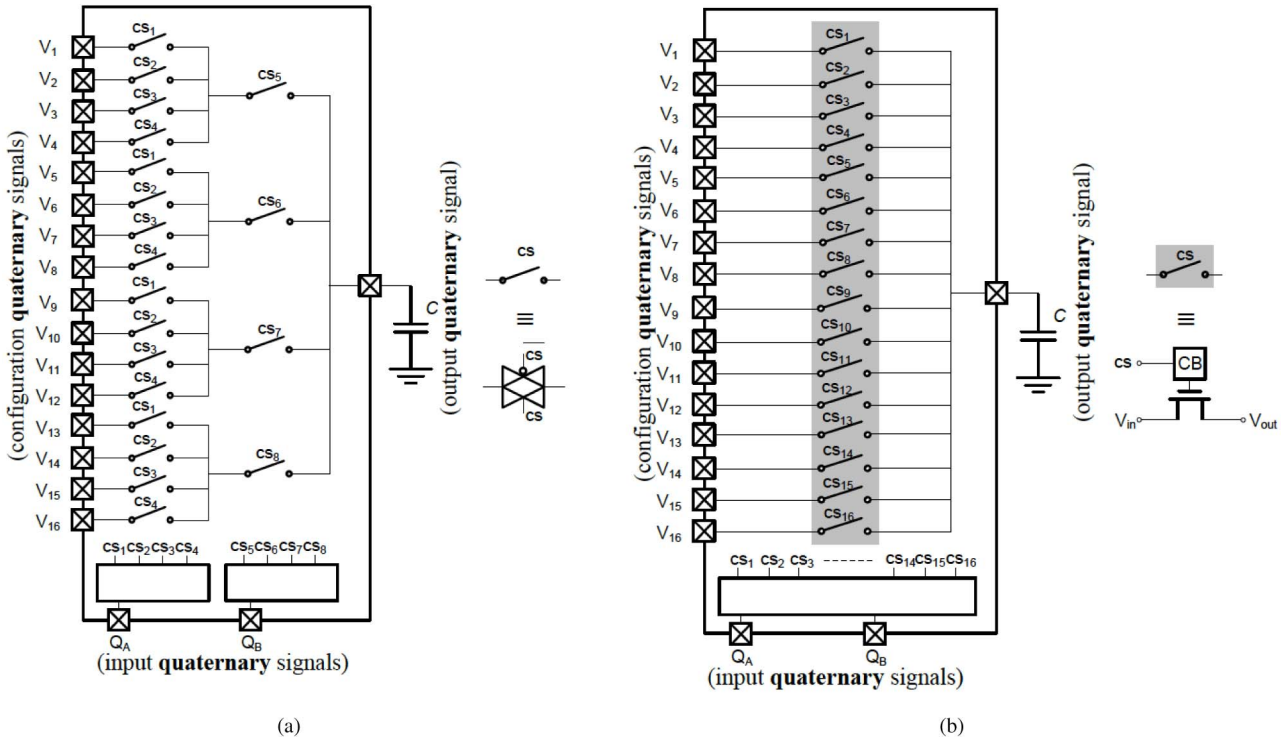


Fig. 4. QLUT. (a) Previous implementation. (b) New proposal.

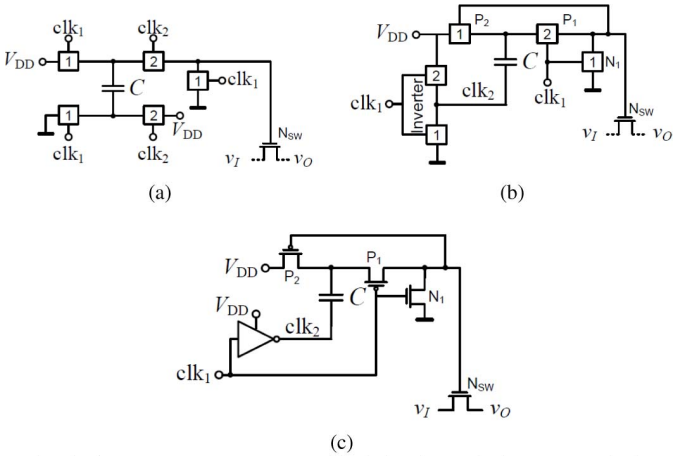


Fig. 5. CB. (a) Conventional high-level model. (b) Proposed high-level model. (c) Proposed transistor-level schematic.

x_i, w_i, and z_i (where i is equal to A or B, depending on the QLUT input) and their complements are applied to a combinational logic block synthesized exclusively by NAND gates. The combinational block is used to generate the one-hot coded output cs, which is finally employed to choose and turn on only one switch among the 16 available in the QLUT. The truth table for the logic function implemented in the combinational block is shown in Table I, together with the corresponding quaternary inputs Q_A and Q_B.

IV. Circuit Dimensioning and Simulation Results

A. Multiplexer 16-1

The switch to be used in the multiplexer, shown in Fig. 5, is dimensioned for an overall rise time of 1.5 ns, which is

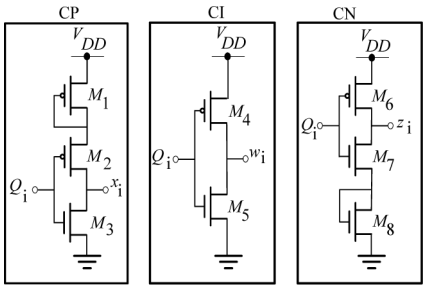


Fig. 6. Self-referenced comparators transistor-level schematic.

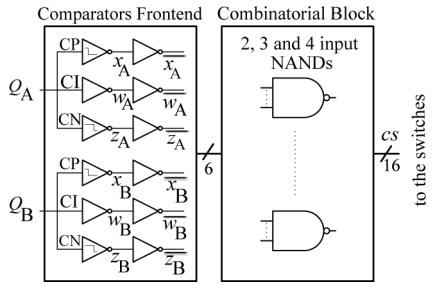


Fig. 7. Proposed quaternary-to-binary decoder high-level model.

15% of the clock period for a target frequency specification of 100 MHz. The CB circuit speed is most sensitive to two design parameters: the nMOS switch (N_{sw}) size and the CB capacitance (C). To achieve the imposed specification, a 15-μm wide and 120-nm long (the minimum possible L for UMC 130 nm) nMOS switch is used. The sizes for the other transistors inside the booster are not so critical, since they only affect the transient response at the circuit start-up. Once the booster capacitance is fully charged, the circuit reaches

TABLE I
COMBINATORIAL BLOCK LOGIC FUNCTIONS

$\mathbf{Q_A}$	$\mathbf{Q_B}$	$\mathbf{x_A}$	$\mathbf{w_A}$	$\overline{\mathbf{z_A}}$	$\mathbf{x_B}$	$\mathbf{w_B}$	$\overline{\mathbf{z_B}}$	*cs(activebit)*
0_4	0_4	1_2	1_2	1_2	1_2	1_2	1_2	$cs(1)$
1_4	0_4	0_2	1_2	1_2	1_2	1_2	1_2	$cs(2)$
2_4	0_4	0_2	0_2	1_2	1_2	1_2	1_2	$cs(3)$
3_4	0_4	0_2	0_2	0_2	1_2	1_2	1_2	$cs(4)$
0_4	1_4	1_2	1_2	1_2	0_2	1_2	1_2	$cs(5)$
1_4	1_4	0_2	1_2	1_2	0_2	1_2	1_2	$cs(6)$
2_4	1_4	0_2	0_2	1_2	0_2	1_2	1_2	$cs(7)$
3_4	1_4	0_2	0_2	0_2	0_2	1_2	1_2	$cs(8)$
0_4	2_4	1_2	1_2	1_2	0_2	0_2	1_2	$cs(9)$
1_4	2_4	0_2	1_2	1_2	0_2	0_2	1_2	$cs(10)$
2_4	2_4	0_2	0_2	1_2	0_2	0_2	1_2	$cs(11)$
3_4	2_4	0_2	0_2	0_2	0_2	0_2	1_2	$cs(12)$
0_4	3_4	1_2	1_2	1_2	0_2	0_2	0_2	$cs(13)$
1_4	3_4	0_2	1_2	1_2	0_2	0_2	0_2	$cs(14)$
2_4	3_4	0_2	0_2	1_2	0_2	0_2	0_2	$cs(15)$
3_4	3_4	0_2	0_2	0_2	0_2	0_2	0_2	$cs(16)$

steady state, and the only charge drawn from the supply is to compensate for the charge redistribution that occurs between the boosting capacitance and the switch capacitance. By employing transistors with minimum dimensions (width of 160 nm and length of 120 nm), the circuit reaches steady state after one clock cycle. Regarding the capacitor, it should be dominant facing the N_{sw} gate capacitance, avoiding a large voltage drop due to charge redistribution. Therefore, we have employed a capacitance value of 75 fF (2.53 μm $\times$ 2.53 μm) since it leads to an optimum value of voltage boost while trading off resistance reduction and long-term gate oxide stress. The switch has to be replicated 16 times, to implement the 16-1 multiplexer.

For a CMOS TG switch to fulfill the same requirements, the transistors have to be implemented with a width of 30 μm. As explained before, increasing the size of these transistors, increases the power needed to control them. Furthermore, this switch requires two control signals, which increases even more the power consumption and increases the size and complexity on the decoder. Both techniques were evaluated by designing the circuits for the same conditions, output rise time (1.5 ns), confirming that by employing the CB switch we have savings of 58% in power consumption and 27% in area.

The multiplexer is evaluated through a 500-run Monte Carlo and corners simulation using the Cadence software tool with parameters from UMC 130-nm technology libraries. The worst transition time observed in all these simulations is of 1.51 ns.

B. Quaternary-to-Binary Decoder

The reference point for each self-referenced comparator, as shown in Fig. 8, can be shifted toward the required levels by changing the transistors sizes.

The widths employed for each transistor are shown in Table II. All the transistors have minimum length (120 nm). The simulated transfer functions are shown in Fig. 9, where the obtained transition points for typical simulation are 328, 591, and 837 mV, with a 1.2 V power supply voltage. Afterward, a 500-run Monte Carlo simulation, using the UMC 130-nm foundry libraries, shows that the mean and standard deviation for the transition points x, w, and z are, respectively,

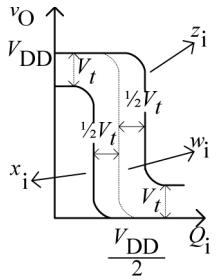


Fig. 8. First-order model transfer functions for the self-referenced comparators.

TABLE II
COMPARATORS FRONTEND TRANSISTOR DIMENSIONS (LENGTH 120 nm)

	Width
$\mathbf{M_1, M_2}$	400 nm
$\mathbf{M_4}$	700 nm
$\mathbf{M_6}$	1000 nm
$\mathbf{M_3, M_5, M_7, M_8}$	160 nm

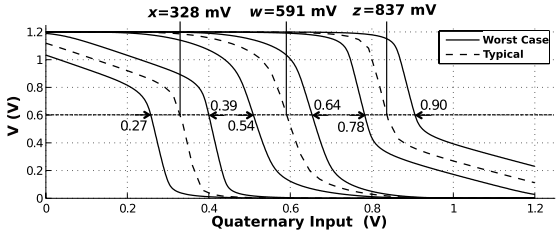


Fig. 9. Monte Carlo transfer functions results for the self-referenced comparators.

TABLE III
NAND GATES TRANSISTOR DIMENSIONS (LENGTH 120 nm)

Width	**PMOS**	**NMOS**
2 – inputNAND	580 nm	320 nm
3 – inputNAND	580 nm	480 nm
4 – inputNAND	580 nm	640 nm

TABLE IV
MEASURED DELAY FOR THE COMBINATIONAL BLOCK LOGIC FUNCTIONS

		Min.	**Avg.**	**Max.**
Monte Carlo	**Rise Time**	26.52 ps	57.16 ps	90.52 ps
	Fall Time	23.64 ps	56.57 ps	86.54 ps
Corners	**Rise Time**	50.06 ps	59.99 ps	74.60 ps
	Fall Time	49.27 ps	57.54 ps	68.96 ps

μ_x = 331 mV, σ_x = 25 mV, μ_w = 590 mV, σ_w= 20 mV, μ_z = 838 mV, and σ_z = 19 mV. Furthermore, based on these figures and in Fig. 9, we observe more than 130 mV of safety margin between the transition curves.

The combinational logic employs only NAND-gates with 2, 3, or 4 inputs. Each function represented on a line of the Table I is synthesized using NAND gates combining the comparator frontend outputs and their complements. The NAND gates transistors sizes are shown in Table III. This combinational block is tested for functionality and timing. In Table IV, we show the simulation results for a 500-run Monte Carlo and corners simulation.

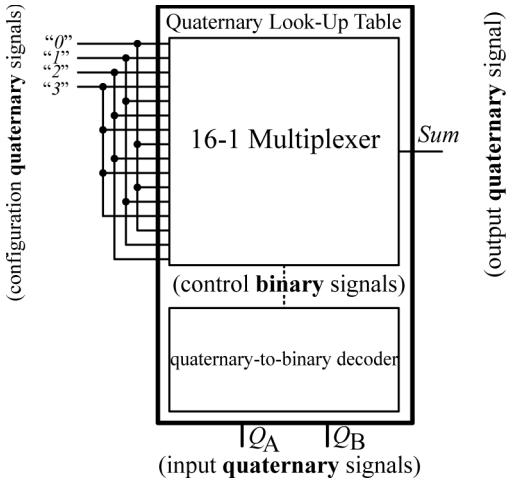


Fig. 10. QLUT half adder high level configuration.

TABLE V
HALF ADDER LOGIC FUNCTION

$\mathbf{Q}_A$	0_4	0_4	0_4	0_4	1_4	1_4	1_4	1_4	2_4	2_4	2_4	2_4	3_4	3_4	3_4	3_4
$\mathbf{Q}_B$	0_4	1_4	2_4	3_4	0_4	1_4	2_4	3_4	0_4	1_4	2_4	3_4	0_4	1_4	2_4	3_4
Sum	0_4	1_4	2_4	3_4	1_4	2_4	3_4	0_4	2_4	3_4	0_4	1_4	3_4	0_4	1_4	2_4

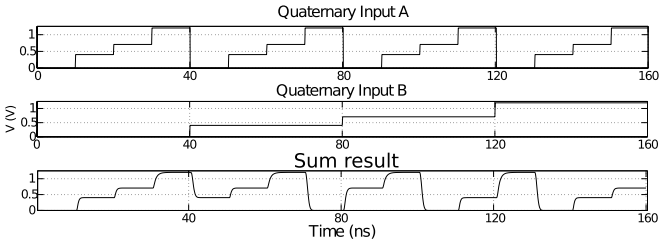


Fig. 11. QLUT half adder simulation results when applied to an output load of 10 pF.

C. QLUT Working as a Half Adder

The QLUT can be configured to implement a half adder using the circuit schematic shown in Fig. 10, with the configuration inputs that results in the outputs summarized in Table V. The typical simulation of this circuit lead to the results shown in Fig. 11, attesting the feasibility of its implementation. The circuit is then evaluated for process and mismatch variations, through a 500-run Monte Carlo simulation and also for corners. The worst case transition time remained at 1.51 ns, confirming that the decoder did not degrade the speed of the multiplexer switches. Additionally, Lazzari *et al.* [9] have presented simulation results for two QLUT circuits with similar functionality, one being binary, consuming 45 μW and one quaternary, consuming 35 μW, for an output applied to a capacitive load of 0.2 pF. In addition, when applied to a load of 2 pf, those circuits were limited to a maximum frequency of 100 MHz. The proposed half-adder implementation has about the same power consumption (34.7 μW), however, it is able to deal with loads up to 10 pF running at 100 MHz.

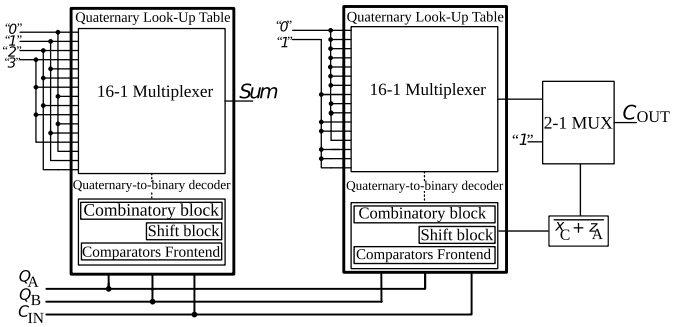


Fig. 12. QLUT full adder high level configuration.

TABLE VI
FULL ADDER LOGIC FUNCTION

$\mathbf{Q}_A$	$\mathbf{Q}_B$	C_{IN}	*Sum*	C_{OUT}	$\mathbf{Q}_A$	$\mathbf{Q}_B$	C_{IN}	*Sum*	C_{OUT}
0_4	0_4	0_4	0_4	0_4	0_4	0_4	1_4	1_4	0_4
0_4	1_4	0_4	1_4	0_4	0_4	1_4	1_4	2_4	0_4
0_4	2_4	0_4	2_4	0_4	0_4	2_4	1_4	3_4	0_4
0_4	3_4	0_4	3_4	0_4	0_4	3_4	1_4	0_4	1_4
1_4	0_4	0_4	1_4	0_4	1_4	0_4	1_4	2_4	0_4
1_4	1_4	0_4	2_4	0_4	1_4	1_4	1_4	3_4	0_4
1_4	2_4	0_4	3_4	0_4	1_4	2_4	1_4	0_4	1_4
1_4	3_4	0_4	0_4	1_4	1_4	3_4	1_4	1_4	1_4
2_4	0_4	0_4	2_4	0_4	2_4	0_4	1_4	3_4	0_4
2_4	1_4	0_4	3_4	0_4	2_4	1_4	1_4	0_4	1_4
2_4	2_4	0_4	0_4	1_4	2_4	2_4	1_4	1_4	1_4
2_4	3_4	0_4	1_4	1_4	2_4	3_4	1_4	2_4	1_4
3_4	0_4	0_4	3_4	0_4	3_4	0_4	1_4	0_4	1_4
3_4	1_4	0_4	0_4	1_4	3_4	1_4	1_4	1_4	1_4
3_4	2_4	0_4	1_4	1_4	3_4	2_4	1_4	2_4	1_4
3_4	3_4	0_4	2_4	1_4	3_4	3_4	1_4	3_4	1_4

V. FULL ADDER CIRCUIT

In this section, we employ the proposed QLUT to implement a full adder. The conventional and direct approach would require four QLUTs to properly implement this function, two QLUTs for each output, sum and carry out, working with the two possible values of the carry in. However, we propose minor modifications to the designed QLUT, which allows the reduction of the number of QLUTs only to two. This is achieved at the cost of a slight increase in binary combinational logic and a 2-1 multiplexer, as shown in Fig. 12. These modifications do not affect the original reconfigurability and functionality of the circuit as a regular QLUT.

A. QLUT With Shift

Table VI shows the full adder truth table. It may be inferred that the results for the Sum and C_{OUT} signals may be easily obtained through logic shifts on the inputs. The shift block is implemented for one of the inputs and performs a single up-shift on the input quaternary value. Using the two QLUTs configured with the results when C_{IN} is 0, as shown in Table VI, it is observed that the result with C_{IN} 1 can be obtained, for the Sum, by up shifting one level on Q_B. For C_{OUT}, the same reasoning can be performed leading to an up shift of one level on the variable Q_A, which corresponds to a shift of four levels on the C_{OUT} output, with exception when Q_A has the level 3, which is handled by combining the y_C and z_A (which are 0 when C_{IN} has the level 1 and Q_A has the level 3) on a NOR to control the 2-1 multiplexer.

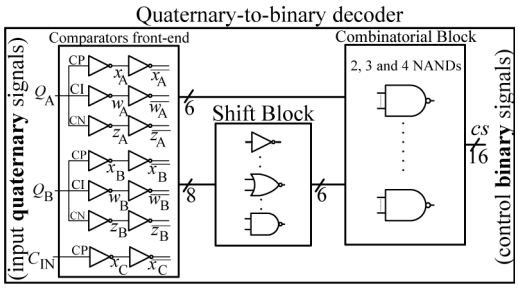
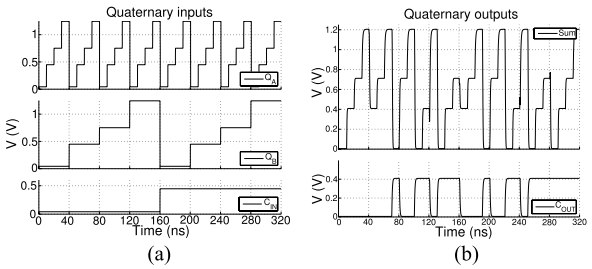


Fig. 13. Quaternary-to-binary decoder with shift high-level model.

TABLE VII
QLUT TIMING SIMULATION RESULTS WHILE APPLIED TO AN OUTPUT LOAD OF 10 pF

Transition time	QLUT w/ shift	QLUT w/o shift
Min.	0.70 ns	0.70 ns
Avg.	1.06 ns	1.00 ns
Max.	1.57 ns	1.51 ns



(a) (b)

Fig. 14. QLUT full adder simulation results while applied to an output load of 10 pF. (a) Input signals. (b) Output signal.

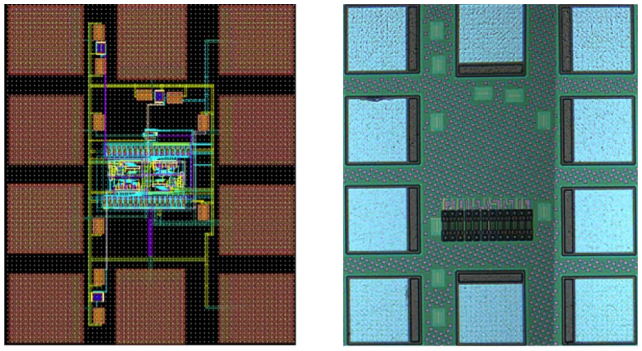
This block is implemented with two 2-input NAND gates, four inverters and two 2-input NOR gates.

The required logic to perform the shifts and to decode the C_{IN} is added to the QLUT. These blocks are implemented keeping area and energy consumption as low as possible while satisfying the delay constraints. Moreover, to convert the quaternary variable C_{IN} into binary, we added a comparator CP and an inverter to the comparators frontend, as shown in Fig. 13. This extra block represented an increase of 5% on the QLUT area.

This decoder replaces the previous designed one and this new QLUT is simulated for timing analysis. The worst time for the transitions is shown, for both QLUTs, in Table VII, to observe that this small modification had small effect on the overall circuit functionality. The power consumption for this modified QLUT is 36.5 μW, which reveals an overhead of 5.2% in power consumption, when compared with the nonmodified QLUT.

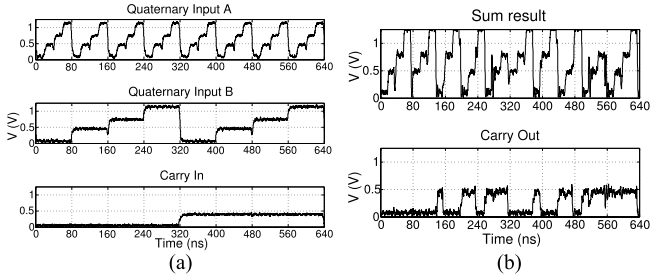
B. Full Adder Simulation and Layout

Simulations show that the average power consumption is 87.5 μW for random-generated quaternary input signals vectors at 100 MHz. The results shown in Fig. 14 confirm that this approach, with minimal modifications in the QLUT design, is feasible with advantages on power consumption. This implementation saves power consumption when compared



(a) (b)

Fig. 15. Full adder. (a) Circuit layout. (b) Die photograph.



(a) (b)

Fig. 16. QLUT full adder low frequency experimental results while applied to an output load of 10 pF and observed with a probe of 2 pF. (a) Input and (b) output signals.

with the commonly used with four QLUTs, which consumes, at least 138.8 μW (4 $\times$ 34.7 μW) and would have a larger area occupation.

The proposed layout was designed in a 130-nm CMOS technology, shown in Fig. 15(a). The main concern is the active area of the QLUT, since the main purpose of this module is to be replicated several times on an FPGA. The obtained active area for the full adder prototype is of 108 μm $\times$ 99 μm. Fig. 15(b) shows a microphotograph of the fabricated circuit under evaluation.

VI. EXPERIMENTAL RESULTS

A. Test Bench Development

The designed prototype is wire bonded directly on a test printed circuit board (PCB). This test board was developed to provide the supply voltage (1.2 V), the reference voltages (1.2, 0.71, and 0.44 V) and the three quaternary input signals (Q_A, Q_B, and C_{IN}) required for testing.

B. Test at 50 MHz

To generate the quaternary reference voltages we used variable resistors adjusted to fit the required values. For a preliminary test, custom high frequency digital signals were generated by an FPGA, which makes it easy to change them simply by programming. These signals, although binary, were applied to a simple resistor digital-to-analog converter to generate the custom quaternary levels. This methodology allowed to perform a test at a lower frequency, 50 MHz (symbol period of 20 ns), showing the correct circuit functionality, as shown in Fig. 16. However, this methodology did not allow a test at

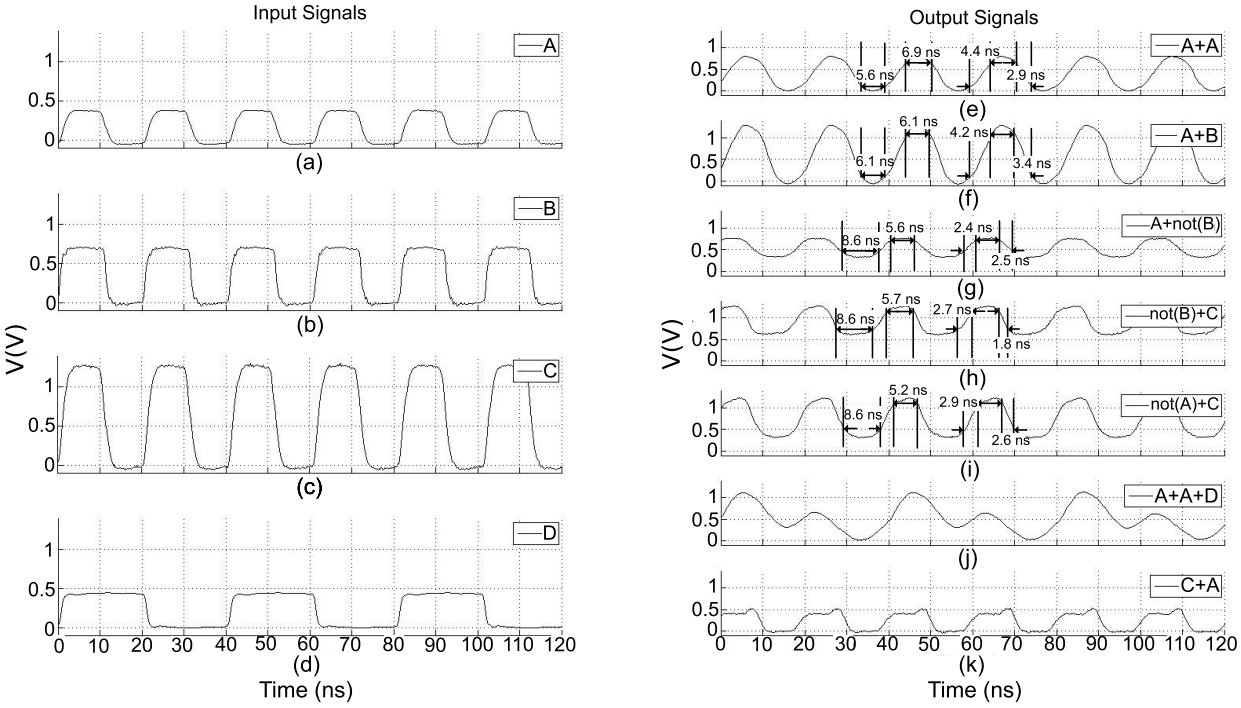


Fig. 17. QLUT full adder experimental test signals for an output load of 10 pF and observed with a capacitive probe of 2 pF. (a)–(d) Set of input signals. (e)–(j) Sum output signals. (k) Carry output signal.

TABLE VIII
FULL-ADDER POWER MEASUREMENT WITH AN OUTPUT LOAD OF 10 pF AND USING THE TEST RESULT SHOWN IN FIG. 17(f)

Power	Simulation	Experimental
on V_{DD}	144 μW	140 μW
on V_{REF3}	564 μW	588 μW
on V_{REF2}	109 μW	139 μW
on V_{REF1}	0.6 μW	10 μW

TABLE IX
FULL-ADDER POWER MEASUREMENT WITH AN OUTPUT LOAD OF 10 pF AND USING THE TEST RESULT SHOWN IN FIG. 17(j)

Power	Simulation	Experimental
on V_{DD}	114 μW	122 μW
on V_{REF3}	333 μW	373 μW
on V_{REF2}	57 μW	64 μW
on V_{REF1}	6 μW	11 μW

higher frequencies. Hence, all the signals were generated using FPGA I/O ports, which have a limited current supply. These custom high frequency digital signals are binary valued. Therefore, we applied them to a resistor network to produce the custom quaternary inputs. All these components increase the noise on the signals, its transition times and the power consumption measurements. Therefore, a new test setup is devised to perform a test at higher frequencies and to obtain more accurate power consumption measurements.

C. Test at 100 MHz

To test the circuit at higher frequencies, we used two pulse generators (HP 8130A and HP 8131A), which are able to provide high frequency square signals with custom high and low levels and with very small rise and fall times (approximately 100 ps), applied directly at the inputs of the QLUT. Then, several tests are performed with a set of different input vectors, as shown in Fig. 17, to attest the circuit functionality at higher frequencies.

To observe the input and output signals, we had to employ a probe (TEK P6205) with 2-pF capacitance, raising the output load, which finally leads to an increase in the rise and fall times. For the power consumption, we have no means of measuring, separately, the short-circuit power and the power required to activate the next logic gate. Therefore, we have removed the probe from the circuit, and measured the average power consumption for two different situations, to obtain a fair approximation of its values. To test the circuit we have chosen the set of input signals, shown in Fig. 17(a)–(d). The first three signals [(a)–(c)] have the same frequency (50 MHz) and different amplitudes: 0.44, 0.71, and 1.2 V, respectively, representing the different quaternary logic levels (1_4, 2_4, and 3_4). The fourth signal (d) has the frequency of 25 MHz with an amplitude of 0.44 V (logic level 1_4). Applying three of these signals directly or switching their phases (by 180°, presented as the negation of the correspondent signal) to the QLUT quaternary inputs, we can obtain different behaviors on the outputs. The signals are combined to obtain three output setups as follows.

1) Fig. 17(e)–(i) shows the results for the Sum, showing this output transitions between the two quaternary logic levels, with the correspondent timing analysis.
2) Fig. 17(j) shows also the Sum result, with an average and more common situation, where we have transitions between the four logic levels.

TABLE X
COMPARISON WITH STATE-OF-THE-ART LUTS

	Quaternary				Binary		
	This work	**[13]**	**[14]†**	**[8]†**	**[9]†**	**[14]†**	**[8]†**
Number of Inputs	2	2	2	2	4	5	4
Technology node	UMC 130 nm	UMC 130 nm	TSMC 180 nm	TSMC 180 nm	UMC 130 nm	TSMC 180 nm	TSMC 180 nm
Technique	Standard CMOS	Standard CMOS	3 Different V_{th}	3 Different V_{th}	Standard CMOS	Standard CMOS	Standard CMOS
Supply Voltages	1.2 V	1.2 V	3 V	1.8 V	1.2 V	3 V	1.8 V
Frequency	100 MHz	100 MHz	1 GHz	500 MHz	100 MHz	1 GHz	500 MHz
Rise/Fall Time	4.4 ns (1.5 ns†)	5 ns	0.69 ns	0.50 ns	3 ns	1.07 ns	0.15 ns
Output Load	10 pF	4 pF	2.5 fF⋆	2.5 fF⋆	1.0 pF	2.5 fF⋆	2.5 fF⋆
Transistor Count	220	112	120	84	68	236	136
Power Consumption	140 μW	126 μW	134 μW	155 μW	94 μW	450 μW	289 μW

[†] Simulation results only [⋆] Aproximate value for the input capacitance of a binary inverter with L=0.18μm and W=0.81μm

3) Fig. 17(k) shows the worst case result for carry out signal.

The rise and fall times for each different situation are also shown, measured at 10% and 90% of the signal amplitude range. The worst case transition is the one from 0_4 to 3_4, with values of 4.4 and 3.4 ns for the rise time and for the fall time, respectively. These values are larger than in simulation. However, in this test setup, we have to consider the pad, bonding wire, PCB wire and probe, which will degrade the performance of the real signal applied to the circuit. In addition, as said previously, due to all the existing parasitic, the measurement is performed using a load larger (>10 pF) than the considered for sizing.

Power measurements are performed for two different situations. For the worst case transition (0_4 to 3_4), represented in Fig. 17(f), with the obtained results shown in Table VIII, and for the more realistic situation shown in Fig. 17(j) leading to the results shown in Table IX.

With the performed tests, we confirm that the circuit is able to work at 100 MHz, while charging a load of 10 pF, proving that this circuit is suited for an FPGA application. The performed power measurements are in agreement with the simulations, confirming the circuit functionality and the low power consumption of this circuit.

The use of these techniques allowed for our circuit to be competitive with the binary counterpart and to be advantageous when compared with previous multiple-valued proposed circuits, as we can observe in Table X. For this table, we considered only the generic 2-input QLUT operation, disregarding our extra full adder functionality. The most similar work, was previously proposed by us in [13], where the topology shown in Fig. 4(a) was used. Our current work has similar results in terms of power consumption; however, it is able to deal with 2.5 times the load. This ability comes at the price of using more transistors (twice as many), being the majority of them of very small dimensions. When compared with the other quaternary proposed works [8], [14], which rely on different voltage threshold transistors, demanding more process steps, our operation frequency is lower, our transistor count is higher and our power consumption is on the same order of magnitude. However, our circuit is able to deal with a load 4000 times higher, which has a direct impact on the design of the circuit and in the previous figures. Moreover, the solutions we compare with would require a buffer when used in an FPGA, which will increase their area and power consumption.

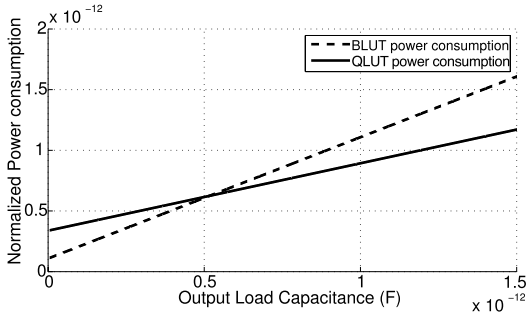


Fig. 18. Power consumption versus output load capacitance.

The same conclusions can be drawn from the comparison of the binary versions of the works in [8] and [14], with the noticeable difference of a lower power consumption. Since the binary work presented in [9] is very similar to our quaternary approach, we present a more in-depth analysis. To ease the comparison, we used some approximations and simplifications, allowing us to evaluate at which output load capacitance value is it advantageous to use our quaternary implementation. To this end, we analyze power consumption in terms of the dynamic power on the load and on the logic.

The dynamic power on the load is estimated by (1) for binary logic and by (2) for quaternary logic. Assuming that the quaternary logic levels have equal probability of occurrence, the V_{av} in (2), will be equal to $5/9V_{\text{DD}}$. For the same output load, we obtain savings in the order of 45% for the dynamic power consumption when compared to the binary logic.

The dynamic power on the logic, since both circuits work internally with binary, is estimated by the equation $P_D \propto nC_gV_{\text{DD}}^2a$, where n is the number of used transistors, C_g is the gate capacitance and a the activity factor. We have considered the same activity factor, since we cannot evaluate it directly. Assuming the same frequency of operation, the same supply voltage and similar gate capacitances we plotted a normalized power consumption in function of the output load capacitance, in Fig. 18. From this figure, we can conclude that when the output load reaches around 0.5 pF our quaternary

LUT implementation becomes more power efficient than the binary LUT. Note that, we are disregarding the effects of the output load in the logic, since the used switches to charge this load have to increase as the load increases. However, this would have similar effect on both cases. Furthermore, we are under evaluating our case, since we are only using one switch with CB versus the two used for the CMOS TG, and we have shown in Section IV-A that our switch is advantageous.

VII. Conclusion

In this paper, we have reported an innovative QLUT design that can be used for multiple valued combinational logic or as a building block in FPGAs. The QLUT internal functionality is implemented using simple standard CMOS structures. This feature is achieved through a quaternary-to-binary decoder that quantize the input signals. This decoder is based on voltage-mode self-referenced comparators that allows the use of a standard CMOS technology and overcomes previous design drawbacks. Also, a CB technique was used to decrease the switches resistance and increase the operation frequency, while at the same time, achieving low power consumption. Therefore, the presented design is a valid solution to reduce the interconnections impact, without increasing power consumption or losing performance. Experimental results were performed on an ASIC implementation of a full adder employing the designed QLUT. The obtained results attested the circuit feasibility and its advantages, using a standard CMOS process and its main characteristics (timing and power).

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