Design and Characterization of a QLUT in a Standard CMOS Process

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***Abstract*— Interconnect has become preponderant in many aspects of circuit design, namely delay, power and area. This effect is particularly true for FPGAs, where interconnect is often the most limiting factor. Quaternary logic offers a means to reduce interconnect since each circuit wire can, in principle, carry the same information as two binary wires. We have proposed in [1] a design implementing a quaternary low-power high-speed look-up table. The main features of this circuit are being based on a voltage-mode structure and using only standard CMOS technology. In this paper we present the design of a prototype implementation and experimental results. These results are discussed and conclusions are drawn that provide further guidelines for improvement.**

I. Introduction

The importance of interconnect in VLSI circuits increases with each new technology node [2]. As transistors shrink with technology, their weight in defining the main circuit characteristics, namely, area, delay or power, reduces in relative terms to interconnect. Moreover, higher integration allows for circuits with a larger number of active elements, increasing the complexity of the required interconnect, both in number and length of wires.

Multiple-valued logic (MVL) has been proposed in the past as a means to reduce the number of wires in a circuit [3]–[5]. In theory, a wire carrying a signal with N logic levels can replace $\log_2 N$ wires carrying binary signals. Hence, the required number of wires may be significantly reduced. In turn, less wiring allows for a more packed layout, reducing the average interconnect length. Besides the immediate area gains, this compounded effect leads to less switched capacitance, with benefits in delay and power consumption.

Field Programmable Gate Arrays (FPGAs) are a class of circuits where interconnect plays a particularly important role [5]. In many cases, the capacity of the programmable circuit can not be exploited to the full extent because many functional cells are simply prevented from being used due to the interconnect. In previous work [1] we have addressed this type of circuits by proposing an innovative implementation of a multiple-valued look-up table based on quaternary representation. This design presents two main advantages over previous solutions. One is that it is based on voltage-mode devices, hence much more power efficient than its current-mode counterparts. The second is that it uses in each class, P and N, transistors with a single threshold voltage V_{th}, thus avoiding the extra steps in the fabrication process for the generation of transistors with different V_{th}s.

We have designed and characterized the cell we have proposed in [1]. In this paper, we describe the options taken for its design, present the experimental set up used for its characterization and discuss the results obtained. These results are very much in line with the simulation results presented in [1], confirming the expected good performance of the cell. In this evaluation process we did find some limitations, and we present a discussion on how this can be addressed with some design modifications.

This paper is organized as follows. Section II makes a brief summary of the cell design we proposed in [1]. In Section III we describe the cell design and experimental set up. The results obtained are presented in Section IV. A discussion on possible improvements to the circuit is given in Section V and Section VI presents some conclusions.

II. Voltage-mode Quaternary Look-up Table

A quaternary look-up table (QLUT) implemented with transmission gates controlled by a new quaternary to binary device was proposed in [1], as depicted in Fig. 1.

Fig. 1 shows a 2-input QLUT with 16 configuration levels, $c_0, \ldots, c_{15}$, selected through only two stages of transmission gates. A special circuit, the quaternary-to-binary converter (Q-decoder), is used to convert the quaternary inputs y_0 and y_1 to the binary signals that control the transmission gates.

The Q-decoder is detailed in Fig. 2. This circuit converts a quaternary input to a 4-bit word in one-hot encoding, and its inverted value. The outputs Q_0 to Q_3 determine which transmission gate will propagate the configuration value $c_i \in C$ to the QLUT output w. Note that values for the controlling signals Q_0, Q_1, Q_2 and Q_3 are binary values, assuming either 0 (0 V) or 1_2 (V_{DD}).

The main advantage of this structure over previous proposed implementations is that it is based solely on standard CMOS structures. The Q-decoder is composed of two comparators *CP* and *CN* which are self-reference analog comparators (Fig. 3(a) and 3(b)), and other conventional digital CMOS circuits such as inverters, NANDs and NORs. This Q-decoder determines the input quaternary value by comparison in three comparators having self-reference voltages, at $1/6V_{DD}$, $3/6V_{DD}$ and $5/6V_{DD}$, respectively.

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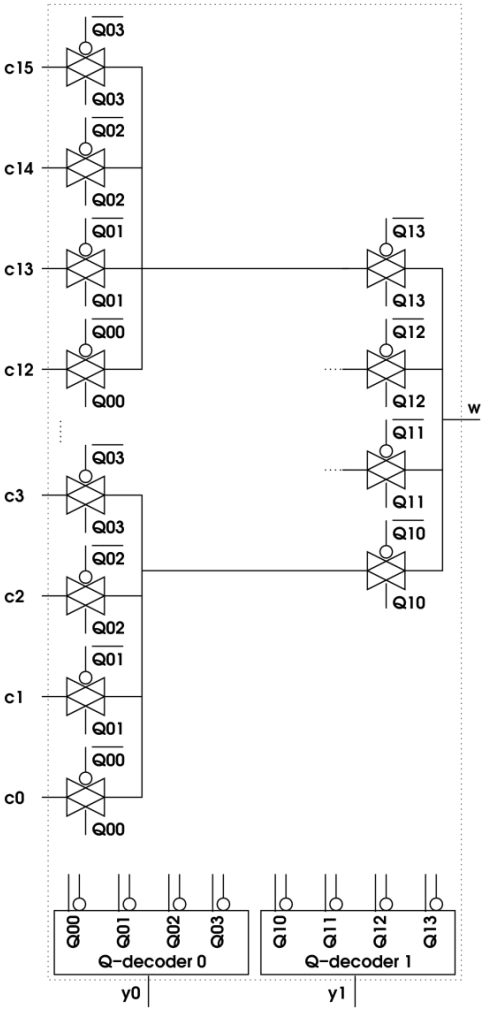


Fig. 1. Quaternary look-up table implementation.

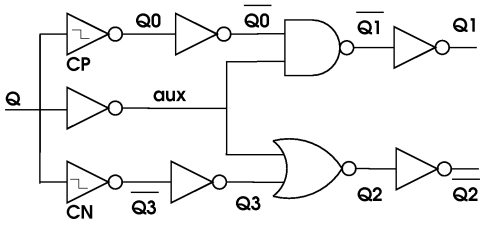
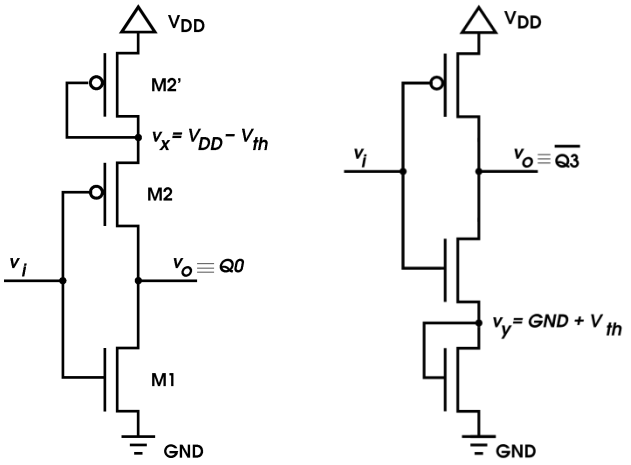


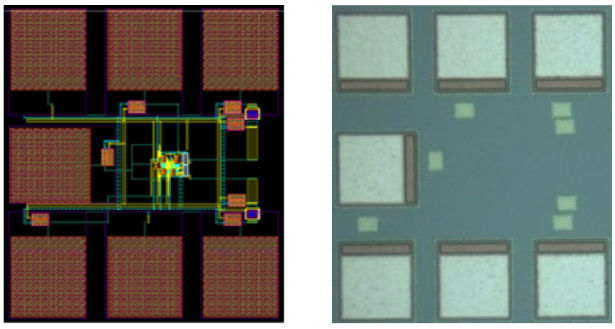
Fig. 2. Q-decoder.

The Q-decoder was implemented with the UMC 130 nm CMOS technology and simulated for process variability and reduced noise margin. This is due to the reduced voltage levels to represent quaternary logic values in comparison to binary circuits, and for this reason they may be, in theory, more susceptible to errors. Monte Carlo simulation with 500 runs shown that our quaternary LUT is robust to process variations when considering random process and mismatch variations. The circuit is able to work at 100 MHz with a load capacitance up to 1 pF.



(a) (b)

Fig. 3. Comparator circuits: (a) CP and (b) CN.



(a) (b)

Fig. 4. (a) Layout and (b) die photograph.

III. Circuit and Test Bench Implementation

To validate the circuit proposed a layout is designed in UMC 130 nm (Fig. 4(a)). The main concern was the die area of the QLUT, once the purpose of this circuit is to be replicated several times on an FPGA. The die area of the QLUT is 37×32 μm^2. On Fig. 4(b) is a picture of the fabricated circuit under evaluation.

The designed QLUT is wire bonded directly on a dual in-line package (DIL). To test it, a test bench (Fig. 6) is developed to provide the supply voltage (1.2 V), the reference voltages (1.2, 0.707 and 0.404 V) and the quaternary input signals.

All these signals are generated on an FPGA, with some added resistor elements. The quaternary reference voltages are obtained, using variable resistors that can be adjusted to obtain the correct values. The custom high frequency digital signals are generated directly from the FPGA making it easy to change them simply by programming. The FPGA outputs are binary valued, therefore we applied them to a resistor network to produce the custom quaternary inputs suited for the test.

This test bench has several limitations that prevent the test of the circuit in the conditions of the simulations carried out in [1]. The FPGA driving capability is limited, furthermore, at 100 MHz the digital output signal exhibit ringing at the output pin connector when measured with a probe (Tek P6205) representing a load of 2 pF (C_{load}) in parallel with 1 MΩ (R_{load}).

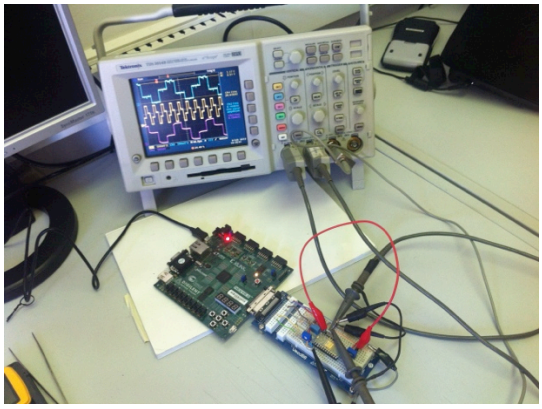


Fig. 5. Testbench overview.

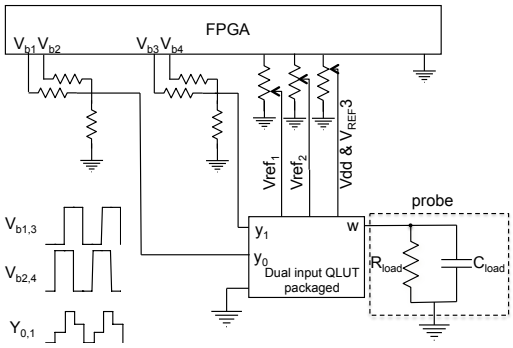


Fig. 6. Test bench illustration.

The ringing cause glitches on the comparators of the Q-decoder, originating undesired switchings, increasing power consumption and making it difficult to evaluate the output result. To make the circuit validation possible we have evaluated experimentally the circuit at a lower frequency. Then we modeled the experimental test bench in the simulator for validation under the same conditions.

It is considered electrical models for the bonding wires, package, breadboard and the active probe.

The bonding is modeled by an inductance 1 nH/1 mm with a small series resistance and a capacitance to ground. For the package it is used a dual in-line package (DIL) model that comprises also resistances, capacitances, inductances and the coupling between lines. For the breadboard we have just considered an estimated 4 pF capacitance followed by the load from due to the probe. Finally, being the power consumption estimation strongly dependent on the rise and fall time of the output signals, they are measured (5 ns) and replicated on the test signals used for simulation.

IV. Experimental Results

Using the test bench described above, we are able to test the circuit at 25 MHz (40 ns in each quaternary level), obtained through the combination of two quaternary signals, y_0@6.25 MHz and y_1@3.125 MHz. The input and output signals are represented in Fig. 7 from the experimental test setup and on Fig. 8 from the simulation test bench.

Fig. 7. Experimental results.

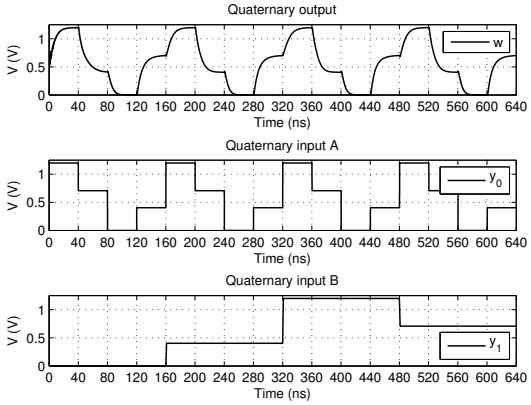


Fig. 8. Simulation results.

These experimental and simulation results match, proving that the proposed QLUT design is feasible, having the output voltage levels well defined. It also indicates, by observing the *RC* charge/discharge behavior (Fig. 7 and 8), that the models used are close to what we have present on the experimental test, and that without the test bench load the circuit would operate at 100 MHz as expected (this would be the real condition inside an FPGA).

In simulation the circuit works at 100 MHz just by removing the probe load. Therefore we tested the circuit at 100 MHz, without probe to measure the current consumption.

The results for the power consumption for both simulation and experimental measurements, on V_{DD} powering the QLUT and the input reference level of 1.2 V, are presented in Table I. There we can observe that the power consumption increases with the load capacitance and the rise time, as expected. Comparing the simulation results with the experimental result we confirm they are of the same order of magnitude, which is also a good indicator that the circuit and the power estimations are in agreement.

Experimental results could be improved if a higher capacitance has been consider as a load or if on-chip probing, having less capacitance, could be performed.

TABLE I

POWER CONSUMPTION SIMULATION RESULTS IN μW AT 100 MHz.

	T_r = 1 ns	T_r = 5 ns
QLUT	35.6	37.5
w/ Package	42.0	44. 3
w/ Package & Breadboard	81.4	91.1
Experimental	Not tested	126.0

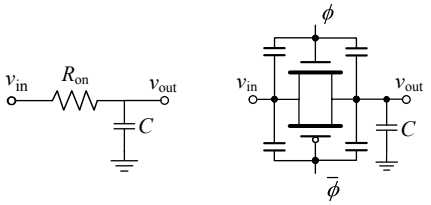


Fig. 9. LUT line equivalent model.

V. ANALYSIS AND CRITIQUE

The results show that the binary to quaternary circuit is feasible and efficient in terms of power consumption while being implemented in a standard CMOS technology with a single type of NMOS and PMOS transistors and a single supply voltage.

The LUT dynamic behavior can be studied in terms of a simple *RC* circuit and the power consumption can be studied in terms of the energy necessary to charge and discharge capacitances. A simple *RC* model is represented in Fig. 9 where *R* represents the switch ON resistance and *C* represents the interconnection load capacitance. The transition time can be obtained from (1) which can be simplified by saying that the transition time is approximately proportional to *RC*.

$$v_{\text{out}} = v_{\text{in}}\left(1 - e^{\frac{-t}{RC}}\right) \tag{1}$$

Relative to power consumption there are two main contributors: the energy required to charge the load capacitor, and the energy necessary to turn the switch ON and OFF (Fig. 9 with a transmission gate).

For the implementation of the LUT in an FPGA context, the load capacitance can be in the order of 10 pF. Being *C* an imposed variable it will require a smaller equivalent resistance for the transmission gate, in order to maintain the wanted operating frequency.

An NMOS transistor in the triode region has a resistance given by (2), where the resistance is inversely proportional to the transistor width, while the capacitance is directly proportional to the transistor area, $W \times L$.

$$r_{\text{ds}} = \frac{1}{2\mu_{\text{n}} C_{\text{ox}} \frac{W}{L}(V_{\text{GS}} - V_{\text{th}})} \tag{2}$$

The low resistance of a transmission gate (NMOS and PMOS transistors) require large transistors, while to reduce the power required to control them requires small transistors.

Therefore the tradeoff is to minimize *R* as much as possible without having to increase the capacitances, and this leads to the following line of reasoning:

- use of transistors with minimal *L*;

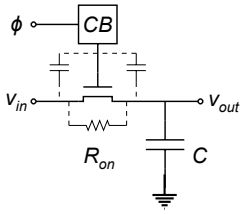


Fig. 10. Single NMOS switch with clock boosting.

- substitute the transmission gate by a single NMOS transistor with clock boosting techniques as illustrated on Fig. 10; it still allows full swing operation and further reduce the *R* due to the increase in V_{GS}. It will also reduce the capacitances because NMOS have lower capacitance than PMOS transistors for the same resistance ($\mu_{\text{n}} > \mu_{\text{p}}$ in 130 nm technology node).
- use of a decoder to reduce the number of switches in the signal path;

It is expected that these techniques lead to a high performance circuit, fast and with low power consumption.

Following these guidelines, a new switch to be used in the QLUT is currently under development. Preliminary results indicate that this implementation saves 5% in consumption and 25% in area, confirming that this solution is feasible with advantages for its use on LUTs. In addiction a decoder will be developed to further reduce consumption.

VI. CONCLUSION

In this paper we have reported the design and the experimental results we have performed on an actual ASIC implementation of an innovative quaternary look-up table design. The results attest for the feasibility and favorable characteristics of the design. We also present a discussion on the limitations of the current circuit and indicate avenues for its improvement. Being currently working on a new version of this design.

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