Variation-Aware, Library Compatible Delay Modeling Strategy

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***Abstract*— Variability in digital integrated circuits makes timing verification an increasingly challenging task. Statistical static timing analysis has been proposed as a solution to this problem, but most of the work has concentrated in the development of timing engines for computing delay propagation. Such tools rely on the availability of delay formulas accounting for both cell and interconnect delay. In this paper, we concentrate on the impact of interconnect on delay and propose an extension to the standard modeling strategies that is variation-aware and compatible with such statistical engines. Our approach, based on a specific type of perturbation analysis, allows for the analytical computation of the quantities needed for statistical delay propagation. We also show how perturbation analysis can be performed when only the standard delay table lookup models are available for the standard cells. Results from applying our proposed modeling strategy to computing delays and slews in several instances accurately match similar results obtained using electrical level simulation.**

I. Introduction

The impact of process variation on circuit performance is an area of increasing concern, both in the semiconductor industry, as well as academic research. Work around statistical static timing analysis of [1], [2] is a well-known example from the research community. Nowadays, designers spend a considerable amount of their verification budget trying to make sure that their circuits will work under all possible settings. To achieve this, they target the worst possible scenarios by considering so-called pessimistic conditions, and design in order to ensure that such corner cases are accounted for. This analysis is usually based on assuming worst-case conditions on all possible variations simultaneously. Such an scenario is pessimistic and may lead to considerable over-design.

Improving this situation requires tools that are better suited to handle realistic variations and the complex inter-relations that exist between those variations. Not only should those tools directly make use of realistic process information, thus making them better suited to model the unpredictability of process parameter variations, but they should be able to implicitly determine how such variations affect the circuit behavior. Such a formulation makes it possible to compute on a single analysis the circuit behavior not only due to a given parameter setting, but to a variety of settings. The recent development [1] of statistical timers that are based on a parametric description of delay in terms of random process variables is an example of movement in this direction.

A timing analyzer consists of several component pieces. In a statistical context, the most well-studied part of the timing engine is the timing graph traversal, which manages the calculation of arrival times and slews at the level of abstraction of a timing graph. An equally important, if more mundane, component is the delay calculation engine. The delay calculator takes as input the cell and interconnect models and produces a delay expression in a form that can be consumed by the graph engine. This paper is concerned with a portion of the delay calculation step, the impact of interconnect on delay. We explore how commonly used interconnect modeling strategies can be extended to be compatible with the most recent generation of statistical timing analysis tools [1]. Specifically, we desire to produce cell and interconnect delay as affine functions of process parameters. We assume that one of several recently proposed approaches for interconnect reduction under process variation is available to generate tractably sized reduced order models [3], [4], [5]. The key technology in our approach is a specific type of perturbation analysis. While digital circuits are strongly nonlinear with respect to the circuit inputs, cell delays are often close to linear *with respect to process parameters*. In this paper we adapt the general development of *linear time-varying* (LTV) perturbation theory [6] for extraction of variation-aware delay models to the specific needs of delay calculation for precharacterized standard cells. The advantage of this type of approach over, for example, differencing repeated delay calculation runs is that it is essentialy an analytic method. Differencing type approaches can suffer from severe robustness problems that make them difficult to use reliably. In addition, our technique can potentially be made very fast, handling parametric models with ten to twenty parameters at minimal penalty relative to a non-variational calculation.

The outline of this paper is as follows: in Section II, we review the basics of delay computation, including cell and interconnect delay, assuming no variations are taken into account. Then, in Section III, we introduce the general perturbation formulation and discuss the specific specialization of the more general technique to cell-level interconnect-related delay. We also discuss how perturbation analysis can be performed when only delay table lookup models are available for the standard cells. A key point is that *analytic* expressions for delay sensitivities can be obtained without having to have closed-form expressions for the cell delay elements (however, see [7] for such closed-form expressions). Results of using our proposed approach are shown in Section V and conclusions are drawn in Section VI.

II. Background

Timing verification is an enabling methodology for optimizing performance and making sure that circuits satisfy certain timing and frequency requirements. To that end, timing verifiers determine approximate but safe estimates of the worst-case delay through a circuit: for every input and output signal, there are many possible paths through the circuit, each path consisting of a set of interconnected network cells. Timing verification deals with the identification and analysis of the critical paths, also known as the longest delay paths in the circuit. In addition to finding critical-path delays, timing verifiers can also be used to do miscellaneous static analysis, like finding high-speed components off the critical path that can be slowed down to save power and several other relevant tasks. However, the most common usage is indeed to determine the worst case paths in a

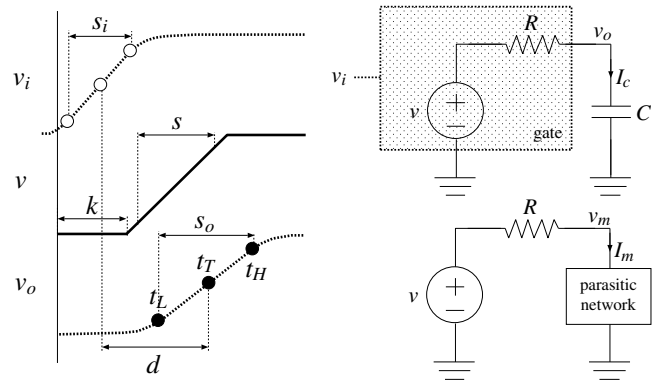

Fig. 1. Cell model, loaded by the effective capacitance (top right), and by the original parasitic network (bottom) and corresponding waveforms (left).

circuit. Computing the delay along a path requires the computation of the delay of every cell along that path, plus the added delay due to interconnect between the cells. In this section we review the standard computation of cell and interconnect delay.

A. Cell Delay and Cell Loading

The most familiar type of cell library model today are the delay look-up tables (LUTs) sometimes referred to as *dot-lib (.lib)* tables. This is a simplified model where delay and power information is maintained in the form of a few parameters. In this simplified model the timing behavior of a cell is usually characterized by a set of lookup tables that, for each input/output pin pair, describe the delay and output slew of the cell as a function of the input slew and output load. Such a model is illustrated in Figure 1 where the standard definitions are also used, namely input and output slews are defined as $s = t_H - t_L$, where t_L and t_H are the time instants at which the respective waveform reaches some pre-defined values, V_L and V_H, related to the definition of noise margins. In a similar manner, delay is defined as the time it takes the output of a cell to reach its transition midpoint, from the time the cell input waveform reached its own midpoint. Cell characterization is performed by simulating the cell behavior as a function of input slew and loading capacitances. These results are then stored in look-up tables as mentioned, which are accessed to determine delay and slew in specific instances.

In Figure 1, the output load is assumed to be a single lumped capacitance that somehow models the capacitive effects introduced by the interconnect and by the input pins of the cells connected to same net. In reality, however, the interconnect attached to the driver cell is a complex RC network that in deep submicron processes is very poorly modeled by a lumped capacitance. The loading effect of interconnect on the cell, i.e. the impact of downstream interconnect on the cell delay itself, cannot be accurately obtained simply by looking at the total capacitance on the net. To try to account for the effects of complex interconnect, while still preserving table-based cell models, the concept of *effective capacitance* has been widely adopted. For the remainder of this paper we will consider that the C shown in Figure 1 is such an effective capacitance.

The idea behind the effective capacitance consists in determining the value of C that in a certain sense approximates as accurately as possible the behavior of the original parasitic network. In Figure 1. the output stage of a cell (or more accurately, of an output pin of a cell) is modelled by a voltage source, producing a voltage ramp v, with slew s, and a series resistor, with resistance R, that models the output resistance of the pin. The figure depicts the output stage of a cell loaded by the effective capacitance C (top right), and by the original parasitic RC-network, obtained by layout extraction (bottom right). In the following, without loss of generality, in order to simplify the description, we restrict ourselves to the case of rising output waveforms for non-inverting cells. Clearly any other case can be derived in a similar manner.

The simple RC circuit on the top of Figure 1 is an approximated model of the output stage of a cell connected to an effective capacitance, that is itself an approximation of the interconnect load. For a given input slew s_i and a given effective capacitance C, we can compute the estimated cell delay d and the estimated output slew s_o, by a simple table lookup in the timing characterization of the cell. Using this information, we can easily compute the three time instants at which the waveform of the output voltage v_o should cross V_L, V_T and V_H, respectively,

$$t_L = \frac{s_i}{V_H - V_L} V_T + d - \frac{s_o}{V_H - V_L}(V_T - V_L) \tag{1}$$

$$t_T = \frac{s_i}{V_H - V_L} V_T + d \tag{2}$$

$$t_H = \frac{s_i}{V_H - V_L} V_T + d + \frac{s_o}{V_H - V_L}(V_H - V_T) \tag{3}$$

For the simple RC circuit presented in Figure 1, with time constant $\tau = RC$, excited by a rising ramp of slew s, shifted in time by k, the voltage v_o is given by,

$$v_o(s,\tau,k,t) = \begin{cases} 0 & if\ \ 0 \le t < k \\ \frac{\alpha V_{DD}}{s}(-\tau + t - k + \tau e^{-\frac{t-k}{\tau}}) & if\ \ k \le t < k + \frac{s}{\alpha} \\ V_{DD} - \frac{\alpha \tau V_{DD}}{s}(e^{\frac{s}{\alpha}} - 1)e^{-\frac{t-k}{\tau}} & if\ \ t \ge k + \frac{s}{\alpha} \end{cases} \tag{4}$$

where $\alpha = (V_H - V_L)/V_{DD}$. In order to simplify our notation, in the following we will assume,

$$\phi = \langle s, k, R, C \rangle. \tag{5}$$

Using Eqn. (4), we can compute a waveform for v (e.g. s and k) and a resistance R, such that the waveform of the response v_o crosses (t_L, V_L), (t_T, V_T) and (t_H, V_H), thus matching the tabulated behavior of the cell and its output response. This problem can be stated by the following three equations,

$$v_o(t_L, \phi) = V_L \tag{6}$$

$$v_o(t_T, \phi) = V_T \tag{7}$$

$$v_o(t_H, \phi) = V_H \tag{8}$$

The waveform of v can be seen as the "ideal" output voltage of the cell, under a zero output load.

We should not lose track of the fact that our goal is to determine an appropriate value for the effective capacitance C. The previous derivations assumed that such a value was somehow known. However, all that is required is that C should approximate the behavior of the original parasitic network as accurately as possible. Several criteria [8] can be used when defining what effective capacitance provides a good approximation of the behavior of the original parasitic network. In this work we consider that the effective capacitance that better approximates the behavior of the original parasitic network is the one that draws the same average current, over the transition period (e.g. when the output voltage switches from V_L to V_H). Formally,

$$\langle I_c \rangle = \langle I_m \rangle \Leftrightarrow \frac{1}{s_o} \int_{t_L}^{t_H} I_c \, dt = \frac{1}{t_H' - t_L'} \int_{t_L'}^{t_H'} I_m \, dt \tag{9}$$

where $v_m(t_L^{'}) = V_L$ and $v_m(t_H^{'}) = V_H$. $\langle I_c \rangle$ can be computed analytically. $\langle I_m \rangle$ must be computed by numerically integrating the port current, obtained by interconnect simulation, as detailed in Section II-B. From Eqns. (6), (7), (8), and (9) we can compute the value of ϕ that both matches the output waveform v_o with the tabulated timing information at t_L, t_T and t_H, and also that matches the average current drawn by the original parasitic network and the effective capacitance. Since Eqns. (6), (7), (8) and (9) contain nonlinear terms, an implicit iterative method must be used to solve them. We have used Newton's method in this work.

Once the value of the effective capacitance C is known, we can compute the delay d and output slew s_o of the cell by a simple lookup in the timing characterization of the cell. This completely characterizes the cell output waveform within the constraints of the simple model. Such a waveform constitutes the input to the interconnect model.

B. Interconnect Delay

Assuming that the cell delay has been computed, signals are then propagated along the path through an interconnect net. The input of such nets, designated by *port*, are tied to the output of a cell, and the net outputs, which we will refer to as *taps*, connect to the inputs of several other cells. At the timing level, the difference in the timing of the transition at the cell output (port) and next cell inputs (taps) we refer to as the intrinsic interconnect delay.

There are various methods of computing the interconnect delay ranging from closed-form expressions that are descendants of the Elmore delay formula to numerical solution of the underlying interconnect equations. In this work we assume the circuit equations of the cell driver plus interconnect network system are solved numerically, either via direct integration or an equivalent process like recursive convolution. Likewise the slew at the output nodes must be computed to be used in the analysis of the following cell.

III. Variation-Aware Methodology

A. General Perturbation Formulation

In this section, we will discuss the parametric analysis of the intrinsic interconnect delay itself. The impact of the interconnect parameters on the cell delay (i.e. variation in cell loading effects) is taken up in the next section.

The starting point of our analysis is the general formulation of time-varying linear perturbation theory (see [6] for details). We assume the existence of a set of nonlinear differential-algebraic equations whose topology is fixed, but whose constitutive relations depend on a continous way on a set of parameters. Without loss of generality the basic circuit equations can be written as

$$\frac{d}{dt}q(v,\lambda) + i(v,\lambda) = u(t) \tag{10}$$

where $v \in \mathbb{R}^n$ represents the circuit state variables, for example, node voltages, $q \in \mathbb{R}^n$, the dynamic quantities such as stored charge, $i \in \mathbb{R}^n$, the static quantities such as device currents, t, time, and $u(t) \in \mathbb{R}^n$, the independent inputs such as current and voltage sources. In departure from the usual case, we introduce a p-element parameter vector $\lambda \in \mathbb{R}^p$. These parameters represent properties of the circuit, such as wire width or thickness, that induce variation in the circuit behavior through the q and i functions.

The perturbation approach to modeling the parameter variation treats the parameters as fluctuations $\Delta\lambda$ around a nominal value λ_0, and assumes the circuit response v can be treated similarly, i.e.

$$\lambda = \lambda_0 + \Delta\lambda \tag{11}$$

$$v = v_0 + \Delta v. \tag{12}$$

Expanding i and q as a function of v and λ and keeping the first order variations,, we get

$$q(v,\lambda) = q(v_0,\lambda_0) + \frac{\partial q}{\partial \lambda}\Delta\lambda + \frac{\partial q}{\partial v}\Delta v \tag{13}$$

$$i(v,\lambda) = i(v_0,\lambda_0) + \frac{\partial i}{\partial \lambda}\Delta\lambda + \frac{\partial i}{\partial v}\Delta v. \tag{14}$$

Assuming a solution to the nominal case, $v_0(t)$ is obtained, that is

$$\frac{d}{dt}q(v_0,\lambda_0) + i(v_0,\lambda_0) = u(t) \tag{15}$$

then substituting the perturbation expansions (13) and (14) into Eqn. (10) and using (15) to eliminate the nominal-case terms, we obtain the equations for the first-order perturbation expansion as

$$\frac{d}{dt}\left[\frac{\partial q}{\partial v}\Delta v\right] + \frac{\partial i}{\partial v}\Delta v = -\left[\frac{d}{dt}(\frac{\partial q}{\partial \lambda})\Delta\lambda + \frac{\partial i}{\partial \lambda}\Delta\lambda\right] \tag{16}$$

The simplest way to compute waveform sensitivities from Eqn. (16) is by solving it once for each parameter in turn, as

$$\text{for each } k: \quad \frac{d}{dt}\left[\frac{\partial q}{\partial v}\frac{\partial v}{\partial \lambda_k}\right] + \frac{\partial i}{\partial v}\frac{\partial v}{\partial \lambda_k} = -\left[\frac{d}{dt}(\frac{\partial q}{\partial \lambda_k}) + \frac{\partial i}{\partial \lambda_k}\right]. \tag{17}$$

This gives the final expression

$$v(t,\lambda) = v_0(t) + \sum_{k=1}^{p}\frac{\partial v}{\partial \lambda_k}(t)\Delta\lambda_k. \tag{18}$$

Once the sensitivities in the waveforms are known, the next step is to translate to sensitivity of delay. As discussed, delay can be computed as $d = t_2 - t_1$ where t_2, t_1 are the crossing times of the two waveforms of interest. The sensitivity in a crossing time can be related to the sensitivity of the waveform value $v(t)$ at that point via the slew, $\partial v/\partial t$. Suppose there is a small change ΔT in the crossing time of a given waveform. With a linear model, the corresponding change in the voltage is

$$\Delta V = \frac{\partial v}{\partial t}\Delta T. \tag{19}$$

Conversely, if the perturbation in the waveform ΔV can be computed, the change in crossing time is given by

$$\Delta T = \frac{\Delta V}{\frac{\partial v}{\partial t}}. \tag{20}$$

Therefore we can compute the sensitivity of the delay as

$$\frac{\partial d}{\partial \lambda_k} = \frac{\frac{\partial v}{\partial \lambda_k}\Big|_{t_2}}{\frac{\partial v}{\partial t}\Big|_{t_2,\lambda_0}} - \frac{\frac{\partial v}{\partial \lambda_k}\Big|_{t_1}}{\frac{\partial v}{\partial t}\Big|_{t_1,\lambda_0}} \tag{21}$$

Note that for this computation, we only need the waveform sensitivity at a few points in time. This fact can be used to further speedup computations (see [6] for details).

This is the formulation for a general first-order perturbation analysis. In the following we restrict ourselves to the problem at hand, namely modeling the linear interconnect sub-circuits assuming variations in parameters affecting the interconnect elements.

B. Specialization to Interconnect

Our concern in this document is with the special case of interconnect parameters, so simplifications of the general theory are possible. On-chip cell-level interconnect models are usually written in terms of capacitances and resistances, or equivalently, capacitances and conductances. Inductance is typically neglected at this level and for the sake of simplicity we will proceed likewise; it is however easy to see that the derivation is quite similar when inductance is involved. Therefore, in this case,

$$q(v,\lambda) = C(\lambda)v \qquad i(v,\lambda) = G(\lambda)v \tag{22}$$

so that

$$\frac{\partial k}{\partial \lambda_k} = \frac{\partial G}{\partial \lambda_k}v \qquad \frac{\partial q}{\partial \lambda_k} = \frac{\partial C}{\partial \lambda_k}v \tag{23}$$

Let us then assume, for now, that for every element in the parasitic network (resistor or capacitor), a linear variational model is available. Such a model contains the nominal values for the elements and also the sensitivities to each parameter. Therefore, the conductance and the capacitance matrices have the form:

$$G = G_0 + \sum_{k=1}^{p} (G_k \Delta\lambda_k) \tag{24}$$

$$C = C_0 + \sum_{k=1}^{p} (C_k \Delta\lambda_k) \tag{25}$$

where G_0 and C_0 are the nominal values of the elements in the interconnect network and the sensitivities $\frac{\partial G}{\partial \lambda_k}$ and $\frac{\partial C}{\partial \lambda_k}$ to each parameter λ_k are given by

$$\frac{\partial G}{\partial \lambda_k} = G_k \qquad \frac{\partial C}{\partial \lambda_k} = C_k. \tag{26}$$

The nominal value corresponds to the solution of the equations with each $\Delta\lambda_k = 0$, that is $\lambda = \lambda_0$. Assuming the variational formulation for G presented in Eqn. (24), and for v presented in Eqn. (12) we obtain, for instance for $i(v,\lambda)$:

$$i(v,\lambda) = \left[G_0 + \sum_{k=1}^{p} (G_k \Delta\lambda_k)\right](v_0 + \Delta v) \tag{27}$$

Simplifying and eliminating the (non-linear) cross-product terms, we obtain:

$$i(v,\lambda) \approx G_0 v_0 + G_0 \Delta v + \sum_{k=1}^{p} (G_k v_0 \Delta\lambda_k) \tag{28}$$

implying that:

$$i_0 \equiv i(v_0, 0) = G_0 v_0 \tag{29}$$

$$\frac{\partial i}{\partial v} = G_0 \tag{30}$$

$$\frac{\partial i}{\partial \lambda_k} = G_k v_0 \tag{31}$$

An identical procedure can be applied to $q(v,\lambda)$ leading, as expected, to:

$$q \approx C_0 v_0 + C_0 \Delta v + \sum_{k=1}^{p} (C_k v_0 \Delta\lambda_k) \tag{32}$$

and therefore, that:

$$q_0 \equiv q(v_0, 0) = C_0 v_0 \tag{33}$$

$$\frac{\partial q}{\partial v} = C_0 \tag{34}$$

$$\frac{\partial q}{\partial \lambda_k} = C_k v_0 \tag{35}$$

Eqns. (15) and (16) which describe the general perturbation analysis framework, can therefore, in the specialization of parameter-varying interconnect, be written as:

$$C_0 \frac{d}{dt} v_0(t) + G_0 v_0(t) = u(t) \tag{36}$$

$$C_0 \frac{d}{dt}[\Delta v] + G_0 \Delta v = -\sum_{k=1}^{p} \left[\frac{d}{dt}(C_k v_0(t))\Delta\lambda_k + G_k \Delta\lambda_k\right] \tag{37}$$

The delay modeling problem is completed by adding the notion of inputs and outputs to form state-space models. In the case of cell-level interconnect, the inputs are represented by drivers, the output stages of cells. For the sake of simplicity of exposition here, we will assume that the input is given by a fixed current source. However, other models (e.g. voltage drivers, or nonlinear current source models [9], [10]) are treated in a similar fashion. In this case,

$$u(t) = B i_{drv}(t) \tag{38}$$

where B is a vector (or matrix, in the case of multiple simultaneous source inputs) that describes the connection of every input source to the interconnect network. For the case of current input sources, B is simply an incidence matrix indicating at which node each driver is connected to.

Similarly, in the case of cell-level interconnect, the outputs are typically receivers, the inputs of the following gates in the circuit. We denote such outputs as "taps" and monitor voltage at these "taps". Assuming that the output is represented by voltage, mathematically this is represented by another matrix L as

$$v_{tap} = L^T v \tag{39}$$

where again L is an incidence-type matrix describing which voltage nodes are monitored.

Using this representation, the full set of equations is now

$$C_0 \frac{d}{dt} v_0(t) + G_0 v_0(t) = B i_{drv}(t) \tag{40}$$

$$v_{0,tap}(t) = L^T v_0(t) \tag{41}$$

$$C_0 \frac{d}{dt}[\Delta v] + G_0 \Delta v = -\sum_{k=1}^{p} \left[\frac{d}{dt}(C_k v_0(t))\Delta\lambda_k + G_k \Delta\lambda_k\right] \tag{42}$$

$$\Delta v_{tap} = L^T \Delta v \tag{43}$$

These equations can be written more compactly if we define

$$s_k(t) = -\left[C_k \frac{d}{dt} v_0(t) + G_k v_0(t)\right] \tag{44}$$

where $v_0(t)$ is the nominal solution computed above. s_k can be interpreted as the "equivalent source" that will allow determination of the sensitivity to the kth interconnect parameter. With this definition, the final, complete set of equations is then rewritten as

$$C_0 \frac{d}{dt} v_0(t) + G_0 v_0(t) = B i_{drv}(t) \tag{45}$$

$$v_{0,tap} = L^T v_0(t) \tag{46}$$

$$C_0 \frac{d}{dt}[\Delta v] + G_0 \Delta v = \sum_{k=1}^{p} s_k(t)\Delta\lambda_k \tag{47}$$

$$\Delta v_{tap} = L^T \Delta v \tag{48}$$

C. Interconnect Sensitivity Calculation

The process of sensitivity calculation can now be concisely stated. First, solve Eqns. (45) and (46) to get the nominal case responses. Then, for each parameter k, solve

$$C_0 \frac{d}{dt}\left[\frac{\partial v}{\partial \lambda_k}\right] + G_0\left[\frac{\partial v}{\partial \lambda_k}\right] = s_k(t) \tag{49}$$

$$\frac{\partial v_{tap}}{\partial \lambda_k} = L^T\left[\frac{\partial v}{\partial \lambda_k}\right] \tag{50}$$

to get the sensitivity of the response waveforms. From the sensitivity waveforms, the delay sensitivity can be computed. Of course, in practice, it is useful to diagonalize the state-space model above, i.e. to put the C_0, G_0 matrices into pole-residue form, as numerical solution of the multiple systems is much more efficient.

IV. Cell Delay Sensitivity Calculation

In the preceding section, we have seen how to perform variation-aware delay computation, by computing the sensitivities of the response waveforms in interconnect blocks. However, it is also necessary to show that similar sensitivites can be computed at the output of cells, in particular assuming that cell delay computation is still based on delay table models.

To show this, we refer back to the derivation in Section II and in particular to Eqns. (6), (7), (8) and (9). If we perform an expansion around a nominal point ϕ_0, keeping the first order variations, and eliminating the nominal-case terms, we obtain,

$$\Delta v_o(t_L, \Delta\phi) = 0 \tag{51}$$

$$\Delta v_o(t_T, \Delta\phi) = 0 \tag{52}$$

$$\Delta v_o(t_H, \Delta\phi) = 0 \tag{53}$$

$$\langle \Delta I_c \rangle (t_L, t_H, \Delta\phi) = \langle \Delta I_m \rangle \tag{54}$$

Noticing the dependence of t_L, t_T and t_H, on d and s_o, and their dependence on s_i and C, we obtain the generic equation,

$$\begin{aligned} &\frac{\partial v_o}{\partial s}\Delta s + \frac{\partial v_o}{\partial k}\Delta k + \frac{\partial v_o}{\partial R}\Delta R \\ &+ \left(\frac{\partial v_o}{\partial C} + \frac{\partial v_o}{\partial t_X}\frac{dt_X}{dC}\right)\Delta C + \frac{\partial v_o}{\partial t_X}\frac{dt_X}{ds_i}\Delta s_i = 0 \end{aligned} \tag{55}$$

where

$$\frac{dt_X}{dC} = \frac{\partial t_X}{\partial s_o}\frac{\partial s_o}{\partial C} + \frac{\partial t_X}{\partial d}\frac{\partial d}{\partial C} \tag{56}$$

$$\frac{dt_X}{ds_i} = \frac{\partial t_X}{\partial s_i} + \frac{\partial t_X}{\partial s_o}\frac{\partial s_o}{\partial s_i} + \frac{\partial t_X}{\partial d}\frac{\partial d}{\partial s_i}. \tag{57}$$

t_X can be replaced by t_L, t_T or t_H to obtain Eqns. (51), (52), and (53), and all derivatives are computed at time t_X. For Eqn. (54) a similar expansion can be performed,

$$\begin{aligned} &\left(\frac{\partial \langle I_c \rangle}{\partial s} - \frac{\partial \langle I_m \rangle}{\partial s}\right)\Delta s + \frac{\partial \langle I_c \rangle}{\partial k}\Delta k \\ &+ \left(\frac{\partial \langle I_c \rangle}{\partial R} - \frac{\partial \langle I_m \rangle}{\partial R}\right)\Delta R + \frac{d\langle I_c \rangle}{dC}\Delta C + \frac{d\langle I_c \rangle}{ds_i}\Delta s_i = \langle \Delta I_m \rangle \end{aligned} \tag{58}$$

where

$$\frac{d\langle I_c \rangle}{dC} = \frac{\partial \langle I_c \rangle}{\partial C} + \frac{\partial \langle I_c \rangle}{\partial t_L}\frac{dt_L}{dC} + \frac{\partial \langle I_c \rangle}{\partial t_H}\frac{dt_H}{dC} \tag{59}$$

$$\frac{d\langle I_c \rangle}{ds_i} = \frac{\partial \langle I_c \rangle}{\partial t_L}\frac{dt_L}{ds_i} + \frac{\partial \langle I_c \rangle}{\partial t_H}\frac{dt_H}{ds_i} \tag{60}$$

Δs_i and $\langle \Delta I_m \rangle$ are related to the parameter variation vector, $\Delta\lambda$, by the following expressions,

$$\Delta s_i = \frac{\partial s_i}{\partial \lambda}\Delta\lambda \tag{61}$$

$$\langle \Delta I_m \rangle = \frac{\partial \langle I_m \rangle}{\partial \lambda}\Delta\lambda \tag{62}$$

where $\frac{\partial s_i}{\partial \lambda}$ and $\frac{\partial \langle I_m \rangle}{\partial \lambda}$ are the sensitivity vectors. Resorting to Eqns. (55), (58), (61), and (62), we can now represent Eqns. (51), (52), (53), and (54) in matrix form as,

$$J\Delta\phi = \left(A\frac{\partial s_i}{\partial \lambda} + B\frac{\partial \langle I_m \rangle}{\partial \lambda}\right)\Delta\lambda \tag{63}$$

$\frac{\partial s_i}{\partial \lambda}$ results from the variational timing analysis on the interconnect of the input net, as described in Section III. $\frac{\partial \langle I_m \rangle}{\partial \lambda}$ can be computed by integrating the sensitivities of the port current, I_m, for the transition period and dividing by its width. All the derivatives in J, A and B can either be computed analytically or by accessing the timing characterization of the cell.

If $N_C = [0\ 0\ 0\ 1]$ is a vector that "selects" the capacitance (fourth) row from $\Delta\phi$, then,

$$\Delta C = N_C\Delta\phi = N_C J^{-1}\left(A\frac{\partial s_i}{\partial \lambda} + B\frac{\partial \langle I_m \rangle}{\partial \lambda}\right)\Delta\lambda \tag{64}$$

Acknowledging the dependence of the delay d and the output slew s_o on the input slew s_i and the capacitance C, the following expressions can be derived,

$$\Delta d = \frac{\partial d}{\partial s_i}\Delta s_i + \frac{\partial d}{\partial C}\Delta C \tag{65}$$

$$\Delta s_o = \frac{\partial s_o}{\partial s_i}\Delta s_i + \frac{\partial s_o}{\partial C}\Delta C \tag{66}$$

where $\frac{\partial d}{\partial s_i}$, $\frac{\partial d}{\partial C}$, $\frac{\partial s_o}{\partial s_i}$ and $\frac{\partial s_o}{\partial C}$ can be computed by direct analysis of the lookup table that contains the timing characterization of the cell. Substituting Eqns. (61), (64) in Eqns. (65), and (66), we can derive the sensitivities of the delay and output slew to the parameters,

$$\frac{\partial d}{\partial \lambda} = \frac{\partial d}{\partial s_i}\frac{\partial s_i}{\partial \lambda} + \frac{\partial d}{\partial C}N_C J^{-1}\left(A\frac{\partial s_i}{\partial \lambda} + B\frac{\partial \langle I_m \rangle}{\partial \lambda}\right) \tag{67}$$

$$\frac{\partial s_o}{\partial \lambda} = \frac{\partial s_o}{\partial s_i}\frac{\partial s_i}{\partial \lambda} + \frac{\partial s_o}{\partial C}N_C J^{-1}\left(A\frac{\partial s_i}{\partial \lambda} + B\frac{\partial \langle I_m \rangle}{\partial \lambda}\right) \tag{68}$$

V. Experimental Results

A realistic circuit block was synthesized and mapped to an industrial 90nm technology. As process parameters, we considered the widths and thicknesses of the six metal layers needed to route the block. During parasitic extraction of the design, we computed the nominal values and sensitivities of each parasitic element (resistors and grounded capacitors), relative to each one of the 12 parameters.

In order to validate the interconnect delay and slew computations, we selected from the design 3671 nets, including nets in the internal logic, nets in the clock tree and nets in the pad wiring. For each of these nets, we computed the parametric delay and slew expressions for each of its taps (resulting in 13870 taps among all nets), while the port was excited by a rising voltage ramp. To assess the accuracy of the proposed methodology, the delay and slew sensitivities were compared to transistor-level simulations performed using the circuit simulator SPECTRE. In Figure 2 we present scatter plots of the sensitivities computed by both methods, for 4 parameters. In Figure 3 we present histograms of the relative errors for other 4 parameters. Both figures clearly show that the computed sensitivities accurately match those obtained by simulation.

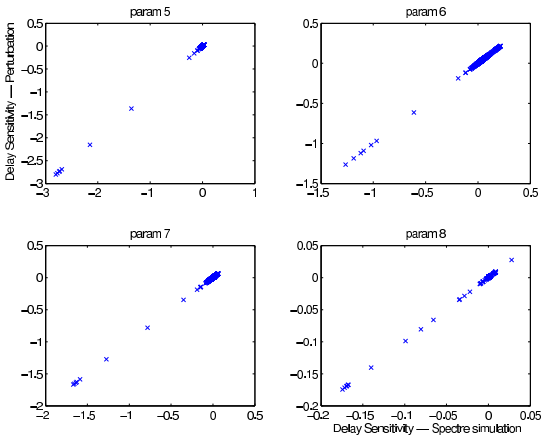

Fig. 2. Computed delay sensitivities vs. transistor-level simulation.

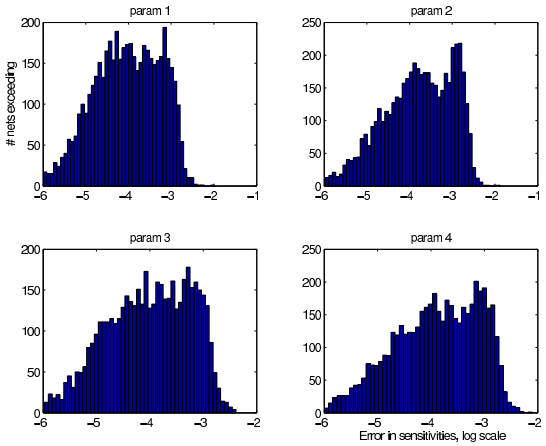

Fig. 3. Histograms of errors in computed delay sensitivities.

In order to validate the cell delay and output slew computations we proceeded as follows. For a given standard cell of that same 90nm technology, and using Spice-level models, we generated a dotlib-style lookup table of size 7x7, for delay and output slew, as a function of input slew and load. Using these tables, and applying the proposed methodology, we computed the delay and output slew sensitivities for one of the cell instances in the previously mentioned design, considering its loading net obtained from extraction. Using the methodology proposed in Section IV we generated the sensitivities of delay and output slew to all 12 parameters. Next, varying the parameter values, a similar set of sensitivities was also computed with SPECTRE, using accurate Spice-level models for the cell. The delay and output slew sensitivity values obtained using the proposed method were then assessed by computing its relative error versus the SPECTRE-generated data. These relative errors are shown in Figure 4 (left plot). As can be observed, the errors are in general small, usually in the low percentage range. The only exception to this rule is the pathological case of the slew sensitivity to parameter #2, whose absolute value is small, the smallest of all the sensitivities and near machine precision. In order to investigate this behavior, we introduced a variation in the input slew depending on parameter #2, so that the delay and output slew sensitivity values to this parameter would become larger. As a result we observed that when this happened the relative error dropped to the normal range, as shown in Figure 4

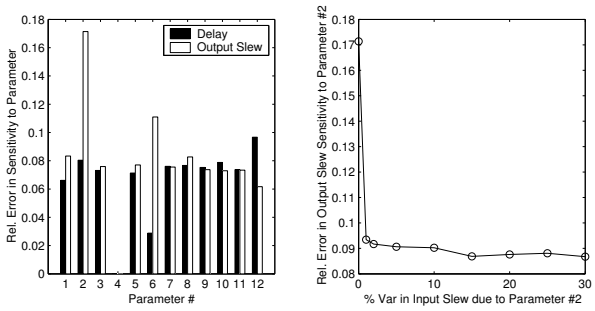

Fig. 4. Relative errors in computed cell delay and output slew sensitivities.

(right plot). Considering that the size of the dotlib-style lookup table used was only 7x7 (typical value), providing a rough approximation of the behavior of the cell, and that the parasitic network was also approximated by a single lumped capacitance, we believe that the accuracy of the computed values is fairly good. Better accuracy should be obtained by using larger lookup tables, or by extending the proposed model for handling tables depending on other parameters.

VI. CONCLUSIONS

In this paper we have developed an analytic delay calculation methodology suitable for use in a statistical static timing methodology. Our approach, based on a specific type of perturbation analysis, allows for the analytical computation of the quantities needed for statistical delay propagation. We also showed how perturbation analysis can be performed when only the standard delay table lookup models are available for the standard cells. The techniques proposed are robust and show good correlation with transistor level calculations. Future work will show how to develop models that include nonlinear contributions from the process parameters.

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