EMPLOYING RADIATION HARDNESS BY DESIGN TECHNIQUES WITH COMMERCIAL INTEGRATED CIRCUIT PROCESSES[1]

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ABSTRACT

Though process hardening remains the preferred method for achieving radiation hardness in high density integrated circuits (ICs), recent investigations[1] into the hardness of specially designed gate array cells fabricated in a commercial 0.8μm CMOS fabrication process have demonstrated greater than 100 krads(Si) total ionizing dose hardness, no single event latchup, and single event upset LET (linear energy transfer) (LET) thresholds greater than 50 MeV-cm^2/mg. This work suggests that it is possible to achieve inexpensive ASICs (Application Specific Integrated Circuits) of modest complexity and radiation tolerance with commercial IC processes.

INTRODUCTION

Space system electronics must survive the natural radiation environment associated with the earth's radiation belts, the solar wind, and galactic cosmic rays (GCRs). For earth orbiting satellites, the radiation environment which must be survived is a function of the altitude and inclination of the orbit and the life of the satellite. An estimate of the total ionizing dose accumulated per year due to electrons and protons for four different orbits is shown in Table 1.[1] Total ionizing dose can result in degradation in microcircuit performance (i.e., increased propagation delay times, lower maximum clock rates, reduced output drive, lower noise margins, increased leakage, and catastrophic failure).

Furthermore, single event effects resulting from GCR strikes or spallation reactions from proton strikes can cause high amplitude, short duration current transients which may discharge nodes causing information loss or initiate latchup conditions leading to catastrophic failure.

With the deemphasis of strategic systems following the end of the Cold War, many vendors have abandoned the production of radiation hardened microcircuits. The parts available from the remaining vendors are quite expensive, and there are long delivery times. However, some relief from the dilemma of radiation hardened parts availability can be achieved by identifying the mechanisms responsible for radiation effects in microcircuits and implementing electrical and layout design solutions to minimize them. These solutions must be consistent with typical semiconductor processing so that resulting microcircuits can be fabricated in commercial foundries. Basically, this approach trades off area and circuit density for radiation hardness.

Table 1. Total Ionizing Dose from Electrons and Protons in rad(Si)/yr[2] (100 mil Al satellite skin)

Orbit Name	GEO[3]	GPS[4]	LEO[5]	DMS[6]
Apogee (km)	35,796	20,189	1,600	846
Perigee (km)	35,795	20,172	1,600	824
Inclination (degrees)	0	55	60	99
Dose rad(Si)/yr	6,600	59,000	17,300	1,260

RADIATION EFFECTS MECHANISMS

Total Ionizing Dose

Parasitic Edge Leakage

As illustrated in Figure 1, MOS transistors are typically designed for a self aligned process in which the polysilicon gate material is deposited over a thin

[1] Sponsored by USAF Phillips Laboratory under Contract F29601-96-D-0043 Subtask 02-01.

[2] 1 rad = 100 ergs/gm in the indicated material.
[3] Geosynchronous orbit.
[4] Global Positioning Satellite.
[5] Low Earth Orbit
[6] Defense Meteorological Satellite.

oxide region. The source/drain implant is then performed and fills the region not covered by field oxide and poly. This process is very manufacturable and produces very dense circuits. Unfortunately, the material at the transition between the field oxide and the thin oxide produces a parasitic transistor that is very susceptible to total ionizing dose effects.[2] The silicon dioxide in this region (known as the bird's beak) is under mechanical stress produced by the dynamics of the oxide growth process and the transition from thin to thick oxide. The transition region oxide is of variable thickness and experiences a relatively high electric field from the combination of poly gate bias and the fringing fields from the source to drain bias.

When this region is exposed to ionizing radiation, significant hole trapping occurs and affects the I/V characteristic as shown in Figure 2. At 150 krad(Si), the edge leakage has increased by approximately three orders of magnitude over its pre-irradiation value. At increasing doses, more of the edge parasitic will become involved in the conduction path, and the leakage will quickly rise to become roughly equivalent to the on-state current of the intrinsic transistor. Edge leakage effects are typically manifested as a rapid increase in supply current with increasing total dose, as the parasitic edge transistors shunt the source-to-drain current around the intrinsic transistor. They may also produce functional failure as the composite N-channel becomes permanently "on".

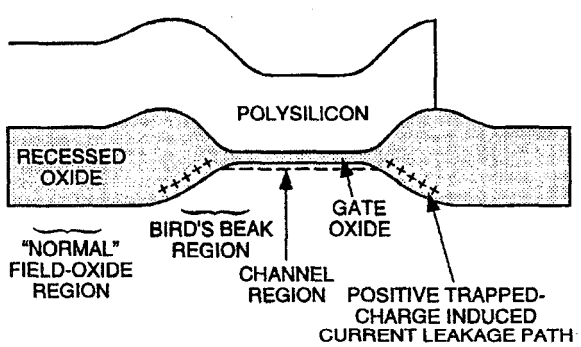

Figure 1. MOS transistor cross section (McLean and Oldham, 1987).

Commercial foundries pay little attention to the characteristics of the edge transition region since the edge parasitic is not turned on in commercial applications. Thus, edge parasitics in commercial devices are quite susceptible to radiation effects, and there is large variability in radiation tolerance since there is little control of the process parameters affecting hardness. Therefore, edge effect mitigation for commercial processes usually requires layout modification.

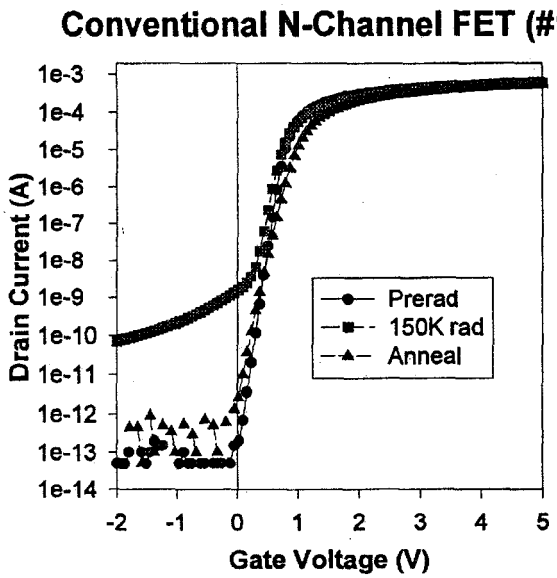

Figure 2. Commercial technology 2-edge N-channel transistor edge effects induced by total ionizing dose.

The most effective layout uses a re-entrant design (Figure 3b) for the N-channel transistor which totally eliminates the thin-to-thick oxide edge between source and drain. Only the N-channel requires a re-entrant design since the P-channel does not experience edge inversion. The effectiveness of the re-entrant structure in eliminating radiation induced edge leakage and its compatibility with commercial processes make it the leading candidate for design hardening practice.

Field Oxide Leakage Another total ionizing dose induced leakage mechanism is associated with the field oxide (FOX) which provides isolation between adjacent transistors. An illustration of the structure of the parasitic FOX transistor is shown in Figure 4. The leakage paths are formed when positive charge is trapped in the field oxide and inverts the surface of the P-type material.[3] Two types of leakage paths are possible. The first is between the N-well (which is typically connected to Vdd), and an N-plus source (which is connected to Vss). The leakage path connects Vdd to Vss, producing a change in supply current with increasing radiation.

Field oxide leakage paths can also span the N-plus source/drain regions between adjacent N-channel transistors. This will increase the Vdd to Vss leakage. Adjacent N-plus source/drain regions

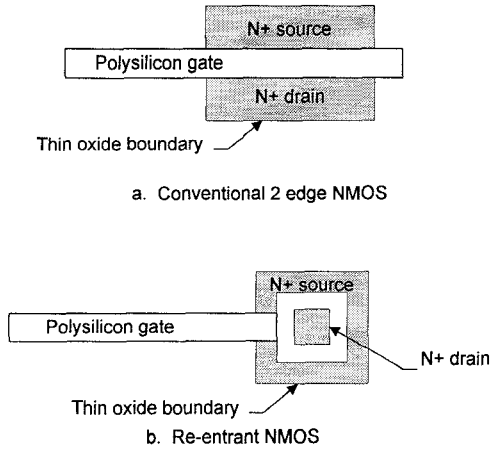

Figure 3. 2-edge and re-entrant topographies.

should not be allowed without an intervening channel stop. A channel stop is a more heavily doped P-region implanted at the interface between the field oxide and the silicon. The increased doping makes the channel stop region more difficult to invert and effectively breaks the leakage path. Most commercial processes include some type of channel stop or field threshold adjust step to control mobile ion effects. However, the step may not be carefully monitored, and the tendency of the P-type implant (i.e., boron) to be leached out during the field oxide growth process results in considerable variability in lot-to-lot leakage characteristics in commercial microcircuits.

The results of field oxide leakage characterization of a typical commercial, submicron technology are shown in Figure 5. Prior to irradiation the parasitic field oxide transistor required approximately 15 volts to turn on the leakage path. The turn-on characteristic is clearly degraded at low doses. An accumulation of 10 krad(Si) produces significant leakage at 5 volts, and 30 krad(Si) produces leakages which would render the microcircuit inoperable.

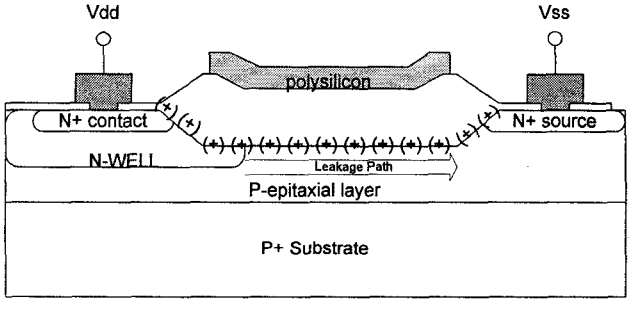

Figure 4. N-well to N+ source leakage path.

Field oxide inversion is the dominant failure mechanism in many commercial microcircuits. The failure may be due to supply current greatly exceeding its specification (e.g., SRAM standby current), input and output leakage currents exceeding parametric specification (e.g., output tri-state leakage), or catastrophic functional failure. Large increases in static supply current with dose are indicative of field inversion.

Total ionizing dose induced field oxide leakage may be reduced by inserting a heavily doped P region in the current path. Since most commercial process do not include provisions for increasing the P-type implant under the field oxide, a P-plus source/drain implant must be used as depicted in Figure 6.

This approach significantly increases the spacing between adjacent N-plus regions and N-well to N-plus regions. However, it is very effective in breaking the leakage path.

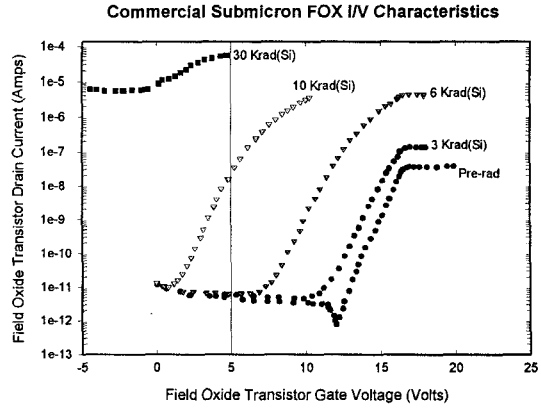

Figure 5. Total dose effects for a typical commercial, submicron CMOS technology.

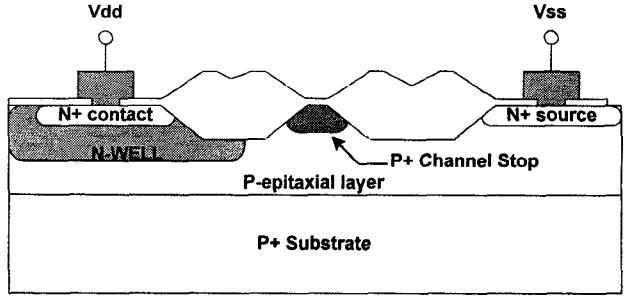

Figure 6. Field oxide P-plus implant channel stop.

Transistor Performance When total ionizing dose induced edge and field oxide leakage effects have been mitigated by using re-entrant design and P-plus channel stops, the performance of the N-channel

and P-channel transistors can be quite robust in a radiation environment. Changes in transistor performance with total dose accumulation are due to positive charge being trapped in the oxide and the build up of interface states. Oxide trapped charge is particularly troublesome in N-channel transistors since it moves the threshold voltage toward depletion mode operation, and consequently decreases noise margin and increases "off-state" current. However, the amount of radiation induced positive oxide trapping is roughly proportional to the inverse of the square of the gate oxide thickness (t_{ox}^{-2}).[4] Since the industry trend is toward thinner gate oxides (e.g., 170Å for a typical 0.8 μm technology), the intrinsic transistors should become harder to total dose.

Interface state build up moves both N-channel and P-channel threshold voltages further into enhancement mode operation and reduces carrier mobility. The result is reduced current drive capability. Interface states also decrease the slope of subthreshold I/V characteristics for both N-channel and P-channel transistors resulting in higher leakage currents. The number of interface states resulting from total dose exposure is a complex function of the fabrication process. The use of hydrogen rich environments for some process steps can be particularly detrimental. Therefore, no general statement can be made concerning the susceptibility of commercial process to radiation induced interface states.[5]

The performance of a re-entrant N-channel and 2-edge P-channel transistor fabricated with the Hewlett Packard 0.8 μm process is shown in Figures 7 and 8, respectively. Neither transistor shows significant change in the I/V characteristic after 160 krad(Si). The N-channel transistor clearly shows the influence of radiation induced interface states following a post-irradiation anneal cycle (100 °C for 168 hours) designed to significantly reduce oxide trapped charge and enhance interface state creation. However, the off-state current and the maximum drive current are not significantly affected. This performance should be compared with that shown previously in Figure 2 for a standard 2-edge N-channel transistor. Clearly, the transistor characteristics shown in Figures 7 and 8 are adequate for designing circuits with good post-irradiation operability.

Single Event Effects

Single Event Latchup The parasitic silicon controlled rectifier (SCR) composed of a four layer PNPN structure inherent in CMOS is a serious problem for microcircuits exposed to GCRs and

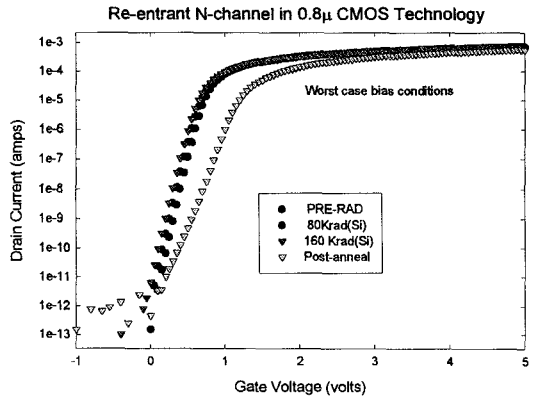

Figure 7. Re-entrant N-channel total dose data.

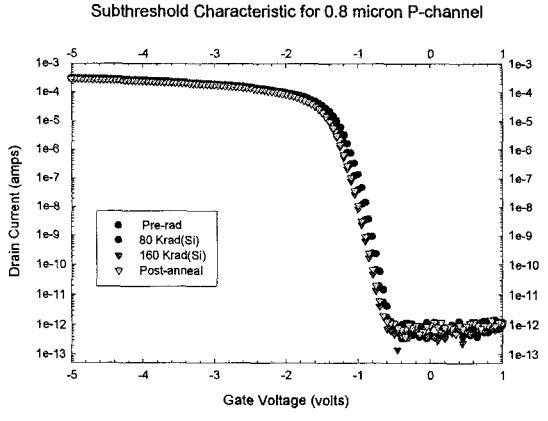

Figure 8. Total ionizing dose data for a P-channel transistor.

protons. The parasitic SCR consists of P-source/drain, N-well, P-substrate, and N-source/drain. It can be turned on by a heavy ion strike and produce a latchup condition that may catastrophically damage the microcircuit.

The latchup path structure for a P-epi technology is shown schematically in Figure 9.[6] The path has been shown in terms of the traditional cross coupled transistor model of an SCR. Under normal bias conditions the P-substrate is held to the lowest potential in the circuit, and the N-well is held to the highest potential. None of the junctions associated with the PNPN structure are forward biased, and the SCR is off. However, an ionization track associated with single particle strike can produce a current transient which will inject charge into either the cathode or anode gate regions.[7] The voltage drop associated with this current flowing to either the well

or the substrate contacts can be sufficient to forward bias a local portion of the junction. This results in bipolar transistor action that rapidly becomes regenerative as the parasitic SCR turns on. The latch path will conduct until the voltage across the path falls below the holding voltage, typically V_{beon} + V_{cesat}. Since this is a low impedance path and often occurs between adjacent Vdd and Vss contacts, the currents may be large enough to burn out metallization and catastrophically damage the IC.

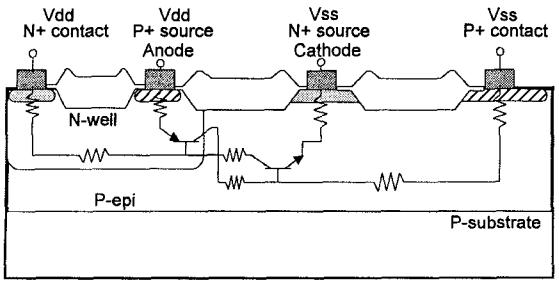

Figure 9. Latch path for CMOS.

There are several design practices which can reduce susceptibility to latchup. The cross coupled transistor model of the parasitic SCR suggests that if the gain product of the parasitic NPN and PNP transistors is reduced below 1 (i.e., $\beta_{NPN}\beta_{PNP} < 1$) over the possible range of collector current, the latchup condition cannot be sustained. Also, if the anode or cathode gate junctions are shorted so that a V_{beon} cannot be maintained, the path will not latch. The design practices employed to reduce latchup susceptibility include (1) increasing the spacing between the N-plus and P-plus source/drain regions and the well edge, (2) adding N-plus guardbands in the N-well and P-plus guardbands in the P-substrate to reduce the gain of the parasitic transistors and control the potential of the well and substrate in the latch path, and (3) increasing the number of well and substrate contacts and decreasing the distance between the contacts and the latch path.

Single Event Upset At the transistor level, a single ion strike is experienced as a current transient appearing at the source/drain node.[8] If the magnitude of the charge in the transient is sufficiently high, the information stored as charge on the node may be lost. The amplitude and duration of the transient is determined by the ion species, its energy, and the fabrication technology of the microcircuit. The shape and amplitude of the transient will be affected by the existence and thickness of an epitaxial layer, the doping profile and depth of the well, and the lateral spacing between adjacent transistors. The current transient waveforms may be approximated with a double exponential function with a FWHM (full width at half maximum) pulsewidth ≥100 Ps for a fast transient.[9]

Several approaches exist which may be considered for mitigating single ion transients for better SEU performance. They begin with selection of a technology with a structure to minimize charge collection. An epi process with the thinnest epi layer and the highest substrate doping is most desirable to reduce funneling effects (i.e., early enhancement of charge collection by the acceleration of charge carriers in the cylindrical ionization sheath by the distorted electrical field from the junction depletion region).[10]

Layout modifications can also be used to mitigate single ion transients at the transistor level. For example, the area of the drain region can be minimized to reduce to cross section of vulnerable nodes. For conventional 2-edge designs, this means eliminating extended drains used as crossunders or intermediate routing layers. This is particularly important where silicided source/drain regions provide low resistivity material. For re-entrant designs, it means using the interior of the annulus as the drain because of its smaller area

Since a significant amount of the charge in an ionization path can be collected by diffusion (particularly for high LET strikes), layout modifications to increase the distance between adjacent devices and to introduce recombination regions can be helpful. Introduction of substrate and well contacts between devices can help prevent multiple bit upsets from a single particle strike.

Radiation Hardening by Design

Primitive Cell

The design procedures identified above for mitigating radiation effects mechanisms have been implemented in a gate array design. A gate array approach was selected because of its simplicity. All the radiation tolerance is achieved in the underlayers and in restriction of macrocell stacking height. This permits the ASIC designer to concentrate on the application function rather than specific hardening techniques. New macrocell designs can be performed by designers with a wide variety of radiation hardness background without compromising the hardness of the result.

The key to the design hardened gate array is the primitive cell shown in Figure 10. It consists of two re-entrant N-channel transistors and two 2-edge P-channel transistors sized for equivalent drive

strength. Edge leakage effects are eliminated by the re-entrant design.

The field oxide leakage is eliminated by enclosing the N-channel thin oxide regions (source/drain) with a channel stop composed of the P-plus source/drain implant of the P-channel transistors. The P-plus source/drain must be used because there is no other mask definable layer for a P-plus channel stop available at most commercial foundries. The polysilicon gate cannot be allowed to cross the P-plus, because it would create a gap in channel stop since the source/drain implants are self aligned to the poly. The gap would provide a possible source-to-well leakage path. Obviously, a significant area penalty has been paid for the channel stop and elimination of polysilicon interconnect between gates. However, all of the potential total-dose-induced leakage paths have been mitigated with the exception of those associated with the intrinsic transistor.

The channel stop also acts as a guardband for latchup suppression. It reduces the gain of any surface lateral NPN transistor by introducing a P-plus region in the base. It also keeps the base of the NPN very close to ground potential by providing a low impedance path to Vss. The foundry process used to fabricate the gate array is silicided so the resistivity of the polysilicon and the source/drain regions is approximately 2 ohms per square. The guardband has five Vss contacts located along the right edge.

To be doubly sure that no SEL problems will be encountered, an N-plus guardband has been placed in the N-well around the P-channel transistors. This spoils the gain of any surface lateral PNP transistor and ties the PNP base to Vdd through a low impedance path to five contacts located along the left edge. Clearly, the double guardbands result is an additional area penalty, but the area tradeoff was worthwhile to minimize latchup prospects.

Hardened Macrocell Designs

A library of frequently used macrocell functions has been developed to support microcircuit designs. Sixty types of macrocells are currently available and additional cells are being added to the library as they are developed to support new designs

Gate array electrical design and layout software has been chosen to keep cost low and provide maximum access. All layout has been done in MAGIC version 6.4.4, which is available over the Internet at gatekeeper.dec.com. Versions are available for both Sparc work stations and PCs

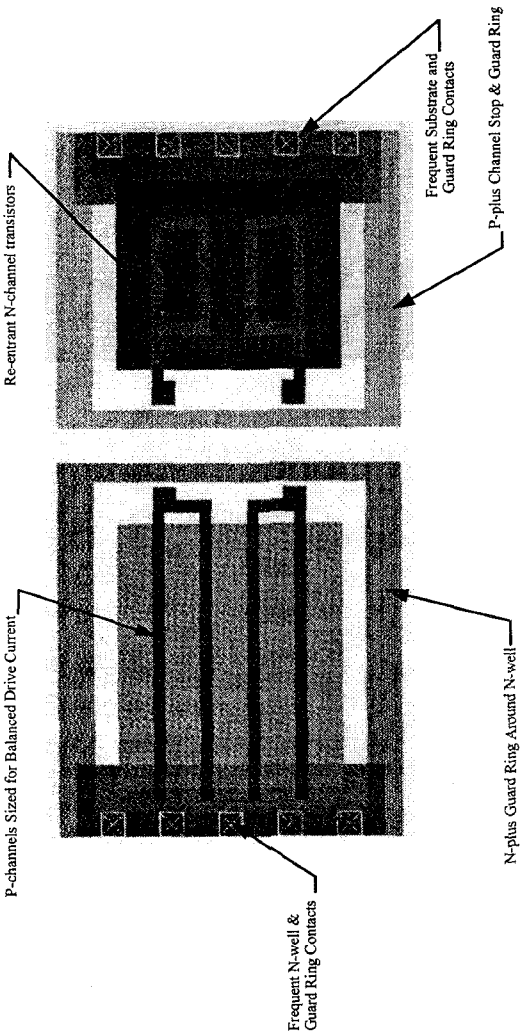

Figure 10. Primitive cell for rad hard gate array

running OS2. The MAGIC layout editor incorporates an on-line DRC (design rule check) capability, which minimizes or eliminates the need for additional DRC tools. All schematic capture for the electronic design of the cells has been done with ORCAD, a PC based tool. Parameters are available for the MOSEQ3 transistor models. VHDL models for the most frequently used cells are available with timing parameters reflecting best, nominal, and worst case performance. Routing is done with the widely used GARDS router from SVR (Silicon Valley Research, Inc.). All of these tools are available as public domain software, low cost PC based software, and as a service by several third party companies.

Hardened Microcircuit Demonstration

To demonstrate the viability of the hardened by design concept, a test chip and a microcircuit implementing a dual register file (DRF) in a 12K gate array were fabricated and tested. Figure 11 is a

photomicrograph of the DRF. The register file occupies two thirds of the die and the remainder is used for design experiments. The fabrication was performed through the MOSIS (MOS Implementation Service) clearing house developed by DARPA and managed by ISI (Information Sciences Institute). [11]. MOSIS subcontracts with several different commercial foundries to process lots on a periodic basis. Microcircuit layouts submitted by their customers are assembled onto a multi-project reticle and passed to the foundry. The participating foundries are high volume commercial lines capable of very high performance. The Hewlett Packard 0.8 μm CMOS foundry is particularly attractive for a design hardened gate array. The process uses a P-epi layer on a P-plus substrate. The epi layer is relatively thick (≈ 12.5 μm), but it is still helpful in suppressing latchup. The process uses one level of polysilicon and three levels of metal. The poly and source/drain regions are silicided with a resistivity of approximately 2 ohms per square. The gate oxide thickness is 170 Å. Design rules for the technology are available through Internet at ftp.mosis.edu.

Fabrication costs for the HP foundry are determined by the die area at the rate of approximately $600 and $650 per mm^2 for government and non-government organizations, respectively. The customer is guaranteed 25 die for this cost. Dedicated wafers (150 mm) can be purchased with a minimum of three wafers costing $88,700. The reticle size is 17mm x 17mm, and there is a leverage of 40 reticles per wafer. MOSIS purchases the wafers to the foundry's parametric specifications. The customer is responsible for ensuring that his design works within the range of the parametric limits. The fabrication cycle is 8 to 9 weeks. Packaging is available for the cost of the packages plus a nominal fee.

Radiation testing has been performed on both the test chip and the DRF. Pre- and post-irradiation performance of a 101 cell, 4-input NOR delay chain is shown in Figure 12. The pulse width corresponds to the total chain delay. Both pre-irradiation and post-irradiation delays are shown.

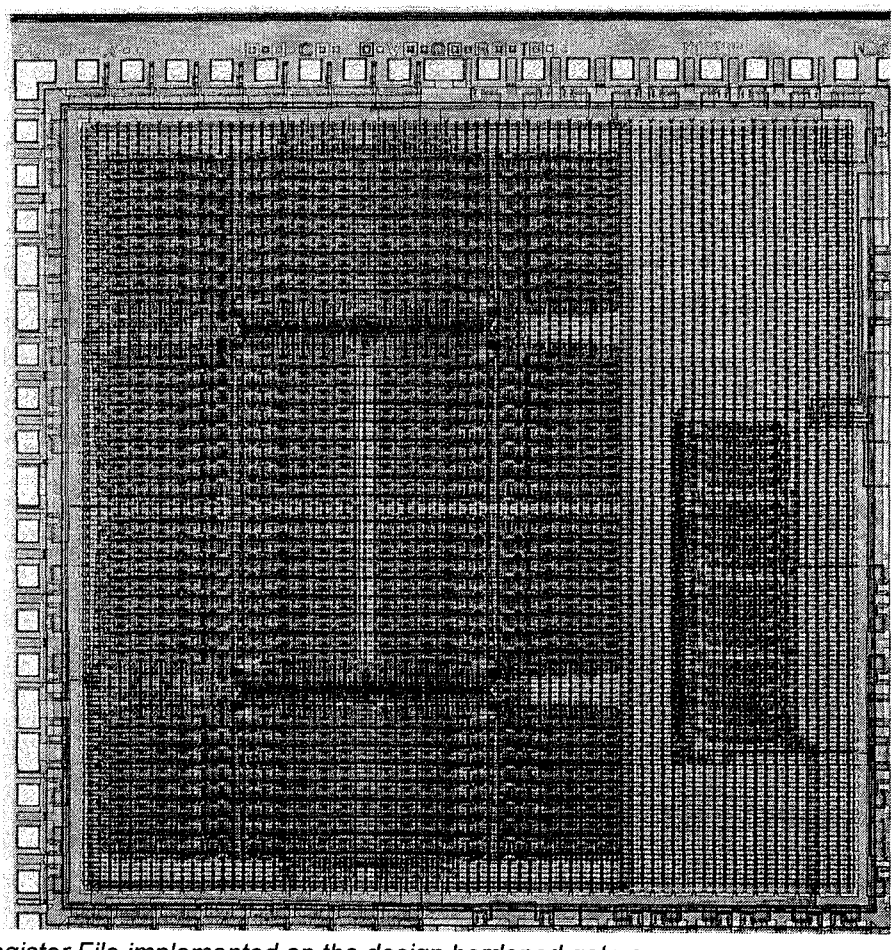

Figure 11. Dual Register File implemented on the design hardened gate array.

The NOR chain represents the worst case performance for total ionizing dose irradiation. It shows minimal change in performance at doses significantly in excess of the goal of 100 krad(Si).

SEU and SEL testing was performed on the DRF at the Brookehaven National Laboratory Tandem Van de Graaff facility. Figure 13 shows the results of the SEU testing and indicates an LET upset threshold greater than 50 MeV-cm^2/mg. This corresponds to 1.7×10^{-7} errors per bit day (ebd) for geosynchronous orbit and 3.5×10^{-9} ebd for low earth orbit (600 km).

The SEL tests were performed at Vdd = 5.5 volts and a temperature of 100 °C to simulate worst case conditions for latchup susceptibility. No latchup was observed for ions up to 102 MeV-cm^2/mg, the limit of the facility. This indicates that the device is essentially immune to latchup in space applications.

Summary

This paper has presented a radiation tolerant design approach suitable for developing ASICs with

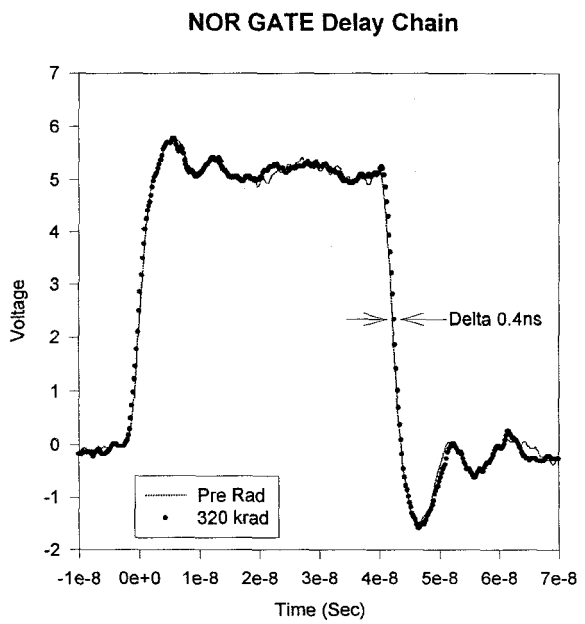

Figure 12. Pre- and Post-irradiation performance of a 101 cell NOR delay chain.

complexities of 100K gates with radiation hardness requirements for no single event latchup and total dose exposures in excess of 100 krad(Si). Activities are currently underway to extend the cell library to 0.6 μm feature size and to develop a library supporting design synthesis using Synopsis tools.

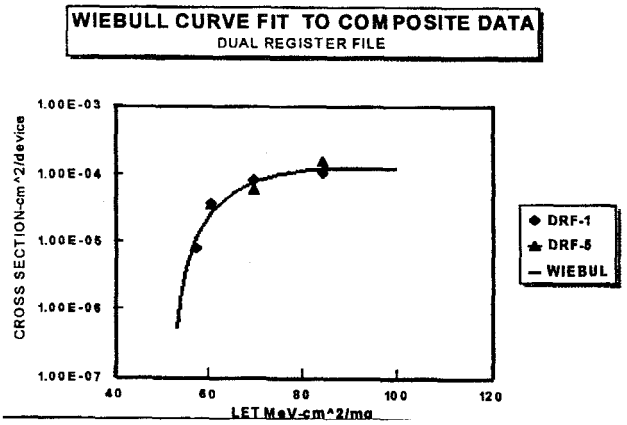

Figure 13. Results of DRF SEU test at Vdd = 4.5 V.

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