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MULTI-BAND and WIDEBAND LOW NOISE AMPLIFIERS

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Dissertação para a obtenção do Grau de Doutor
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Sumário

A maioria das arquitecturas de receptores de rádio utiliza somente uma banda de frequência, relativamente estreita em relação à frequência central. Actualmente há uma procura grande de equipamentos capazes de comunicar com diferentes normas, utilizando diferentes bandas de frequência. Isto requer que os blocos do receptor sejam multi-banda ou tenham banda de passagem larga de modo a acomodarem as diferentes bandas em que se pretende efectuar a comunicação.

Nesta tese estudam-se diferentes topologias de amplificadores de baixo ruído, quer multi-banda, quer de banda larga.

Tipicamente, um amplificador de baixo ruído recebe sinais de alta frequência de uma antena, através de uma linha de transmissão. A distância da antena ao amplificador é geralmente da ordem de grandeza do comprimento de onda e por isso a impedância de entrada do amplificador deve estar adaptada à impedância característica da linha que vem da antena, para maximizar a potência de sinal fornecida ao amplificador. O amplificador de baixo ruído deve também amplificar o sinal recebido com adição de ruído mínima. A montagem que serve de base a muitos amplificadores de baixo ruído é a montagem cascode com degeneração indutiva.

Nesta tese são propostos dois circuitos de amplificadores de baixo ruído operando em duas (ou mais) bandas, ambos baseados na montagem cascode com degeneração indutiva. Ambos os circuitos têm uma entrada com adaptação de impedância abrangendo duas ou mais bandas simultaneamente. O primeiro circuito encaminha as diferentes bandas por caminhos distintos, utilizando os transistores cascode para activar uma ou mais saídas. O segundo circuito tem uma única saída onde ocorrem duas bandas simultaneamente. este circuito permite variar o ganho relativo nas duas bandas e, no limite, cancelar uma das bandas, através da variação de uma tensão de polarização.

Nesta tese também se mostra que é possivel realizar amplificadores de baixo ruído com banda larga utilizando duas malhas de realimentação. Em primeiro lugar, são determinadas quais as topologias de realimentação dupla adequadas à realização de amplificadores de baixo ruído. Das montagens possíveis, há uma que é analizada com mais detalhe. Uma primeira análise é feita considerando um modelo detalhado da malha de realimentação e um bloco de amplificação ideal. Posteriormente,

considera-se um bloco de amplificação não ideal e um modelo simples de malha de realimentação e estabelecem-se as condições para que o bloco de amplificação se possa considerar ideal.

É projectado um protótipo do amplificador de baixo ruído com duas malhas de realimentação estudado em mais detalhe. O seu dimensionamento é descrito em detalhe e os resultados das medidas efectuadas sobre um circuito de teste são apresentados e analizados.

Palavras-Chave:

Micro-electrónica, Rádio Receptores sem Fios, Amplificador de Baixo Ruído, Amplificador de Baixo Ruído Multi-Banda, Amplificador de Baixo Ruído de Banda Larga, Realimentação com Duas Malhas, Transformador Integrado.

Abstract

Most wireless receiver architectures use a single frequency band, with a bandwidth much smaller than the central frequency. Nowadays, there is a great demand for equipments able to operate with different communication standards, using different frequency bands. The receiver building blocks must be either multi-band or wideband, to accommodate the different frequency bands.

In this thesis, different multi-band and wideband low noise amplifiers (LNAs) are studied.

Typically, an LNA receives high frequency signals from an antenna, through a transmission line. The distance between the antenna and the LNA is usually of the order of the signal wavelength; thus, the LNA input impedance must be matched to the transmission line in order to maximize the power transfer. The LNA must amplify the received signal with reduced noise addition. The cascode stage with inductive degeneration is the most widely used topology in LNA design.

In this thesis, two LNA circuits operating in two (or more) bands are proposed. Both circuits are based on the cascode LNA with inductive degeneration. Both circuits have input impedance matching for two or more frequency bands simultaneously. The first circuit splits the different bands through different outputs, using the cascode transistors to activate one or more outputs. The second circuit has a single output where both frequency bands are present simultaneously. This circuit is able to vary the relative gain at both bands (and may even cancel one of them) by changing the cascode bias voltage.

In this thesis, it is also shown that it is possible to design wideband LNAs using amplifiers with two feedback loops; these are referred to as double loop feedback (DLF) LNAs. The double loop feedback topologies suitable for LNA design are determined. From the possible topologies, one is studied in more detail. A performance analysis is done using a detailed model for the feedback network and an ideal amplifying block. Another analysis, using a detailed amplifier model and a simple feedback model, is performed to establish the conditions for the amplifying block to be considered ideal.

A prototype of the DLF LNA, which was studied in more detail, was produced. An important element of this LNA is an integrated transformer, which is described

in detail. Measurement results of the transformer alone and of the complete LNA circuit are presented and discussed.

Key-Words:

Microelectronics, Wireless Receivers, Low Noise Amplifier, Multi-band LNA, Wide-band LNA, Double Loop Feedback, Integrated Transformer.

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We know accurately only when we know little, with knowledge doubt increases.
Johann Wolfgang von Goethe

Wichtig ist, dass man nicht aufhört fragen.[1]
Albert Einstein

[1]It is important that men never stops questioning.

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List of Symbols and Acronyms

δ	Skin effect parameter
Δf	Bandwidth
ε_{ox}	Oxide permittivity
γ	Bias dependent factor
Γ	Reflection coefficient
λ	Wavelength
μ	Air magnetic field
Ψ	Magnetic flux
σ	Metal conductivity
ADC	Analog-to-Digital Converter
AMS	Austria Mikro Systeme
F	Noise Factor
DLF	Double Loop Feedback
IF	Intermediate Frequency
i_n	noise current
G	Power gain
G_A	Available gain
g_m	Transistor transconductance
G_m	Amplifying block transconductance
G_T	Transducer power gain
H	Magnetic field
IIP_3	Third-order intercept point
j	Imaginary unit
k	Magnetic coupling coefficient
k_B	Boltzmann constant
K_1, K_2,...	Taylor coefficients
LNA	Low Noise Amplifier
LO	Local Oscillator
n	Transformer voltage ratio
N	Noise power
NF	Noise Figure
$P_{-1\text{dB}}$	1 dB compression point
PSD	Power Spectral Density
q	Electron charge
RF	Radio Frequency
R_S	Source Resistance
S	Signal power
Si	Silicon
SiGe	Silicon-Germanium
SiO_2	Silicon Oxide
S_{xy}	Scattering parameter
SNR	Signal-to-Noise Ratio
T	Absolute temperature
v_n	Noise voltage
Z_0	Characteristic impedance

Chapter 1

Introduction

1.1 Background and Motivation

A few years ago, wireless receivers worked typically at a single frequency band using a single communication standard; however, the interest in wireless receivers working with different communication standards at different frequencies is increasing [1].

In figure 1.1 the input of a general wireless receiver is represented. It comprises several blocks that can be found in most wireless receiver architectures. These blocks are an antenna, a low noise amplifier (LNA), a mixer, and a local oscillator (LO).

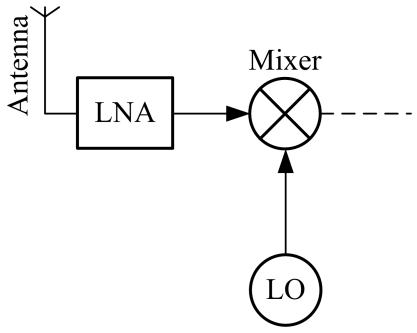

Figure 1.1: Input of a general wireless receiver.

Typically, the antenna receives a high frequency carrier modulated by a signal that is amplified by the LNA and is then multiplied at the mixer by a periodic signal generated at the LO [2–5]. The simplest form of obtaining multi-standard receivers consist of duplicating the receiver and tuning the replicas to different frequencies; however, this is not the most economical solution [1]. An alternative consists on using multi-band blocks [6].

This thesis is dedicated to the study of LNAs suitable for multi-standard receivers.

The LNA is the first block of a receiver, and is responsible for the amplification of the radio signal received by the antenna. The received radio frequency (RF) signal has typically a high frequency, which leads to propagation effects (if the signal travels distances of the same order of the signal wavelength); these should be minimized by proper impedance matching. This is the case of the connection between the antenna and the LNA input, which is typically performed by a standard 50 Ω transmission line that should be terminated with 50 Ω at both ends. Adapting the impedances at both ends of the transmission line prevents the signal power to be reflected towards

the antenna, when it is received by the LNA. This is specially important when the signal-to-noise ratio (SNR) is low. The LNA should amplify the signal power, with minimum addition of noise, to minimize the SNR degradation. Three major LNA parameters are [2–5, 7–9]:

- gain;
- input impedance;
- noise factor.

The LNA frequency response is also important [4, 10–21]. LNAs can be:

- narrowband;
- multi-band;
- wideband.

Narrowband LNAs work in a narrow band around a high frequency (the bandwidth is several orders of magnitude lower than the center frequency). A multi-band LNA is able to operate at different frequency bands, and a wideband LNA has a large bandwidth (the bandwidth can be of the same order of magnitude of the center frequency). It is desirable that multi-band and wideband LNAs are not obtained simply by replicating several narrowband LNAs, to save power and die-area [6]. In this thesis, techniques to design multi-band and wideband LNAs are studied.

The study of multiband LNAs starts by an overview of their most common design techniques. Some drawbacks are pointed out, like parasitic resistances in the signal path due to switches, or a large die area. To overcome these drawbacks, a new topology based on using inductors with magnetic coupling is proposed. The magnetic coupling leads to the dual-band capability of this LNA, and using current steering it is possible to control the relative gain in the two bands.

Wideband LNAs are important, to explore forms of communication, other than the typical carrier based ones [10, 22]. This thesis explores the applicability of double loop feedback (DLF) to design wideband LNAs [23, 24]. A DLF amplifier is studied in detail and a prototype is designed and measured to confirm the feasibility of this type of wideband LNAs.

1.2 Organization of the Thesis

This thesis is divided into eight chapters and six appendixes. The first three chapters, including this one, show the interest of multi-band and wideband LNAs, describe the basic concepts of radio receivers, and present an overview of the design of low noise amplifiers. Chapters four to six describe the new work developed about multi-band and wideband LNAs. Chapter seven describes the prototyping of a wideband LNA and finally chapter eight draw some conclusions and perspectives future work. Chapters are described ahead in more detail.

Chapter two describes the most important topics on RF design and some major LNA parameters. The scattering parameters are introduced, due to their importance in RF design, mainly to evaluate input impedance matching and gain. The most important noise sources and the circuits noise performance are discussed. Finally, a section is dedicated to the design of inductors and transformers, due to their importance on LNA implementation.

Chapter three gives an overview of LNA implementation. It describes LNA basic concepts, and presents several LNA topologies. Due to its importance on LNA design, the cascode LNA with inductive degeneration is described in more detail. A little known type of LNAs is obtained by using double loop feedback (DLF). In this chapter, DLF topologies suitable for LNA implementation are investigated considering ideal blocks.

Chapters four and five are devoted to multi-band LNAs. In chapter four a multi-band LNA having multiple outputs is studied. This topology receives a multi-band signal that is amplified and split through different narrowband paths. It has the advantage that there are no parasitic resistances in the signal path. In chapter five an LNA with magnetically coupled inductors is proposed. Two different bands can be tuned in the same output. It is shown that the gain at each band can be controlled easily through the variation of a single bias voltage.

In chapter six, one of the DLF topologies suitable for LNA realization that were identified in chapter three is analyzed in more detail. The analysis is divided into two steps. First the LNA performance limits are evaluated assuming an ideal amplifying block. Then, the amplifying block is analyzed and dimensioned in order to be approximately ideal.

In chapter seven, a prototype of the DLF LNA studied in chapter six is designed and experimental results are presented.

Finally in chapter eight, some conclusions are given and suggestions for future research are proposed.

1.3 Original Contributions

The original contributions presented in this thesis are:

1. study of a multi-band LNA, based on the cascode LNA with inductive degeneration, that has multiple outputs, each one controlled by a cascode transistor;
2. proposal of a new dual-band LNA based on current balancing and inductor magnetic coupling, analysis of this new LNA in terms of noise, gain and input impedance [25, 26];
3. study of DLF topologies suitable for LNA realization;
4. study of one DLF LNA, concerning the input impedance, voltage gain and noise performance, considering an ideal amplifying block [27, 28];
5. study of the conditions for the amplifying block in the DLF LNA to be considered ideal [29].

The author has collaborated in a study of the impedance evaluation of integrated circular spiral inductors. Since this matter is somewhat outside the scope of this thesis, it is presented in appendix F [30].

Chapter 2

Topics on Radio Receivers

2.1 Introduction

In figure 2.1 a basic configuration of a communication system is represented [5]. The transceiver (*trans*mitter and re*ceiver*) is responsible for processing a signal transmitted through a channel and to process it into an information recognizable by another part of the system where the transceiver is inserted. The received/sent signals are characterized by a frequency spectrum, that theoretically can occupy frequencies from zero to infinity; however, lower frequencies carry few information and require long antennas, and higher frequencies are highly attenuated [31].

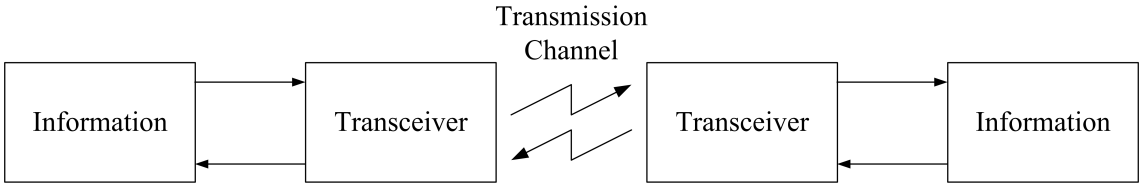

Figure 2.1: Basic configuration of a communication system.

The transceiver performance is determined by the capability of transmitting information. Shannon's equation (2.1) expresses the transceiver capacity C (in bits/second) in terms of the channel bandwidth B [Hz], the signal power S [W], and the noise power N [W] [2, 10].

$$C = B \log_2 \left(1 + \frac{S}{N}\right) \tag{2.1}$$

The ratio S/N is the signal-to-noise ratio (SNR), and measures the signal integrity, since it is proportional to the probability of recovering the information after its transmission [3].

In this thesis, only the receiver is considered, and inside it, a great attention is given to one building block: the low noise amplifier (LNA). The LNA is usually the first receiver block and is responsible for the amplification of the typically weak signals received at the antenna. It should be designed to amplify signal power S without degrading significantly the SNR - Shannon's equation (2.1).

This chapter is divided into six sections. Section 2.1 presents a short introduction to the LNAs working context. In section 2.2, basic wireless receiver architectures are presented and some building blocks surrounding the LNA are briefly referred. Section 2.3 presents the most important LNA parameters: input impedance matching, gain and bandwidth. The scattering-parameters are also introduced due

to their importance in the LNA design. Noise performance is another fundamental LNA parameter, and due to its importance it has section 2.4 dedicated exclusively to it. Finally, section 2.5 describes the design of inductors and transformers, due to their importance as building elements of modern LNA circuits. In section 2.6 some conclusions are drawn.

2.2 Wireless Receiver Architectures

In figure 2.2 a division of a modern wireless receiver into an RF part and a digital part is represented. The RF part of the wireless receiver is responsible for the analog signal processing since this is received by the antenna till it is converted into a binary code at the analog-to-digital converter (ADC), being the remaining signal processing in the digital domain at the digital part.

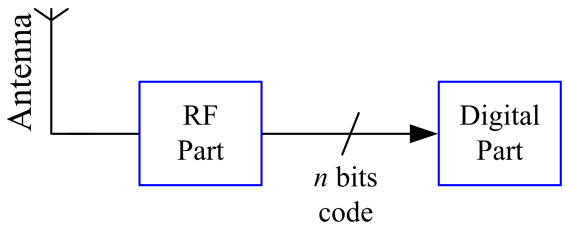

Figure 2.2: Possible block diagram of a wireless receiver.

Theoretically, wireless receivers can work at any frequency; however, low frequencies lead to very long and non-portable antennas, and high frequencies suffer from high attenuation when the electromagnetic wave is propagating through open space. The frequency range of portable wireless receivers is bounded by these considerations and is typically between hundreds of MHz and tens of GHz [2].

With respect to signal bandwidth, wireless receivers can be divided into:

- narrowband receivers;
- multi-band receivers;
- wideband receivers.

In a narrowband receiver, the signal bandwidth is much lower than the carrier frequency [5]. A multi-band receiver can work at several narrowbands. It can work at all narrowbands simultaneously or one at a time. In a wideband receiver, it is possible not to use carrier and the signal bandwidth can be of the same order of magnitude of the central frequency [32].

A quantitative criterion to distinguish a wideband from a narrowband receiver is that the fractional bandwidth is higher than 0.2 for a wideband receiver:

$$2\frac{f_H - f_L}{f_H + f_L} > 0.2 \tag{2.2}$$

where f_H and f_L are, respectively, the upper and the lower frequencies of the signal band [33, 34]. If a signal is wideband and its bandwidth is higher than 500 MHz, the signal is considered an ultra-wideband signal [34, 35].

2.2.1 Common Wireless Receiver Architectures

Most of the wireless receivers used nowadays are carrier-based and narrowband. This means that a high frequency carrier that is modulated by a signal, to be recovered should be down-converted at the receiver to a lower frequency before further processing. Narrowband receivers can be of two basic types [2–5, 7, 36–38]:

- homodyne or Zero-IF (direct conversion) receiver;
- heterodyne or IF (Intermediate Frequency) receiver.

The block diagram of figure 2.3 represents the different blocks of a narrowband receiver and is applicable both to homodyne and heterodyne receivers. The main building blocks are: antenna, low noise amplifier (LNA), local oscillator (LO), mixer, and analog-to-digital converter (ADC).

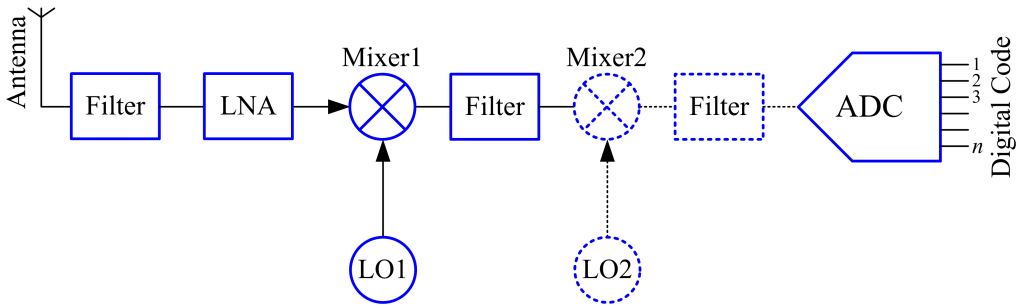

Figure 2.3: Narrowband wireless receiver.

The LNA is responsible for the amplification of the RF signal received by the antenna. The amplified RF signal is then multiplied by a sinusoid (generated by the LO) at the mixer. In an homodyne receiver, the LO sinusoid and the carrier frequency are equal, resulting in a baseband signal at the mixer output. The spurious components resulting from the mixing can then be filtered out (the dashed-line blocks in figure 2.3 are not used). In an heterodyne receiver, the LO frequency is different from the carrier frequency, resulting in an intermediate frequency at the mixer. To relax the filter specifications, more than one mixing/filtering stages can be used, each having a different LO frequency. A special case of heterodyne

receiver, often used, is the low-IF receiver.

These architectures are the most commonly used; however, others can be found in literature [10, 18, 33, 35, 39, 40]. In the following, the wireless receiver building blocks are shortly described and a special emphasis is given to the LNA.

2.2.2 Receiver Building Blocks

Low Noise Amplifier (LNA):

The LNA is the first block of a wireless receiver and its input is typically connected to an antenna. The distance between the two is commonly of the order of the wavelength, which means that the propagation effects require that connections are made using standard impedance transmission lines [7, 31]. To maximize the power transfer, the LNA and the antenna should be impedance matched[1].

As the LNA is at the beginning of the receiver chain, the noise at its input and the noise generated at the LNA are amplified by the gain of the subsequent blocks. Since the input SNR is typically low, the LNA noise contribution should be as low as possible to prevent the degradation of the SNR, when the input signal is amplified. The LNA linearity is not a major concern because the overall wireless receiver linearity is dominated by the last blocks of the receiver chain, mainly the down-converting mixers [4, 38, 41]. LNAs should also have a good feed-forward isolation to prevent instability, and signal leakage from the subsequent blocks that might be reradiated by the antenna [4]. The LNA output impedance does not have to be impedance matched because the following receiver block, usually a mixer, is also integrated and the interconnection can be made short. Finally, LNAs are typically used in portable receivers and should be very efficient in terms of power use.

Chapter 3 is dedicated to the LNA implementation and characterization. There, an overview is made of some of the most common LNA topologies used nowadays.

[1]The most typical value of characteristic impedance is 50 Ω, and this value corresponds to the characteristic impedance of coaxial cables, at which the power transfer capability and the attenuation loss have a better compromise. The exact number is merely conventional and is due to simplicity reasons [2].

Local Oscillator (LO)

An oscillator generates a periodic signal. A voltage controlled oscillator (VCO) is an oscillator, the frequency of which is controlled by a voltage. The periodic signal generated by an LO is used by the mixer to down-convert the high frequency RF signal. One important specification of the LO is low phase noise to prevent down-conversion of the signals of adjacent channels [3, 5].

Mixer

After the LNA, the signal is usually down-converted to a lower frequency by a mixer, which multiplies the LNA output signal by a constant frequency signal. The mixer is a three port block with two inputs and one output. One input receives the LNA output signal and the other input is the LO sinusoid; the output is the product of both input signals, which corresponds to an intermediate frequency IF in an heterodyne conversion and to the baseband signal in a direct conversion receiver [3, 5, 7, 38].

Analog-to-Digital Converter (ADC)

The analog-to-digital converter converts the analog baseband signal into a digital signal. The main ADC specifications are the sampling frequency and the resolution; i.e., the number of bits of the output code [42].

2.3 Basic Concepts of RF Design

Linear circuits having multiple ports can be represented by linear combinations of the voltages and currents at these ports. The matrix description of linear circuits with two ports (2-port) is particularly useful to represent circuits having only one input and one output [43]. Using the general 2-port block, with its port voltages v_i and currents i_i, represented in figure 2.4, different description matrices can be obtained, their choice being dependent on the circuit where the 2-port block is inserted. In appendix A are listed the different matrices.

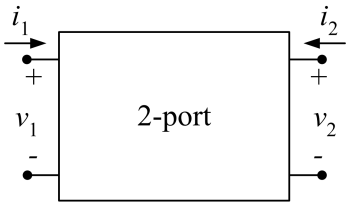

Figure 2.4: 2-port block.

When the signal wavelength is of the same order of the circuit dimensions or interconnects length, the circuit analysis should account for propagation effects [2, 3, 7, 8].

In this thesis, the LNA input is considered to be at a distance of the order of magnitude of the input signal wavelength; and thus, its input should be impedance matched to the input transmission line in order to maximize the power transfer from the signal source and simultaneously overcome undesired signal reflections. The expected LNA circuit dimension is much lower than the signal wavelength, so it can be treated as a lumped element circuit. The importance of impedance matching is discussed in the following.

2.3.1 Impedance Matching and Reflection Coefficient

Figure 2.5 represents a transmission line with characteristic impedance Z_0 excited by a high frequency signal generator V_s and terminated by a load impedance Z_L. The voltage and current have a spacial variation along the line [9]:

$$\begin{cases} V(x) = V^+ e^{-j\beta x} + V^- e^{j\beta x} \\ I(x) = \dfrac{1}{Z_0}(V^+ e^{-j\beta x} - V^- e^{j\beta x}) \end{cases} \tag{2.3}$$

where V^+ and V^- are respectively the amplitudes of the incident and reflected voltage waves, $\beta = 2\pi/\lambda$, λ is the signal wavelength and x is the position. The different signs of the exponents account for the opposite directions in which the incident and reflected waves travel.

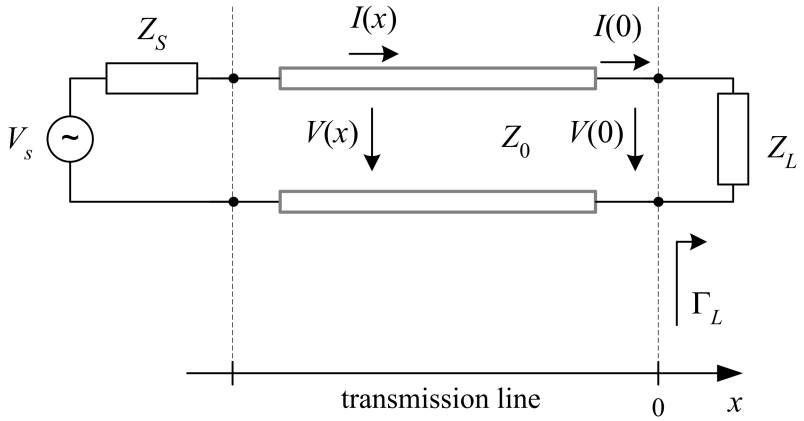

Figure 2.5: Transmission line with characteristic impedance Z_0 terminated with impedance Z_L and excited by voltage generator V_s.

The presence of impedance Z_L at position $x = 0$ makes the signal wave to be partially reflected towards the generator, and as a result of this reflection, next boundary conditions are obtained:

$$\begin{cases} V(0) = V^+ + V^- \\ I(0) = \dfrac{1}{Z_0}(V^+ - V^-) \\ Z_L = \dfrac{V(0)}{I(0)} \end{cases} \tag{2.4}$$

The ratio of V^- and V^+ is the reflection coefficient Γ_L from (2.4) obtaining:

$$\Gamma_L = \frac{V^-}{V^+} = \frac{Z_L - Z_0}{Z_L + Z_0} \tag{2.5}$$

Γ_L corresponds to the reflection coefficient when observing from the transmission line to the load impedance Z_L.

The situation represented in figure 2.5 can be found at the LNA input (here represented by impedance Z_L), where the presence of a reflected voltage V^- means that a voltage wave is propagated towards the antenna and reradiated.

This reradiation is undesired and should be minimized, by reducing the reflected wave V^- by proper impedance sizing. Making the load impedance equal to the transmission line characteristic impedance ensures that the reflection coefficient is zero and consequently the reflected voltage wave V^- is canceled. This situation corresponds to the maximum power transfer from the transmission line to the LNA input because the incident voltage amplitude is maximum.

The theory described here is used to define a form of representing 2-port considering propagation effects.

2.3.2 Scattering Parameters

The scattering parameters or S-parameters allow a 2-port description in terms of incident and reflected power waves. Consider the 2-port represented in figure 2.6, in which ports 1 and 2 have respectively impedances Z_1 and Z_2, and are connected to transmission lines of characteristic impedance Z_0. The 2-port is supplied by a signal source V_s, having an output impedance $Z_S = Z_0$ connected directly to the transmission line. The 2-port has a load impedance $Z_L = Z_0$ connected to the 2-port output via a transmission line. Due to reflections, each port has an incident and a reflected power at their ports represented respectively by P_m^+ and P_m^-, where m is the port number [9].

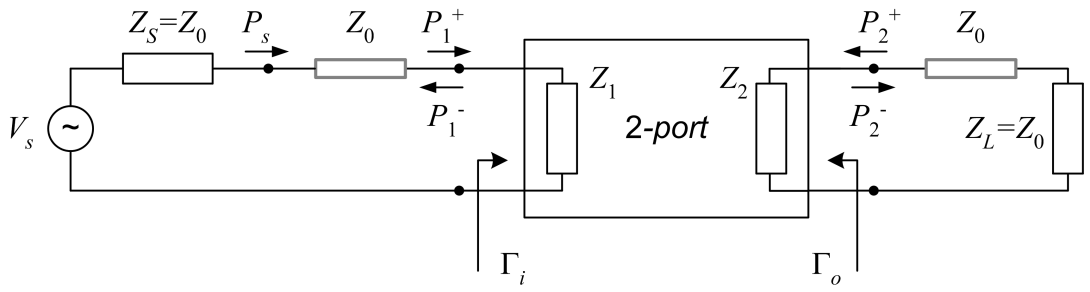

Figure 2.6: 2-port block with incident and reflected waves.

The average power absorbed by each port is equal to the difference between both power components and can be determined by using the incident and reflected wave amplitudes in (2.4). The average power is defined as

$$P_{\text{av}} = \frac{1}{2}\text{Re}\{VI^*\} \tag{2.6}$$

Using equations of (2.4), the reflection coefficient (2.5) and the average power

definition (2.6), the average power absorbed by each port is:

$$P_1 = P_1^+ - P_1^- = \frac{1}{2}\frac{|V_1^+|^2}{Z_0}(1 - |\Gamma_i|^2) \tag{2.7}$$

$$P_2 = P_2^+ - P_2^- = \frac{1}{2}\frac{|V_2^+|^2}{Z_0}(1 - |\Gamma_o|^2) \tag{2.8}$$

where Γ_i and Γ_o are:

$$\Gamma_i = \frac{Z_1 - Z_0}{Z_1 + Z_0} \qquad \text{and} \qquad \Gamma_o = \frac{Z_2 - Z_0}{Z_2 + Z_0} \tag{2.9}$$

With (2.4) and (2.6), the incident and reflected power amplitudes can also be determined as a function of the voltages and currents at the respective port:

$$\begin{cases} P_m^+ = \frac{1}{2}\mathrm{Re}\{V_m^+ I_m^{+*}\} = \frac{|V_m(0) + Z_0 I_m(0)|^2}{4Z_0} \\ P_m^- = \frac{1}{2}\mathrm{Re}\{V_m^- I_m^{-*}\} = \frac{|V_m(0) - Z_0 I_m(0)|^2}{4Z_0} \end{cases} , m \in \{1, 2\} \tag{2.10}$$

Again, Z_0 must be real to consider (2.10) valid. Consider now the square root of the incident and reflected power waves, also known as normalized incident and normalized reflected power waves, and represented by a_m and b_m respectively. Using (2.10) they are:

$$\begin{cases} a_m = \sqrt{P_m^+} = \frac{V_m + Z_0 I_m}{2\sqrt{Z_0}} \\ b_m = \sqrt{P_m^-} = \frac{V_m - Z_0 I_m}{2\sqrt{Z_0}} \end{cases} \tag{2.11}$$

The S-parameters relate a_m and b_m of each port by means of a matrix defined as:

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{pmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{pmatrix} \begin{bmatrix} a_1 \\ a_2 \end{bmatrix} \tag{2.12}$$

Determining S_{11} with (2.4), (2.11) and (2.12)

$$S_{11} = \left.\frac{b_1}{a_1}\right|_{a_2=0} = \frac{V_1 + Z_0 I_1}{V_1 - Z_0 I_1} = \Gamma_i \tag{2.13}$$

It is concluded that S_{11} is equal to the reflection coefficient Γ_1. It can be shown that $S_{22} = \Gamma_o$. This means that S_{11} and S_{22} measure the ratio between the reflected and incident power waves at port 1 and 2 (when no incident wave is present on the other port), being measures of the input and output 2-port impedance matchings.

S_{21} is a voltage gain between the incident voltage at port 1 and the reflected voltage at port 2. Using (2.4), (2.11) and (2.12), S_{21} is

$$S_{21} = \left.\frac{b_2}{a_1}\right|_{a_2=0} = \frac{V_2 - Z_0 I_2}{V_1 + Z_0 I_1} = \frac{V_2^-}{V_1^+} \tag{2.14}$$

S_{12} is known as the reverse voltage gain as it measures the ratio between the incident voltage at port 2 and the reflected voltage at port 1. As determined for S_{21}, S_{12} is

$$S_{12} = \left.\frac{b_1}{a_2}\right|_{a_1=0} = \frac{V_1 - Z_0 I_1}{V_2 + Z_0 I_2} = \frac{V_1^-}{V_2^+} \tag{2.15}$$

2.3.3 Power Gain

Due to the power reflections at the 2-port input and output, different power gain values can be determined. The most used are [7, 9]:

- Transducer Power Gain:

$$G_T = \frac{\text{power delivered to the load}}{\text{power available from the source}} = \frac{P_2^- - P_2^+}{P_s} \tag{2.16}$$

- Power Gain (Operating Power Gain):

$$G = \frac{\text{power delivered to the load}}{\text{power supplied to the 2-port}} = \frac{P_2^- - P_2^+}{P_1^+ - P_1^-} \tag{2.17}$$

- Available Power Gain, G_A, is the ratio between the power at the output of the 2-port and the power delivered by the power source:

$$G_A = \frac{\text{power available at the 2-port output}}{\text{power available from the source}} = \frac{P_2^-}{P_s} \tag{2.18}$$

Since these ratios can vary by several orders of magnitude, it is convenient to express them in dB.

$$G_{\text{dB}} = 10 \log_{10} G \tag{2.19}$$

2.3.4 Signal Distortion and Linearity

Distortion results from circuit non-idealities. Consider the system represented in figure 2.7 and two input signals: $x_1(t)$ and $x_2(t)$.

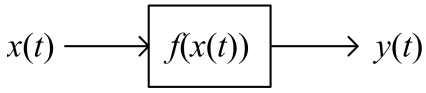

Figure 2.7: System modeling $f(x(t))$ having input $x(t)$ and output $y(t)$.

Consider now the system excited individually by two different inputs $x_1(t)$ and $x_2(t)$, originating respectively y_1 and y_2. The system is linear if,

$$ax_1(t) + bx_2(t) \rightarrow ay_1(t) + by_2(t) \tag{2.20}$$

where a and b are constant [3]. When the system is non-linear, time invariant, and memoryless, and function $f(x(t))$ has all derivatives till m order around a point of operation, it is possible to represent the system by a Taylor series till m degree [44] [45]:

$$y(t) = K_1x(t) + K_2x(t)^2 + K_3x(t)^3 + ... + K_mx(t)^m \tag{2.21}$$

where K_m are the Taylor coefficients [44]:

$$K_m = \frac{1}{m!}\frac{\partial^m f}{\partial x^m} \tag{2.22}$$

Usually, only the first three terms of the Taylor series are considered. These three terms represent a compromise between analysis complexity and approximation error [46]. K_1 is the system gain, and K_2 and K_3 are respectively the second-order and the third-order nonlinearity coefficients, respectively [45]. A practical measure of linearity is the third-order intercept point (IIP_3) and in this case a double tone input signal is considered:

$$x(t) = A\cos\omega_1 t + A\cos\omega_2 t \tag{2.23}$$

where ω_1 and ω_2 are two frequencies inside the bandwidth of operation. Substituting (2.23) in (2.21) and considering only the first three terms, $y(t)$ becomes:

$$\begin{aligned} y(t) &= (K_1 + \frac{9}{4}K_3A^2)A\cos\omega_1 t + (K_1 + \frac{9}{4}K_3A^2)A\cos\omega_2 t + \\ &+ \frac{3}{4}K_3A^3\cos(2\omega_1 - \omega_2)t + \frac{3}{4}K_3A^3\cos(2\omega_2 - \omega_1)t \end{aligned} \tag{2.24}$$

Assuming weak distortion ($K_1 \gg \frac{9}{4}K_3A^2$), the amplitude A for which the output components at ω_1 (and ω_2) equal the components at $2\omega_1 - \omega_2$ (and $2\omega_2 - \omega_1$) is the third-order intercept point IIP_3 [3]:

$$\mathrm{IIP}_3 = \sqrt{\frac{4}{3}\frac{K_1}{K_3}} \tag{2.25}$$

A graphical definition of IIP_3 is represented in figure 2.8. The $P_{-1\mathrm{dB}}$ is the 1 dB compression point, which corresponds to the input power for which the output power is 1 dB below the expected, and the dynamic range is the power range between the noise floor and the $P_{-1\mathrm{dB}}$.

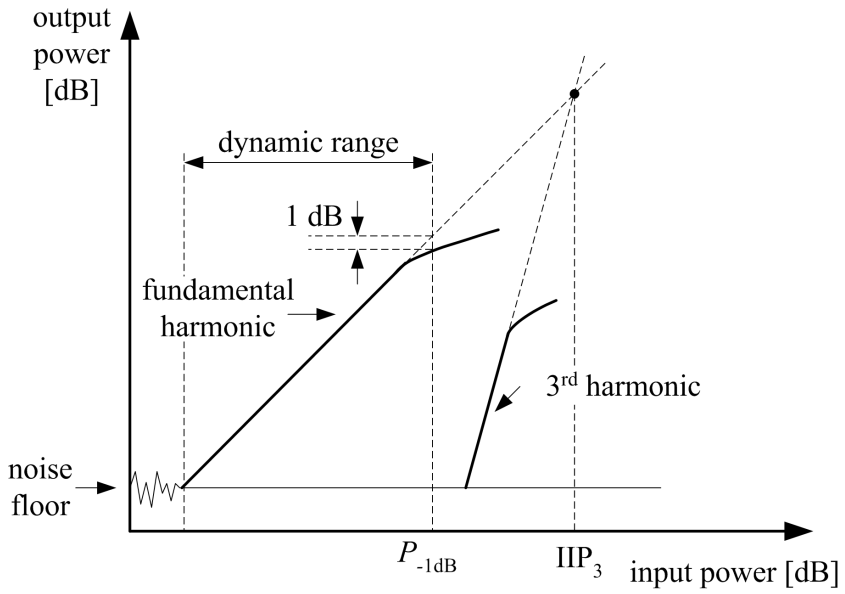

Figure 2.8: Definition of IIP_3.

2.3.5 Bandwidth

Frequency bandwidth of a system is the range of signal frequencies for which the gain has a specified maximum loss (typically 3 dB) with respect to the maximum value. The bandwidth of a signal is the frequency range where almost all signal power (usually 98 or 99%) is located [3]. The signal bandwidth is usually represented by B or by Δf.

2.4 Noise

In electronics, noise is a random fluctuation of a voltage or a current within a circuit [47]. Noise has different sources, having different physical explanations. Most of these sources can be characterized statistically.

In wireless receivers, noise can be divided into external and fundamental noise [48]. External noise is generated outside the receiver, for instance electromagnetic interference in the transmission channel. This kind of noise can be minimized by good electromagnetic shielding and adequate system architecture. Fundamental noise results from physical phenomena in the electronic devices. Several types of fundamental noise are identified: thermal noise, flicker noise and others.

2.4.1 Noise and the Wiener-Khintchine Theorem

The frequency spectrum of a deterministic signal is determined by its Fourier transform, defined as:

$$X(f) = \int_{-\infty}^{+\infty} x(t)e^{-j2\pi ft}dt \tag{2.26}$$

In the case of noise, it is possible to determine the noise power distribution in the frequency domain - power spectral density (PSD), $N(f)$. Its definition is [3, 47]:

$$N(f) = \lim_{T\to\infty} \frac{\overline{|X_T(f)|^2}}{T} \tag{2.27}$$

where $X_T(f)$ is:

$$X_T(f) = \int_0^T x_n(t)e^{-j2\pi ft}dt \tag{2.28}$$

Consider now the 2-port represented in figure 2.9, which has a network function $H(f)$ and is excited by a noise source with PSD $N_x(f)$. The output power spectral density $N_y(f)$ is given by:

$$N_y(f) = |H(f)|^2 N_x(f) \tag{2.29}$$

The relation (2.29) is known as the Wiener-Khintchine theorem and its demonstration can be found in [3, 7, 41, 47, 49].

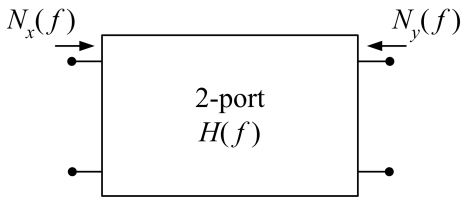

Figure 2.9: 2-port with transfer function $H(f)$ excited by noise source with power spectral density $N_x(f)$.

2.4.2 Noise Figure

The most common noise performance measure used in RF for 2-ports is the noise factor, F, or noise figure, NF, when expressed in dB. It is defined as the ratio between the 2-port total output noise power and the 2-port output noise power due only to the 2-port input noise:

$$F = \frac{\text{Total Output Noise Power}}{\text{Output Noise Power due to the Source}} \tag{2.30}$$

The noise factor as defined above can also be determined by the ratio between the input and output signal-to-noise ratio, SNR_i and SNR_o respectively:

$$F = \frac{\text{SNR}_i}{\text{SNR}_o} \tag{2.31}$$

The SNR is defined as the ratio of the average signal power S and the average noise power N and is independent of frequency. Thus, the noise factor as defined above does not give information about the circuit noise performance along the frequency; however, (2.31) is a good measure of the SNR degradation that a (noisy) signal suffers when processed by a 2-port. Therefore, the noise factor in (2.31) is also known as excess noise factor [2, 47, 50–52].

To express the noise performance as a function of frequency, other noise factor expressions have been proposed, of which the most used is the spot noise factor. To determine the spot noise factor, consider the noisy 2-port of figure 2.10, excited by source characterized by a signal power $S_i(f)$ and a noise power $N_i(f)$.

The source has an available signal power, represented hereafter by $S_i(f)$, which is frequency dependent. The source also has available noise power, frequency dependent, represented by $N_i(f)$. The available power is the (signal or noise) power that

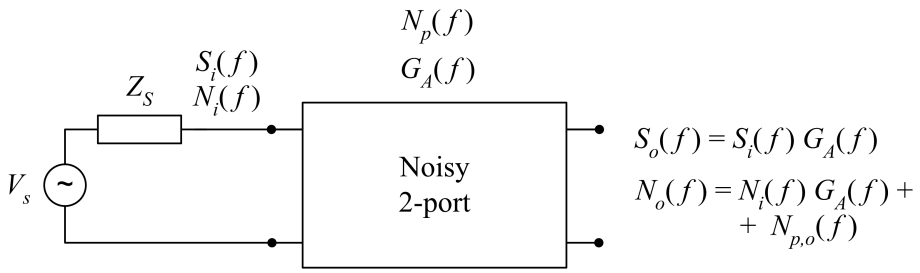

Figure 2.10: Noisy 2-port with available power gain $G_A(f)$ excited by signal and noise source.

would be supplied by the source to a matched load impedance [50]. The source is loaded by a 2-port which has an available power gain $G_A(f)$ and that generates a noise power that reported to the output has a value of $N_{p,o}$. The spot noise factor F is defined as [52]:

$$F(f) = \frac{\dfrac{S_i(f)}{N_i(f)}}{\dfrac{G_A(f)S_i(f)}{G_A(f)N_i(f) + N_{p,o}(f)}} \tag{2.32}$$

The numerator of (2.32) is the ratio of the spectral densities of the signal and noise powers at the input, while the denominator corresponds to the same ratio but at the output. Note that the noise power at the output has two terms, one due to the input $G_A(f)N_i(f)$ and one due to the 2-port itself, $N_{p,o}$. If this last term were zero, i.e., if the 2-port were noiseless, the noise factor would be 1. (2.32) can be simplified to:

$$F(f) = 1 + \frac{N_{p,o}(f)}{G_A(f)N_i(f)} = 1 + \frac{N_{p,i}(f)}{N_i(f)} \tag{2.33}$$

$N_{p,i}$ is the noise power generated by the 2-port and reported to its input. The noise generated inside a 2-port can be represented by the equivalent input noise voltage $v_{n,i}$ and the equivalent input noise current $i_{n,i}$, as shown in figure 2.11. The source has a resistance R_S that generates a noise voltage $v_{n,S}$.

The noise current source can be transformed into a voltage by multiplying it by the source impedance. The equivalent input noise voltage, considering the source transformations of appendix C, becomes:

$$v'_{n,i} = v_{n,i} + R_S i_{n,i} \tag{2.34}$$

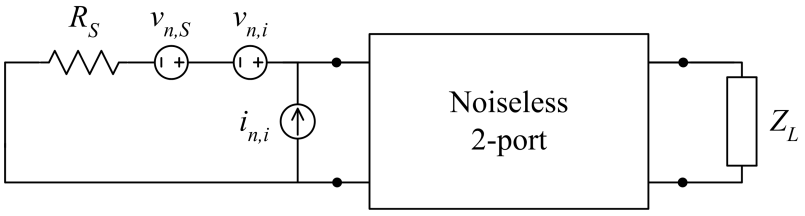

Figure 2.11: 2-port circuit block with equivalent noise sources.

The input noise power spectral density due to the 2-port is determined by the Wiener-Khintchine theorem (2.29):

$$N_i(f) = N_{v_{n,i}}(f) + R_S^2 N_{i_{n,i}}(f) \tag{2.35}$$

$N_{v_{n,i}}$ and $N_{i_{n,i}}$ are the power spectral density due to the 2-port input noise voltage and current respectively. The noise factor is finally:

$$F(f) = 1 + \frac{N_i(f)}{N_S(f)} \tag{2.36}$$

where $N_S(f)$ is the power spectral density of the noise generated by the source resistance R_S.

2.4.3 Cascaded Systems

A wireless system can be analyzed as a cascade of 2-ports, as represented in figure 2.12. The equations of the noise factor F and the IIP_3 of the cascade, give an idea of the relative importance of the different 2-ports on the overall performance.

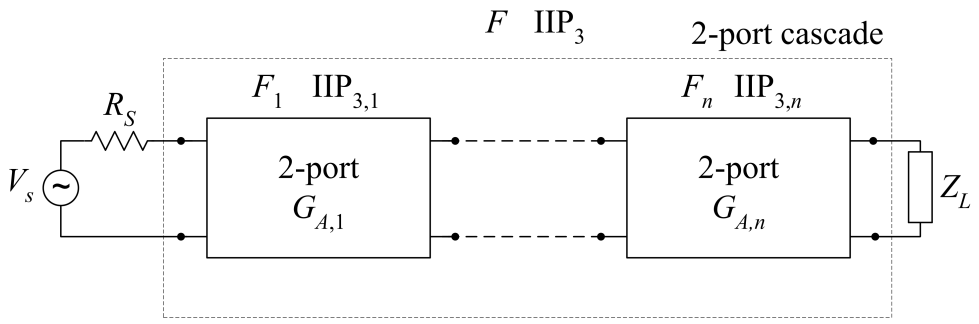

Figure 2.12: Cascade of 2-ports.

The noise factor referred to the input of the first block is [3, 36, 50]:

$$F = F_1 + \frac{F_2 - 1}{G_{A1}} + \frac{F_3 - 1}{G_{A2}G_{A1}} + ... + \frac{F_n - 1}{\prod_{i=1}^{n} G_{Ai}} \tag{2.37}$$

This is known as Friis Law, and shows that the gain of the first blocks reduces the influence of the noise from last blocks, meaning that the first blocks have a greater contribution to the overall cascade noise factor.

The IIP_3 equation for the cascade of figure 2.12 is [3]:

$$\frac{1}{\text{IIP}_3} = \frac{1}{\text{IIP}_{3,1}} + \frac{G_{A1}}{\text{IIP}_{3,2}} + \frac{G_{A1}G_{A2}}{\text{IIP}_{3,3}} + ... + \frac{\prod_{i=1}^{n} G_{Ai}}{\text{IIP}_{3,n}} \tag{2.38}$$

The conclusion for linearity is the opposite of that for noise; i.e., the last cascade blocks have more influence on IIP_3 than the first ones. Thus, from (2.37) and (2.38) it is concluded that the 2-ports located at the beginning of the cascade have more influence on the noise performance, while the last ones are more relevant for the linearity performance. As the LNA is the first 2-port of the cascade, its'noise factor is a more important specification than linearity.

2.4.4 Noise Sources

Several noise sources are identified in electronic components. The most important for RF design are thermal noise, flicker noise and shot noise.

Thermal Noise

Thermal noise occurs because thermally excited electrons, when traveling between two points of a conducting material, have a brownian movement due to its collisions within the fixed atoms [53, 54]. This phenomenon produces voltage fluctuations at the device terminals. The noise power in a conductor is independent of the material and frequency, and depends only on the temperature and resistance. At thermal equilibrium, the noise power spectral density is [47]:

$$N(f) = 4k_B TR \tag{2.39}$$

k_B is the Boltzmann constant[2] ($k_B = 1.380 \times 10^{-23}$ JK^{-1}), R is the resistance and T the absolute temperature in Kelvin [K].

Flicker Noise or $1/f$ Noise

Two theories are found in literature to explain flicker noise [47, 48, 53, 55]:

- The **carrier number fluctuation theory** explains the flicker noise as the random trapping and release of charges in the oxide near the Si-SiO_2 interface, which causes surface potential variations. This affects the channel carrier density and, consequently, the current flowing in the transistor channel.
- The **mobility fluctuation theory** explains flicker noise as a bulk mobility fluctuation.

Flicker noise is proportional to the inverse of frequency, and that is why this noise is also known as $1/f$ noise. This type of noise is more relevant for mixers that perform down-conversions. As the LNA works at high frequencies, flicker noise is negligible in comparison with other noise sources [53].

Shot Noise

Electrical current is the result of a flow of discrete electrical charges - electrons. The electrical current, at a certain section, has a discrete fluctuation which is a multiple of a minimum value - the electron charge q ($q = 1.602176 \times 10^{-19}$ C) [54]. There are two conditions that should be verified for the occurrence of shot noise:

- flow of current through a device;
- existence of a potential barrier through which the electrons jump.

The second occurs in p-n junctions and the shot noise results from the randomness of the time of arrival of one unit charge to the boundary of the barrier. The noise power spectral density of shot noise is [2, 55]:

$$N(f) = 2qI_{\mathrm{DC}} \tag{2.40}$$

[2]The Boltzmann constant is represented in this thesis with an indice B to distinguish it from the transformer magnetic coupling coefficient represented by k.

where q is the electron charge and I_{DC} is the DC current that flows through the device.

2.4.5 Noise in Transistors

Noise in MOS Transistors:

For LNA design, two noise sources are considered in MOS transistors: the thermal noise generated in the gate resistance R_g and represented by a voltage source v_{n,R_g}, and the thermal noise generated by the channel admittance g_{d0} and represented by a current source $i_{n,d}$; both sources are represented in figure 2.13.

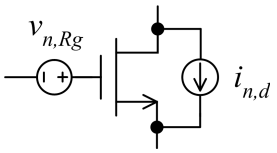

Figure 2.13: MOS transistor noise sources for RF design.

The noise power spectral densities of the two noise sources are respectively [53]:

$$\begin{cases} N_{R_g}(f) = 4k_B T R_g \\ \\ N_{i_d}(f) = 4k_B T \gamma g_{d0} \end{cases} \tag{2.41}$$

where g_{d0} is the zero-bias drain conductance and is related with the transistor transconductance g_m by a constant α ($g_m = \alpha g_{d0}$). For long channel transistors $\alpha = 1$ [47, 56]. γ is a (dimensionless) bias dependent factor (γ is 2/3 for long channel transistors and higher for short channel transistors) [56]. The equivalent input noise sources v_n and i_n, in figure 2.14, are [41]:

$$\begin{cases} v_n = v_{n,Rg} + \dfrac{1}{g_m}\left(1 + \dfrac{R_g}{Z_{gs}}\right) i_{n,d} \\ \\ i_n = i_{n,d} \end{cases} \tag{2.42}$$

where Z_{gs} is the impedance due to the gate-source capacitance.

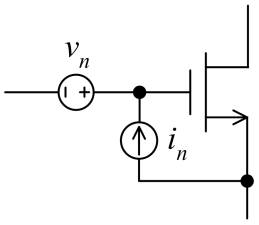

Figure 2.14: Equivalent input noise sources in a MOS transistor.

Noise in Bipolar Transistors:

In a BJT, there are the following noise sources: the thermal noise voltage v_{n,R_b} produced by the base resistance R_b, the base shot noise current $i_{n,b}$ and the collector shot noise current $i_{n,c}$. These noise sources are represented in figure 2.15:

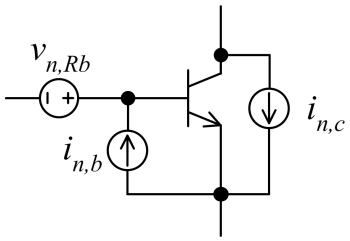

Figure 2.15: BJT noise sources for RF design.

The represented noise sources have the following noise power spectral noise densities [57]:

$$\begin{cases} N_{R_b}(f) = 4k_B T R_b \\ \\ N_{I_B}(f) = 2qI_B \\ \\ N_{I_C}(f) = 2qI_C \end{cases} \tag{2.43}$$

where R_b is the base resistance of the transistor and I_B and I_C are, respectively, the DC base current and the DC collector current. It is possible to determine the equivalent transistor input current and voltage noise sources in accordance with figure 6.25:

$$\begin{cases} v_n = v_{n,R_b} + \dfrac{1}{g_m}\left(1 + \dfrac{R_b}{Z_{be}}\right) i_{n,c} \\ \\ i_n = i_{n,b} + \dfrac{1}{g_m Z_{be}} i_{n,c} \end{cases} \tag{2.44}$$

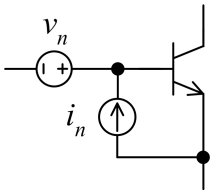

Figure 2.16: BJT with equivalent input referred noise sources.

where Z_{be} is the base-emitter capacitance.

2.5 Integrated Inductors and Transformers

This section gives an overview of integrated inductors and transformers. It starts with a discussion about inductors realized in integrated technologies. After, a generic inductor model, using lumped element models is presented and its most relevant limitations are discussed. Finally, the realization of integrated transformers using different topologies is shortly discussed.

2.5.1 Integrated Inductors

An inductor is usually realized as a coil of conducting material, which generates a magnetic field H when current i passes through it. The inductance L is defined by the magnetic flux Ψ generated by the current i, where Ψ is [58]:

$$\Psi = Li \tag{2.45}$$

L depends only on the circuit geometry and magnetic field permittivity.

In an integrated circuit, an inductor can be as a lumped element when implemented with one or several turns of metal layers [59]. Another implementation consists on using transmission lines; however, integrated circuits are not long enough for the required lengths [60].

As the number of metal layers is limited, the preferred geometry is the spiral coil, which minimizes the number of metal layers to two: one for the coil itself and one for the connection of the inner spiral point. The spirals can be circular, square or polygonal. The square geometry is not the most area efficient; however it is the simplest to implement and one of the simplest to model [2, 61].

In figure 2.17 the 2-D view of a spiral square inductor in a silicon process is represented, and in figure 2.18 the 3-D view is shown. The following design parameters are indicated in figures 2.17 and 2.18 [62]:

- external diameter d_{out};
- edge-to-edge spacing between adjacent turns s;
- turn metal width w;
- number of turns n_{turn};

- distance between the metal layer and the substrate a.

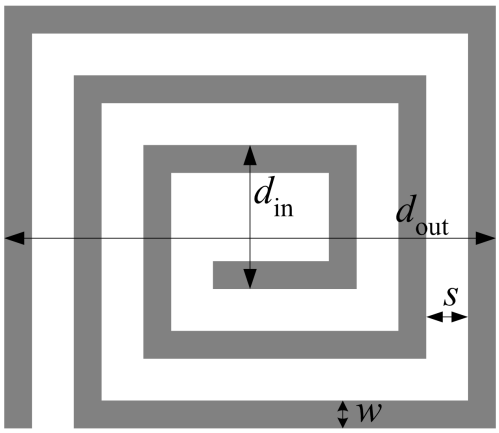

Figure 2.17: 2-D view of an integrated inductor.

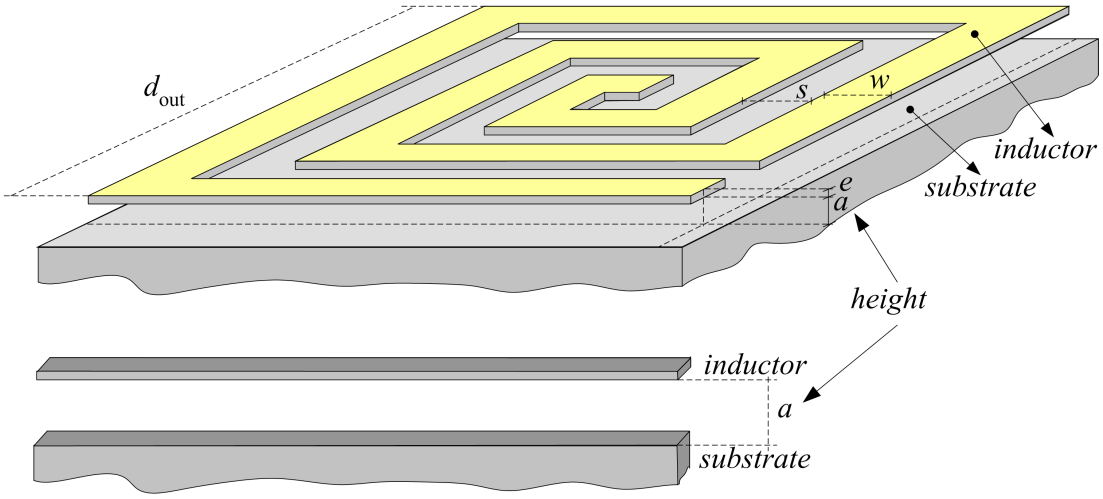

Figure 2.18: 3-D view of an integrated inductor.

The metal thickness e is a technology parameter that cannot be dimensioned by the designer.

In figure 2.19 the equivalent single-π model of an integrated inductor is represented. It includes the following elements [2, 63, 64]:

- series inductance L;
- coil series resistance R_s;
- inductor-substrate capacitance C_{ox};
- substrate capacitance C_{si};

- substrate spreading resistance R_{si}.

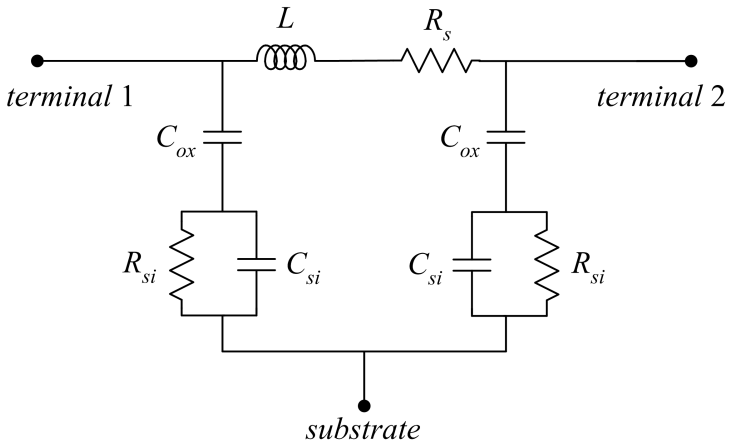

Figure 2.19: π circuit model of an integrated spiral inductor.

The effect of the inter-turn fringing capacitance is usually small because the adjacent turns are almost equipotential - the wave length is much larger than the inductor dimensions [65].

Much work was done in order to determine the inductor model elements. The first reported work (widely referenced) about the inductance determination of a square spiral inductor is given in [61]; however this method does not provides simple equations. One simple equation to determine an approximation of the inductance value can be found in [2]:

$$L \approx \mu_0 r n^2 \tag{2.46}$$

where μ_0 is the air magnetic constant ($\mu_0 = 4\pi \times 10^{-7}$ NA^{-2}), n is the number of turns and $r = d_{\text{out}}/2$ is the radius. More complex and more approximate equations can be found. One, only applicable to square spirals, is [66]:

$$L \approx \frac{2\mu_0 n^2 d_{\text{avg}}}{\pi}\left(\ln\frac{2.067}{\rho} + 0.178\rho + 0.125\rho^2\right) \tag{2.47}$$

where d_{avg} is the arithmetic mean of the inner d_{in} and outer diameters d_{out} and ρ is

$$\rho = \frac{d_{\text{out}} - d_{\text{in}}}{d_{\text{out}} + d_{\text{in}}} \tag{2.48}$$

Nowadays inductances are determined for any geometry, using electromagnetic simulators that solve Maxwell's equations by computational methods [67].

Equations for other model parameters can also be found in literature. The series resistance is given by [2]:

$$R_s = \frac{l}{w\sigma\delta(1 - e^{-t/\delta})} \tag{2.49}$$

where σ is the metal conductivity, l, w and t are, respectively, the total length, the width and the thickness of the winding, and δ is the skin effect parameter

$$\delta = \sqrt{\frac{2}{\omega\mu_0\sigma}} \tag{2.50}$$

The inductor-substrate capacitance C_{ox} is [2]:

$$C_{\text{ox}} = wl\frac{\varepsilon_{\text{ox}}}{t_{\text{ox}}} \tag{2.51}$$

The product wl is the winding metal area, ε_{ox} is the oxide permittivity and t_{ox} is the oxide thickness measured from the substrate to the winding.

Integrated silicon technologies are not optimized for inductor design. They have typically a limited number of metal layers and the thickness between them is not controllable, limiting the inductors optimization. Besides, the low substrate resistance degrades inductances and the silicon cost proportional to area also demands a reduction in the number of inductors, due to their low inductance per square unit in comparison to the inductances required for design. Thus, the inductor design results from the compromise between these constrains. Some practical design guidelines of an integrated inductor are given in the following [2, 60].

Practical Considerations on Integrated Inductor Design:

- The use of the top metal layer decreases simultaneously the inductor series resistance R_s and the oxide capacitance C_{ox}. R_s is lowered because the top metal layer is in some technologies, thicker than the others and C_{ox} is minimized because the top layer is further away from the substrate.

- In a multilevel metal process it is possible to use different metal layers to increase the inductance value and simultaneously optimize the inductor area.

- It is possible to connect two or more metal layers, by using vias, to lower the series resistance. The penalty is an increase in oxide capacitance, due to the use of lower metal layers.

- If the inductor is placed over a doped substrate, the magnetic field penetrates into the substrate, inducing loop currents that degrades the self inductance of the spiral inductor [65]. To prevent the electric field from penetrating the substrate a patterned ground shield can be used. The shield has to be patterned to avoid the magnetically induced eddy currents to form in the substrate and the patterned slots should be sufficiently narrow to prevent the vertical electric field to penetrate the substrate. One trade-off is an increase in the inductor substrate capacitance because of the reduction of the effective oxide thickness [62]. In figure 2.20 a possible patterned ground shield is presented.

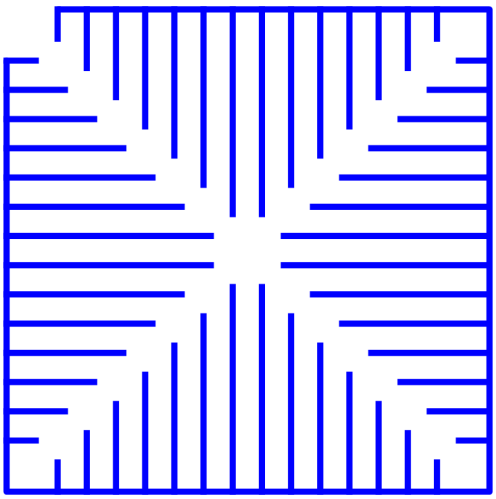

Figure 2.20: 2-D view of a patterned ground shield.

If two inductors are close to each other, there is magnetic coupling between them that should be minimized. However, this magnetic coupling can also be used to design integrated transformers, as described next.

2.5.2 Integrated Transformers

Integrated transformers are realized using two spiral inductors magnetically coupled. Different transformer configurations, can be obtained according to the inductors design and relative position between the two inductors. The most common configurations are [62]:

- tapped transformer,
- interleaved transformer, and
- stacked transformer.

They are described next.

2.5.2.1 Common Integrated Transformer Configurations

Tapped Transformer:

The tapped transformer, represented in figure 2.21, has both windings in same metal layer, which is suitable for technologies with few metal layers. This configuration also minimizes the capacitance between windings. The magnetic coupling coefficient is low [68].

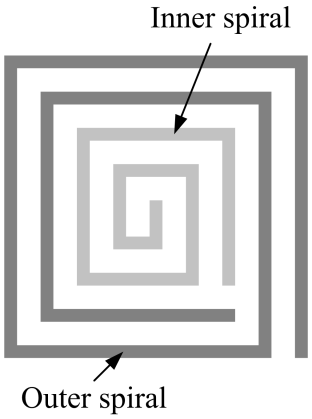

Figure 2.21: 2-D view of a tapped transformer.

Interleaved Transformer:

The interleaved transformer is shown in figure 2.22. Both windings are realized in the same metal layer. The capacitance between windings is higher than in the tapped transformer, due to the interleaving. It is also characterized by a weak magnetic coupling and less flexibility in setting the number of turns and relative size of the two windings.

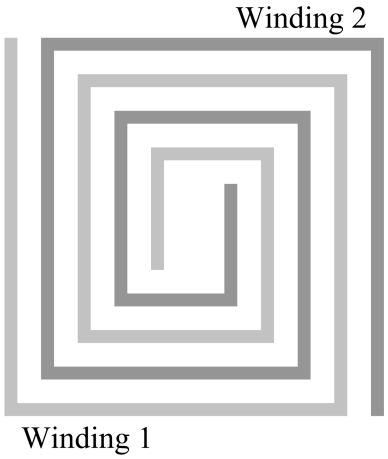

Figure 2.22: 2-D view of an interleaved transformer.

Stacked Transformer:

Another configuration for an integrated transformer consists of stacking two spiral inductors as represented in the 3-D view in figure 2.23. This configuration requires more metal layers than the two configurations presented before; however, it achieves higher magnetic coupling. The magnetic coupling coefficient can be controlled by displacing one of the windings relatively to the other, as represented in figure 2.24. This reduces the capacitance between windings.

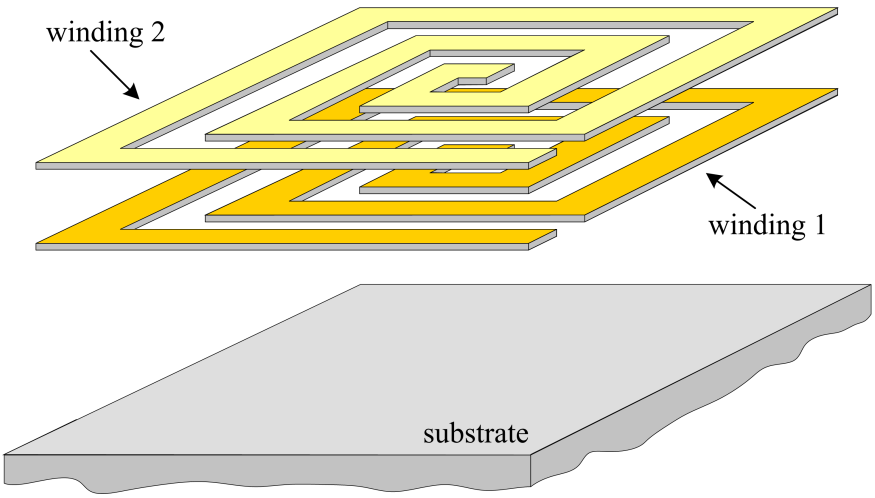

Figure 2.23: 3-D view of a stacked transformer.

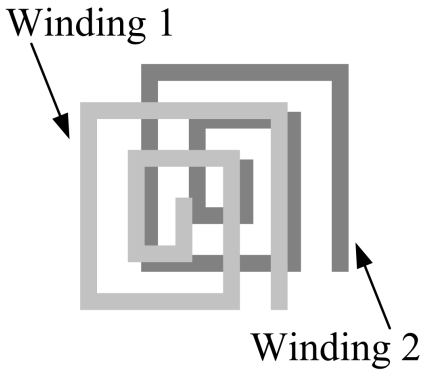

Figure 2.24: 2-D view of a stacked transformer in which the windings are shifted to control the magnetic coupling coefficient.

2.5.2.2 Transformer Equations

An ideal transformer is described by the following equations:

$$\begin{cases} v_1 = nv_2 \\ i_2 = ni_1 \\ v_1 i_1 = v_2 i_2 \end{cases} \tag{2.52}$$

v_m and i_m are respectively the voltage and current at port m. The ideal transformer symbol of figure 2.25 is used from now on.

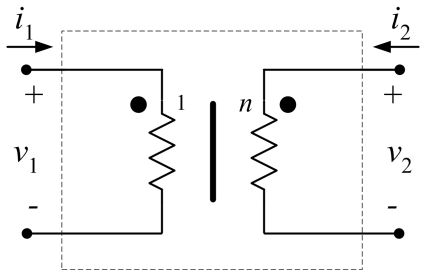

Figure 2.25: Symbol of an ideal transformer.

Practical integrated transformers are implemented with two windings magnetically coupled. The magnetic coupling coefficient k varies between zero, for independent inductors, and one, for perfect magnetic coupling. A transformer considering winding inductances is represented in figure 2.26. L_{11} and L_{22} are, respectively, the self-inductances of windings 1 and 2.

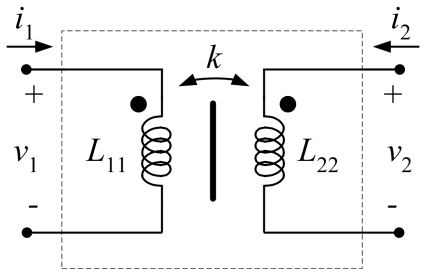

Figure 2.26: Transformer 2-port symbol considering winding inductances L_{mm}.

The equations that describe the transformer of figure 2.26 are:

$$\begin{cases} V_1(s) = sL_{11}I_1(s) + sL_M I_2(s) \\ \\ V_2(s) = sL_M I_1(s) + sL_{22}I_2(s) \end{cases} \tag{2.53}$$

where $L_M = k\sqrt{L_{11}L_{22}}$ is the mutual inductance, which has an upper limit $\sqrt{L_{11}L_{22}}$, when $k = 1$ [69]. Using (2.53), and matrix **H** definition of appendix A, it can be shown that the 2-port **H** matrix of this transformer is

$$\mathbf{H}_T = \begin{pmatrix} sL_{11}(1-k^2) & \dfrac{1}{n} \\ \\ -\dfrac{1}{n} & \dfrac{1}{sL_{22}} \end{pmatrix} \tag{2.54}$$

where n is

$$n = \frac{1}{k}\sqrt{\frac{L_{22}}{L_{11}}} \tag{2.55}$$

This matrix representation is used in feedback systems when analyzed using matrices.

2.6 Conclusions

This chapter reviews the most important theoretical aspects of an LNA design. LNAs are part of modern wireless receivers and are responsible for the amplification of signals received from the antenna. The amplified signal is usually down-converted by a mixer connected ahead of the LNA. The importance of the LNA input impedance matching on the maximization of the power transfer from the antenna is emphasized. The LNA should have enough gain to amplify the weak RF signals received by the antenna and reduce the noise influence of other receiver blocks - Friis Law. The LNA should also generate low noise to avoid a degradation of the SNR of the input signal. Finally, some aspects of the technological implementation of the LNA are discussed, mainly concerning integrated inductors and transformers.

Chapter 3

Overview of Low Noise Amplifiers

3.1 Introduction

This chapter is an overview of LNA design. LNAs are characterized by three main parameters: input impedance, gain, and noise figure. Typically, the input impedance should have a precise value, while the gain should be maximized with the minimum noise addition. Several circuits achieve a precise input impedance; however, not all are suitable for LNA design.

LNA circuits have typically an amplifying block and a resonant network to achieve the required input impedance. These two blocks may form sometimes a single loop feedback network. Single loop feedback circuits are studied in the literature and an overview is presented in this chapter. Double loop feedback (DLF) circuits are studied in this chapter to evaluate their suitability to LNA design.

The major LNA parameters are discussed in section 3.2 and the typical LNA topologies are presented in section 3.3. The common-source LNA using inductive degeneration is the most widely used, and it is described in more detail in section 3.4. Double loop feedback topologies are described in section 3.5. In section 3.6 some final remarks are discussed.

3.2 LNA Basic Concepts

In the LNA design there is a trade-off between its main specifications [9]:

- input impedance matching;
- high gain in the bandwidth of interest;
- low noise factor;
- high frequency operation;
- bandwidth.

The ideal LNA has a finite input impedance matched to the output impedance of the preceding block, in order to maximize the power transfer of the received high frequency signal. This signal should be amplified without noise addition. The LNA has a bandwidth specification and it is often included in a portable system which limits the power consumption.

Usually, the output impedance of the block preceding the LNA is purely resistive and equal to 50 Ω [2]; thus, the LNA input impedance should also be 50 Ω, to prevent undesired reflections, and, consequently, to maximize the signal power transfer. The LNA gain is important to amplify the typically low received signals. A low noise factor is another important characteristic because the LNA is usually at the beginning of the RF receiver chain, so all the noise that it produces is amplified by the whole chain. Linearity has a lower priority in comparison with other characteristics: it is more important for the blocks situated at the end of the RF system chain, because they deal with larger signals. Concerning bandwidth, LNAs can be narrowband, multi-band or wideband.

The most important LNA specifications are the input impedance, the noise factor and the (voltage or current) gain, and few circuits can satisfy these specifications simultaneously at the required frequency band. In the following sections, an overview on the most used LNA topologies is presented.

3.3 LNA Topologies

Of the three most important LNA characteristics (input impedance, noise factor and gain), only the input impedance should have a precise value; i.e., it should equal the output impedance of the preceding block. The noise factor should be below a specific value and the gain should be above a specific value. Thus, LNAs are designed to have a precise input impedance with high gain and low noise figure.

LNAs can be implemented in several technologies, and in this thesis two technologies are considered: MOS and bipolar transistors. MOS circuits will be considered here, and the simple transistor incremental model in figure 3.1 will be adopted. It includes only the transconductance g_m and the gate-source capacitance C_{gs}. Other elements, like the gate resistance R_g and the gate-drain capacitance C_{gd} produce second-order effects that are only relevant for more detailed analysis, and are considered later in this chapter.

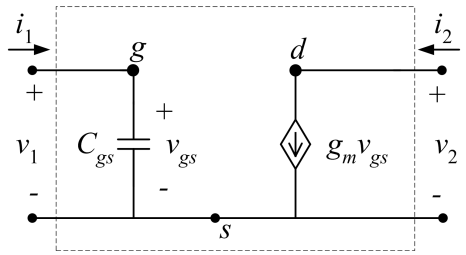

Figure 3.1: MOS incremental π model.

Several forms of obtaining CMOS LNAs are presented next.

3.3.1 LNA using Input Resistor

The simplest form of obtaining real input impedance is to place a resistor in parallel with the amplifying block, as shown in figure 3.2 [56].

The input impedance Z_{in} is $R_{S1}//Z_1$. If $Z_1 \gg R_{S1}$, the input impedance Z_{in} is approximately equal to R_{S1}, and there is input impedance matching, if $R_{S1} = R_S$.

Assuming that the 2-port is noiseless, the only noise contribution is the thermal

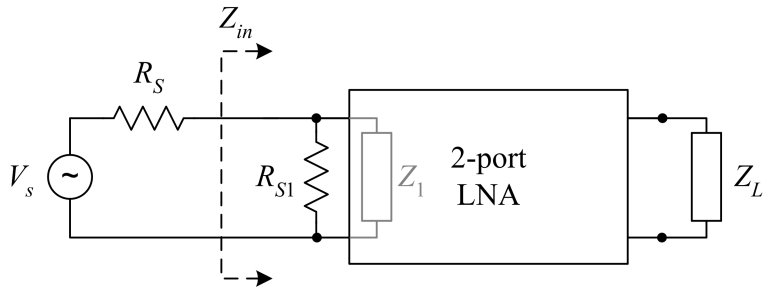

Figure 3.2: LNA with resistive input power matching.

noise generated by R_{S1}. The noise factor is [2, 56]:

$$F = \frac{N_S + N_{S1}}{N_S} = \frac{R_S + R_{S1}}{R_S} = 2 \tag{3.1}$$

where N_S and N_{S1} are the noise power spectral densities due to the source resistance R_S and the input matching resistance R_{S1}, respectively. (3.1) shows that having a resistor in parallel with the LNA input impedance, of a value equal to the source impedance, leads to a noise figure penalty of 3 dB. A 3 dB noise figure is used as a boundary, below which, the LNA has a low NF.

3.3.2 Common-Gate LNA

The common-gate LNA, shown in figure 3.3, uses the transistor transconductance to realize the LNA input impedance matching [56, 70–73]. Replacing the common-gate transistor by the incremental model of figure 3.1, leads to:

$$Z_{in} \approx \frac{1}{g_m} \tag{3.2}$$

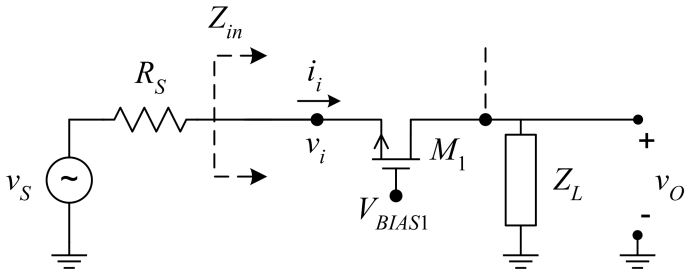

Figure 3.3: Incremental model of the common-gate LNA (biasing not represented).

Concerning the noise analysis and considering the CMOS transistor noise sources (2.41), the noise power spectral density due to the common-gate transistor referred

at its input can be determined as:

$$N_i(f) = 4k_BT(R_g + R_S^2\gamma g_m) \tag{3.3}$$

R_g is the gate resistance of M_1 and γ is a bias dependent factor (γ is 2/3 for long channel transistors and higher for short channel transistors [56]). Using (3.3) and (2.41), the noise factor is:

$$F = \frac{N_S + N_i}{N_S} = 1 + \frac{R_g}{R_S} + R_S\gamma g_m \tag{3.4}$$

Assuming that $R_g = 0$ and $\gamma = 2/3$, this LNA topology has a minimum noise factor of 5/3; i.e., $NF \approx$ 2.2 dB.

One limitation of this topology is that the voltage gain cannot be optimized because g_m is fixed to ensure the input impedance matching.

3.3.3 Common-Source LNA with Inductive Degeneration

Another LNA topology, first proposed in [56], is represented in figure 3.4: it is a common-source stage with inductive source degeneration.

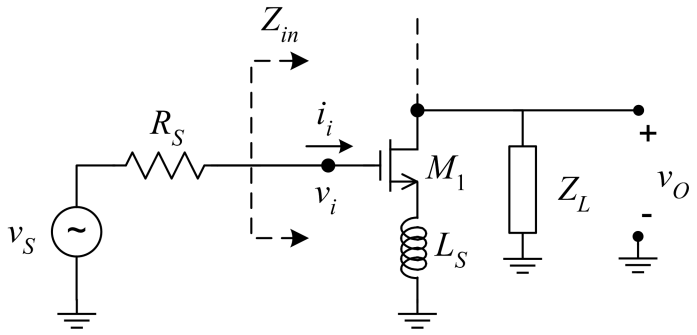

Figure 3.4: Common-Source LNA using inductive degeneration (biasing of M_1 not represented).

From the incremental model in figure 3.5, the input impedance Z_{in} is:

$$Z_{in} = \frac{g_m L_S}{C_{gs}} + \frac{1}{sC_{gs}} + sL_S \tag{3.5}$$

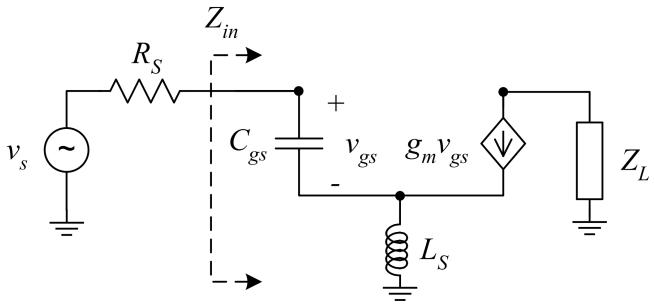

Figure 3.5: Incremental model of the common-source LNA using inductive degeneration.

The input impedance is real at the resonant frequency:

$$Z_{in} = \frac{g_m L_S}{C_{gs}} \qquad \text{at} \qquad \omega_0 = \frac{1}{\sqrt{L_S C_{gs}}} \tag{3.6}$$

The real part of the input impedance depends on three different parameters (g_m, C_{gs} and L_S) which are theoretically noiseless: this means that it is possible to achieve a real input impedance without addition of noise using this topology. The LNA gain is proportional to g_m, which can be maximized, while the values of C_{gs} and L_S are used to obtain the required input impedance. This is not possible in the common-gate LNA, where the maximization of g_m affects the input impedance.

3.3.4 LNA with Current Reuse

The LNA using current reuse is a variant of the common-source LNA using inductive degeneration. This topology, represented in figure 3.6, uses both PMOS and NMOS transistors in a common-source configuration with inductive degeneration. This topology achieves the same noise factor and the same transconductance of the single NMOS transistor common-source LNA using half the current consumption. However, this topology requires an higher voltage supply to feed the two stacked transistors. [74–76].

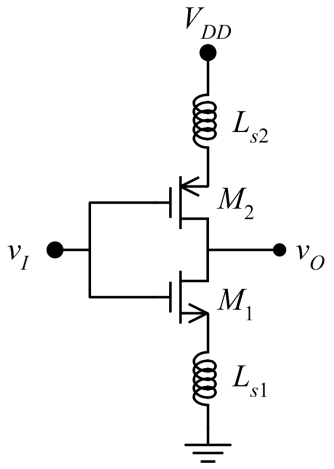

Figure 3.6: LNA using current reuse (biasing of M_1 and M_2 not represented).

3.3.5 LNA with Resistive Feedback

The LNA in figure 3.7 uses one resistor connected in a shunt-shunt feedback topology [77, 78]. The LNA input impedance, from the incremental model of figure 3.8, is:

$$Z_{in} = \frac{R_F + Z_L}{1 + g_m Z_L + (R_F + Z_L) s C_{gs}} \tag{3.7}$$

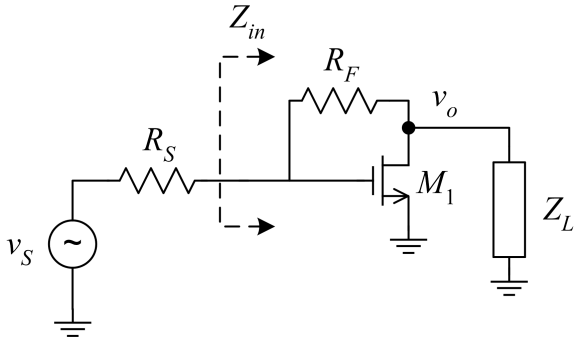

Figure 3.7: LNA with resistive feedback (biasing of M_1 not represented).

If the load impedance Z_L is high enough, Z_{in} simplifies to:

$$Z_{in} = \frac{1}{g_m + s C_{gs}} \tag{3.8}$$

For frequencies at which sC_{gs} is negligible in comparison with g_m, the input impedance is almost real and equal to $1/g_m$. Neglecting Z_L and C_{gs}, it can also be shown that the voltage gain is

$$A_v = \frac{v_o}{v_s} = \frac{1 - R_F g_m}{1 + R_S g_m} \tag{3.9}$$

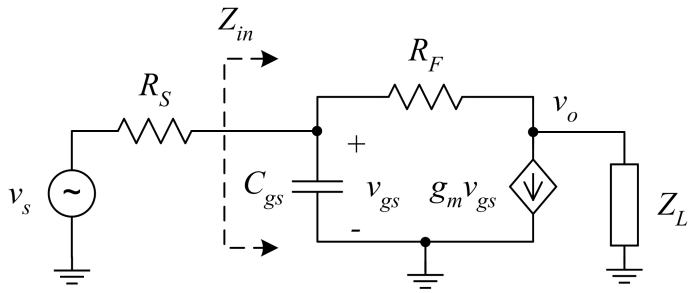

Figure 3.8: Incremental model of the LNA with resistive feedback.

If g_m is high enough, the voltage gain becomes

$$A_v \approx -\frac{R_F}{R_S} \tag{3.10}$$

The noise figure also benefits from the transistor g_m increase, but, as in the common-gate LNA, the maximization of g_m in order to improve the LNA voltage gain (3.9) affects the input impedance (3.8).

3.3.6 Discussion

Another LNA is the distributed LNA, based on transmission lines, which is out of the scope of this work, that is restricted to lumped element circuits. Typically distributed LNAs have higher power consumption than other circuits [79–82].

In the common-gate LNA and in the LNA using resistive feedback, the precise input impedance value relies on a precise value of g_m. This is a disadvantage because the gain maximization is not possible. For the remaining topologies (common source LNA with inductive degeneration, LNA with current reuse), the input impedance depends on three different parameters (g_m, C_{gs} and L_S), allowing gain optimization simultaneously with input impedance matching. The topology with the best noise performance is the common-source LNA topology with inductive degeneration (the noise performance of this topology is developed ahead in this chapter). This makes this topology the most widely chosen for LNA design . This is analyzed with more detail in the following section.

3.4 Cascode LNA with Inductive Degeneration

The common-source LNA using inductive degeneration is further studied in this section, due to its importance in the design of the multi-band LNA proposed in this thesis. This topology is presented in figure 3.4 and is claimed to be the LNA topology with better noise performance [56]. This topology was analyzed in last section considering a simple model, neglecting the gate-drain capacitance C_{gd} and the gate resistance R_g. This will be considered in the following analysis.

3.4.1 Effect of C_{gd}

Throughout the overview presented in section 3.3, the transistor model does not include the gate-drain capacitance C_{gd}. This capacitance creates a signal path from the output to the input, that degrades the LNA reverse isolation. Several techniques have been proposed to overcome this problem, and three of them are discussed next.

Transformer Feedback

The LNA proposed in [83] and represented in figure 3.9 uses one transformer to feed back part of the output signal in order to cancel the signal feed back through C_{gd}.

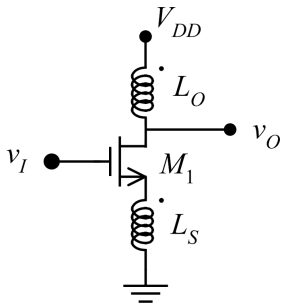

Figure 3.9: Transformer feedback LNA (biasing of M_1 not represented).

The use of the source inductor L_S coupled to the output inductor L_O leads to an input impedance different from that of the common-source LNA studied before [84]. Another trade-off is the transformer design and all concern on its parasitics.

Tuned Inductor Feedback

The LNA of figure 3.10, also proposed in [83], uses inductor L_f to resonate with C_{gd}. This technique requires an extra inductor and a large capacitor that leads to a die area increase. The use of a resonant inductor also affects the LNA resonant frequency.

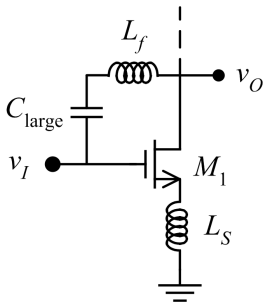

Figure 3.10: LNA using tuned inductor (biasing of M_1 not represented).

Cascode LNA

Another technique consists of using the cascode transistor M_2 of figure 3.11.

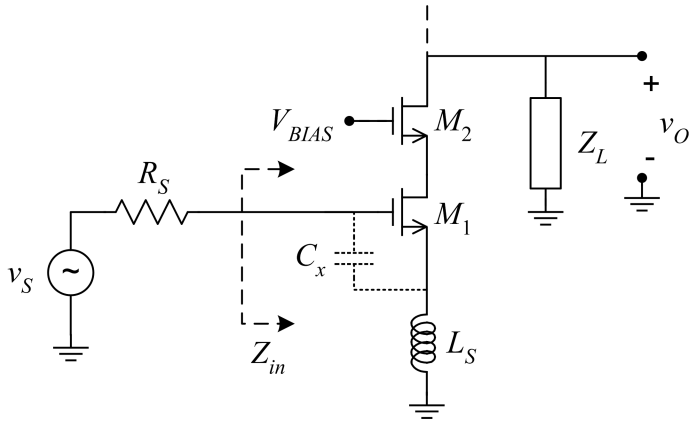

Figure 3.11: Cascode LNA (biasing of M_1 not represented).

Besides the advantage of reducing significantly the Miller effect due to C_{gd} of transistor M_1, the cascode circuit presents other advantages [85–89]:

- the output-input isolation is improved without significant power consumption increase;
- the LNA output impedance is increased;

- the noise interference of systems ahead of the LNA is reduced.

This LNA circuit requires a higher supply voltage than the last two; however, it has a much lower area. The bias voltage V_{BIAS} is usually equal to the supply voltage V_{DD} to prevent the use of another DC voltage.

3.4.2 Input Impedance and Noise Figure

The cascode LNA with inductive degeneration is represented in figure 3.11. The capacitor C_x is connected in parallel with C_{gs} of transistor M_1, and is used to add an extra variable to the circuit design. The incremental model of the cascode configuration formed by M_1 and M_2 is represented in figure 3.12. The input impedance is:

$$Z_{in} = \frac{g_{m1}L_S}{C_t} + \frac{1}{sC_t} + sL_S \tag{3.11}$$

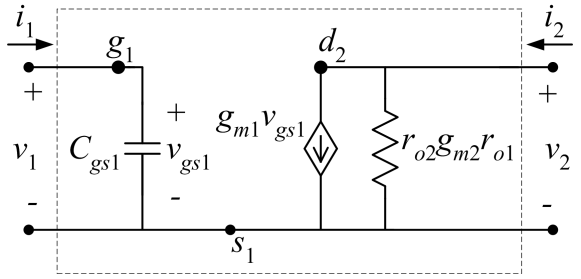

Figure 3.12: Cascode configuration incremental model.

where $C_t = C_{gs1} + C_x$. This amplifier has a real input impedance at its resonant frequency; i.e.,

$$Z_{in} = \frac{g_{m1}L_S}{C_t} \tag{3.12}$$

when

$$\omega_0 = \frac{1}{\sqrt{L_S C_t}} \tag{3.13}$$

Figure 3.13 represents the amplifier incremental model suitable for noise analysis, which includes only the transistor M_1 noise sources. The non-resistive passive elements are considered noiseless and the noise due to M_2 is considered negligible.

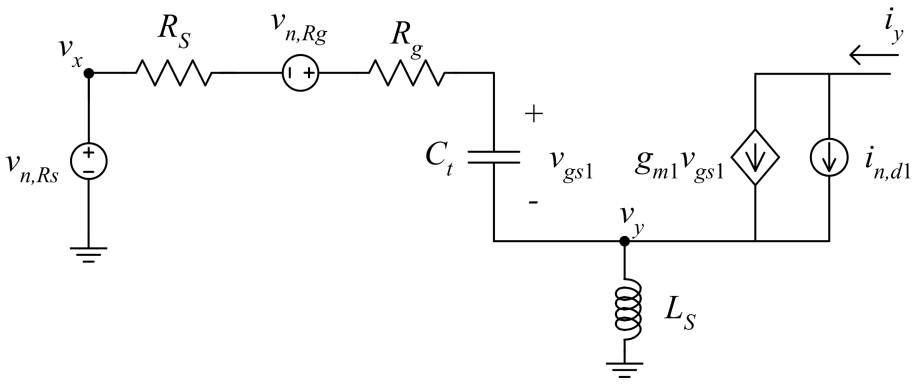

Figure 3.13: Incremental model of the degenerated cascode LNA with noise sources.

In the incremental model of figure 3.13, the transistor M_1 output resistance r_{o1} is considered high enough to be negligible. One way of determining the noise factor consists of transferring all noise sources to the LNA input. Considering the MOS equivalent input noise sources, described in section 2.4, the equivalent noise sources referred to the input, and in accordance with figure 3.14, are:

$$v_{n,i} \approx v_{n,R_g} + \left(A_v Z_S - \frac{1}{G_m} \right) i_{n,d} \tag{3.14}$$

where $G_m = i_y/v_x$ is the transconductance of the incremental model and $A_v = v_x/v_y$ is the voltage ratio between points x and y:

$$G_m(s) = \frac{i_y}{v_x} = \left(R_S + R_g + \frac{1}{Y_t} + Z_S + \frac{g_m L_S}{C_t} \right)^{-1} \frac{g_m}{Y_t} \tag{3.15}$$

$$A_v(s) = \frac{v_x}{v_y} = \frac{(R_S + R_g)Y_t + 1 + (g_{m1} + Y_t)Z_S}{(g_{m1} + Y_t)Z_S} \tag{3.16}$$

Y_t is the admittance due to C_t and Z_S is the admittance due to L_S.

The input noise power spectral density, using the Wiener-Khintchine theorem, is:

$$N_i(f) = N_{R_g} + \left| A_v Z_S - \frac{1}{G_m} \right|^2 N_{i_d} \tag{3.17}$$

and the noise factor, determined at the resonance frequency ω_0, assuming a matched input impedance $R_S = g_m L_S/C_t$, and $|G_m|^{-1} \gg A_v Z_S$, is:

$$F(\omega_0) = 1 + \frac{N_i(\omega_0)}{N_S(\omega_0)} \approx 1 + \frac{R_g}{R_S} + \frac{\gamma g_{d0}(R_S + R_g)^2 \omega_0^2 C_t^2}{R_S g_m^2} \tag{3.18}$$

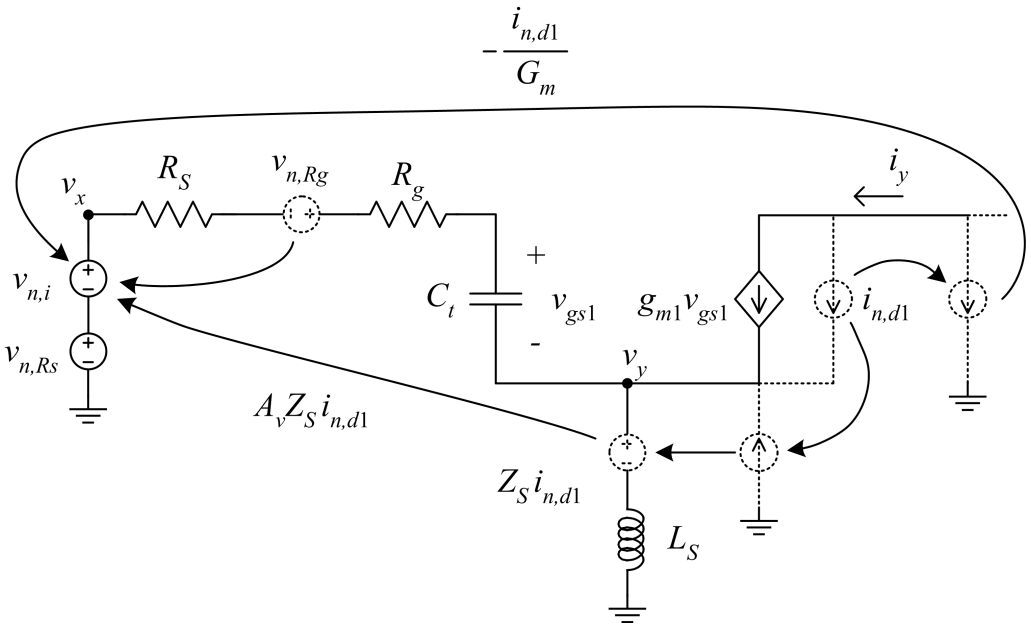

Figure 3.14: Incremental model of the degenerated cascode LNA with an input equivalent voltage noise source.

If $R_S \gg R_g$,

$$F \approx 1 + \gamma g_{d0} \frac{\omega_0^2 C_t^2 R_S}{g_m^2} \tag{3.19}$$

From (3.19), it is concluded that the noise factor improves (decreases) for technologies with higher transition frequencies f_t. The gate resistance R_g can be minimized by proper design, for example by multi-fingering of the transistor gate [2]. This topology has been widely studied [2, 3, 7, 8, 45, 56, 85, 86, 90–99].

3.5 Double Loop Feedback LNAs

3.5.1 Four Feedback Topologies

In section 3.3, some known LNA topologies are discussed and most of them use feedback in an implicit way. Feedback has several advantages like: better noise performance, gain insensitivity against parameter changes, precise control of input and output impedances, increased bandwidth and reduced non-linear distortion [43, 89, 100–102].

A feedback amplifier has an amplifying block A, which provides gain, and a feedback network β, which samples the output signal and feeds the result to the amplifying block input as shown in figure 3.15 [102–104]. If the feedback results in an output signal increase, it is called positive feedback (used in oscillator design), otherwise it is negative feedback (used in amplifier design) [43].

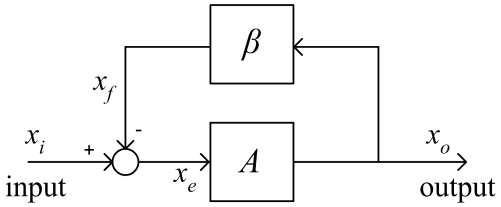

Figure 3.15: Block diagram of a feedback system.

The gain is

$$A_F = \frac{x_o}{x_i} = \frac{A}{1 + A\beta} \tag{3.20}$$

where $A\beta$ is the loop gain and β is the feedback factor. If $A\beta \gg 1$, A_F depends only on the feedback network:

$$\lim_{A \to \infty} A_F = \frac{1}{\beta} \tag{3.21}$$

In this situation, A_F is insensitive to the amplifying block variations, due to temperature, age or bias conditions. This leads to a common design methodology, that consists of designing the feedback network assuming that the amplifying block is designed to have a high gain. An ideal amplifying block can be represented by a nullor, which is a 2-port with infinite gain (voltage gain, current gain, transconductance

and transimpedance [41, 101]). The nullor chain matrix is:

$$\begin{bmatrix} v_1 \\ i_1 \end{bmatrix} = \begin{pmatrix} 0 & 0 \\ 0 & 0 \end{pmatrix} \begin{bmatrix} v_2 \\ -i_2 \end{bmatrix} \tag{3.22}$$

Four different feedback circuit configurations can be considered: series-series (figure 3.16), series-shunt (figure 3.17), shunt-series (figure 3.18) and shunt-shunt (figure 3.19).

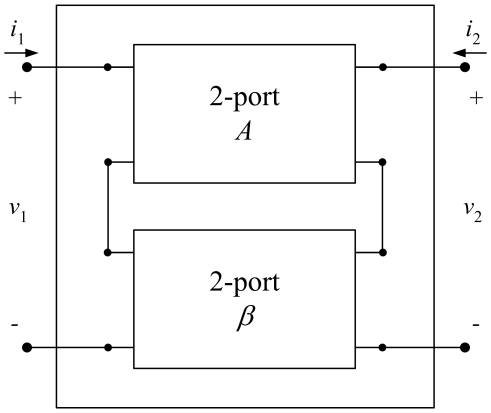

Figure 3.16: Series-series feedback.

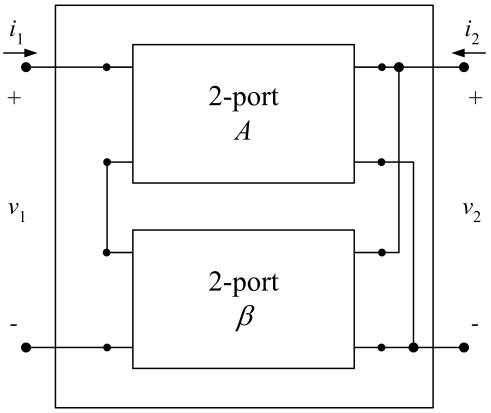

Figure 3.17: Series-shunt feedback.

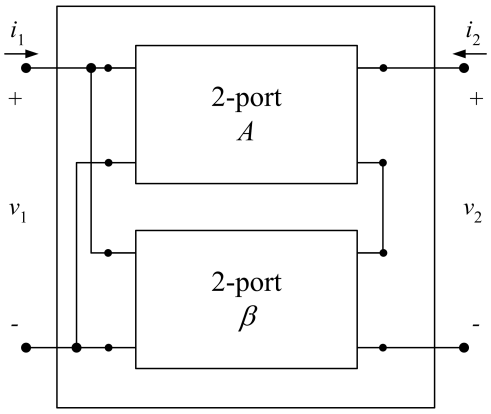

Figure 3.18: Shunt-series feedback.

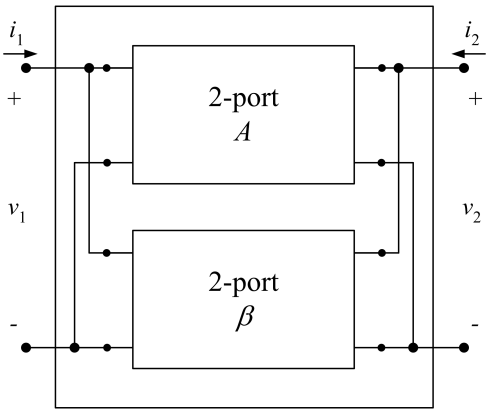

Figure 3.19: Shunt-shunt feedback.

For each feedback configuration, there is a matrix description that is the most suitable for describing the complete feedback system, and that consists on simply adding both 2-port matrices, as indicated in table 3.1 [43, 105]. The different matrices are defined in appendix A.

Table 3.1: Four feedback topologies.

Feedback configuration	Input comparison quantity	Output sampling quantity	Most suitable 2-port matrix
series-series	voltage	current	**Z**
series-shunt	voltage	voltage	hybrid **H**
shunt-series	current	current	hybrid **H'**
shunt-shunt	current	voltage	**Y**

3.5.2 Feedback Low Noise Amplifiers

During the LNA design, it is convenient to start by replacing the amplifying block by a nullor. Thus, it is possible to evaluate the performance limits of the feedback amplifier due only to the feedback network non-idealities. This allows hierarchization of the design process, by first designing the feedback network and then designing an amplifying block that approximates the nullor performance.

The passive elements used in the feedback block can be two terminal (resistors, capacitors, and inductors) or four terminal (transformers). Using one two-terminal element, two feedback configurations are possible: series-series and shunt-shunt feedback. Using transformers, the other two feedback configurations are also possible: series-shunt and shunt-series feedback. It is not recommended to use transformers in the series-series and shunt-shunt feedback configurations, because the transformer current-voltage ratio is not linear. In figures 3.20 to 3.23 the four different feedback configurations using a single element are represented.

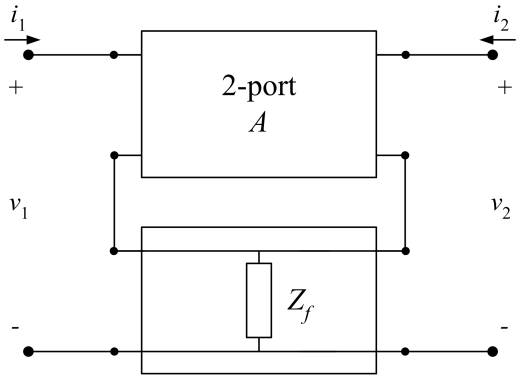

Figure 3.20: Series-series feedback with two-terminal element.

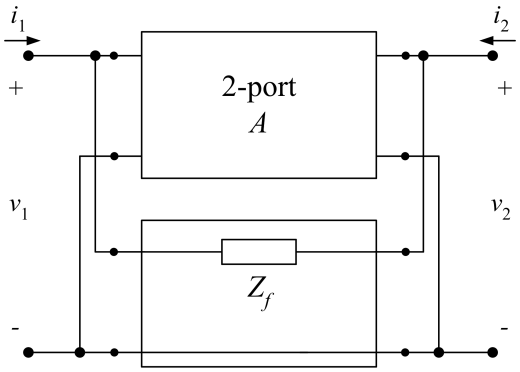

Figure 3.21: Shunt-shunt feedback with two-terminal element.

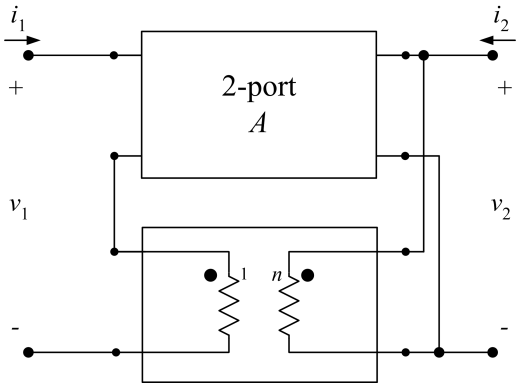

Figure 3.22: Series-shunt feedback with a transformer.

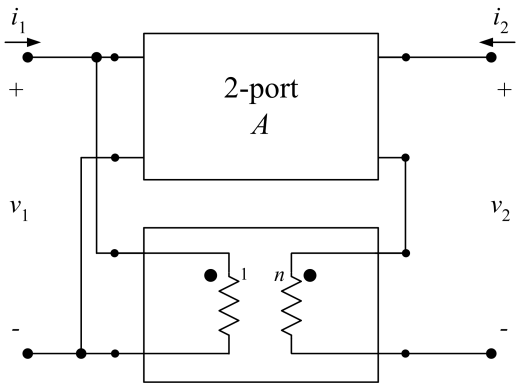

Figure 3.23: Shunt-series feedback with a transformer.

Consider now the amplifying block with finite input impedance Z_i, represented in figure 3.24.

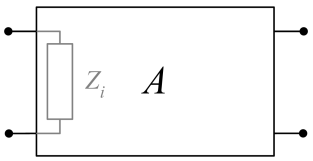

Figure 3.24: Amplifying block having finite input impedance.

The feedback amplifier input impedance is $Z_i(1+A\beta)$ for the input series connection (figures 3.20 and 3.22) and is $Z_i/(1+A\beta)$ for the input parallel connection (figures 3.21 and 3.23) [89]. If the amplifying block gain is infinite, it is not possible to obtain finite input impedances using a single loop feedback [23]. To obtain a finite and precise input impedance using a single loop, the amplifying block gain must be finite. This is what happens in the common-source LNA using either inductive degeneration or resistive feedback (discussed in section 3.3).

Since it is not possible to design an LNA using a single loop feedback if the amplifying block gain is infinite, double loop feedback is evaluated in the following.

3.5.3 Double Loop Feedback (DLF)

Consider the case where both feedback loops compare the same variable. In figure 3.25 a) current is compared and in figure 3.25 b) voltage is compared. If the amplifying block A is a nullor, in the first case $v_i = 0$, so the input impedance (v_i/i_i) is zero. In the second case $i_i = 0$; so the input impedance is infinite. Thus, it is not possible to obtain a finite input impedance using two feedback loops comparing the

same variable at the input.

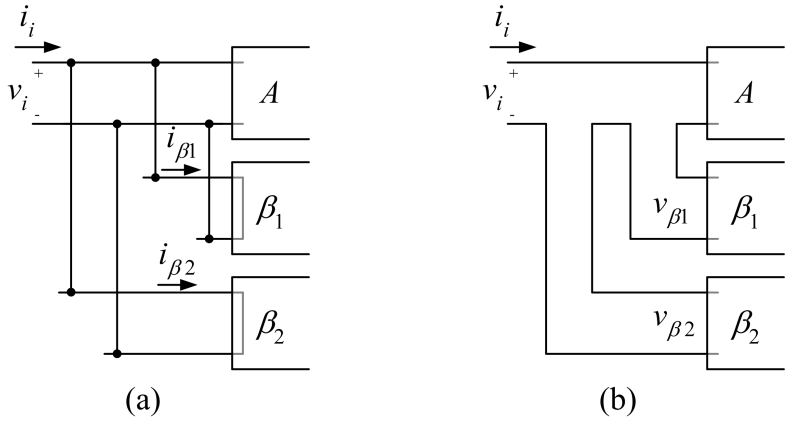

Figure 3.25: Two feedback loops, both comparing (a) current; or (b) voltage.

Consider now the comparison of different variables. First consider only DLF amplifiers having different variables sampled at the output. The different possibilities are represented in figure 3.26.

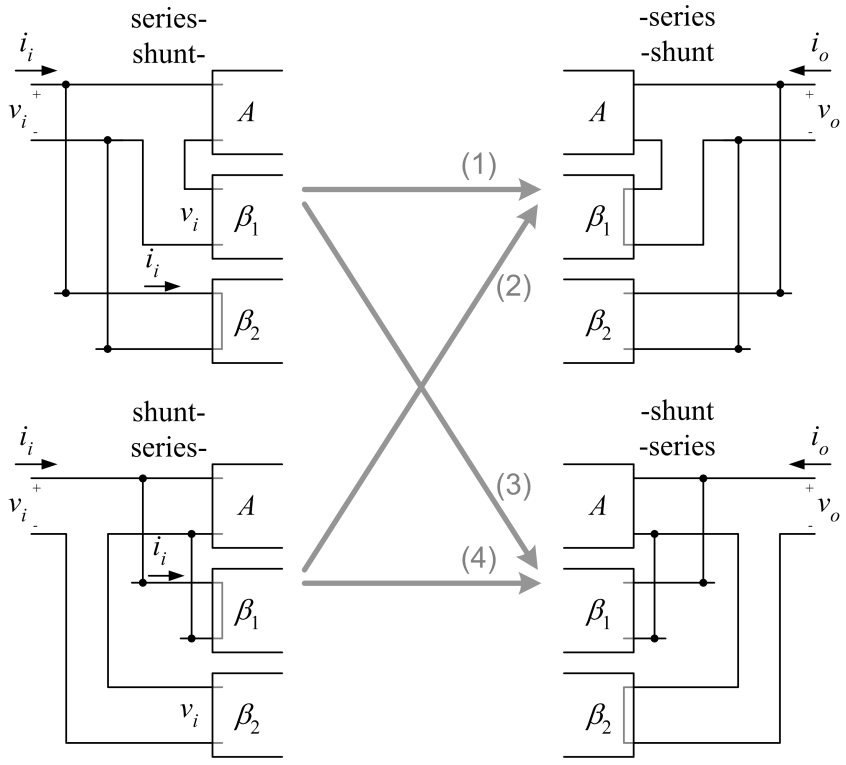

Figure 3.26: Double loop feedback amplifier sampling different variables and comparing different variables.

Table 3.2: Input impedance for the DLF amplifier combinations of figure 3.26.

Topology in figure 3.26	Feedback loops	Input impedance
(1)	series-series inside shunt-shunt	$\frac{\beta_1}{\beta_2}\frac{i_o}{v_o}$
(2)	shunt-series inside series-shunt	$\frac{\beta_2}{\beta_1}\frac{i_o}{v_o}$
(3)	series-shunt inside shunt-series	$\frac{\beta_1}{\beta_2}\frac{v_o}{i_o}$
(4)	shunt-shunt inside series-series	$\frac{\beta_2}{\beta_1}\frac{v_o}{i_o}$

The input impedance of the different DLF amplifiers obtained is listed in table 3.2. In all cases the input impedance is not independent of the output load (v_o/i_o).

Consider now DLF amplifiers sampling the same variable and comparing different variables. In figure 3.27 the different amplifier combinations are presented.

The input impedance of the DLF amplifier combinations of figure 3.27 is listed in table 3.3.

It is concluded that it is now possible to have a finite input impedance, independent of the output load. Thus, the feedback amplifier must have the same quantity sampled at the output and different quantities at the input [23, 106]. The only DLF amplifiers that are suitable for LNA design are those having the following feedback loops:

- shunt-series and series-series;
- shunt-shunt and series-shunt.

These DLF amplifiers will be studied considering an ideal amplifying block, but replacing the feedback loops by circuit elements.

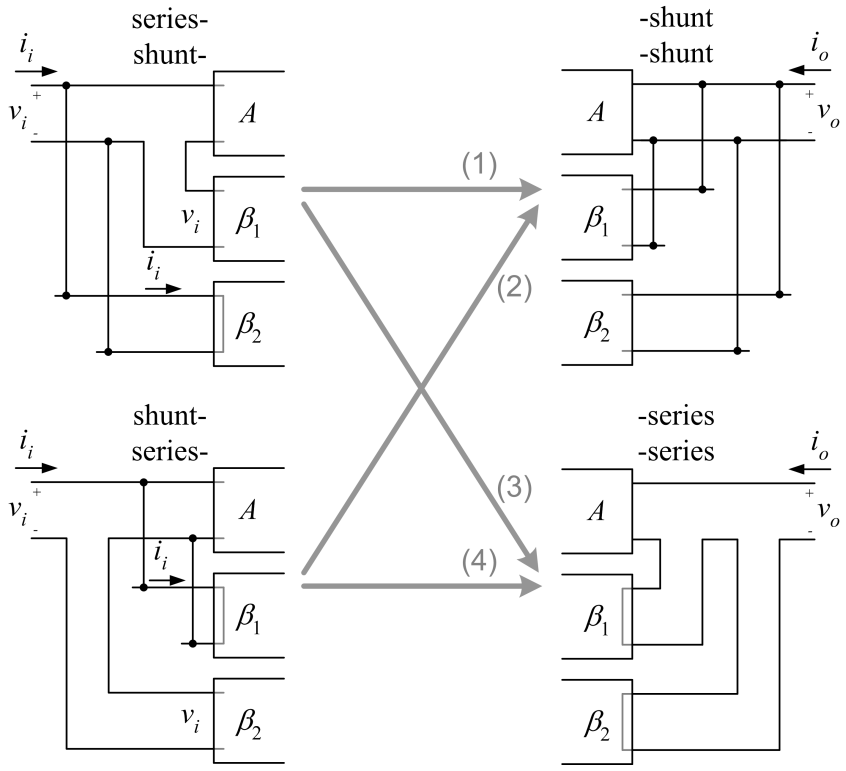

Figure 3.27: Double loop feedback amplifier sampling the same variable and comparing different variables.

Table 3.3: Input impedance for the DLF amplifier combinations of figure 3.27.

Topology of figure 3.27	Feedback loops	Input impedance
(1)	series-shunt inside shunt-shunt	$\frac{\beta_1}{\beta_2}$
(2)	shunt-series inside shunt-shunt	$\frac{\beta_2}{\beta_1}$
(3)	series-series inside shunt-series	$\frac{\beta_1}{\beta_2}$
(4)	shunt-series inside series-series	$\frac{\beta_2}{\beta_1}$

3.5.4 DLF Amplifiers suitable for LNA Design

Using the feedback types of figures 3.20 to 3.23, the four different DLF amplifiers suitable to obtain finite input impedances independent on the output load are represented in figures 3.28 to 3.31 using lumped elements.

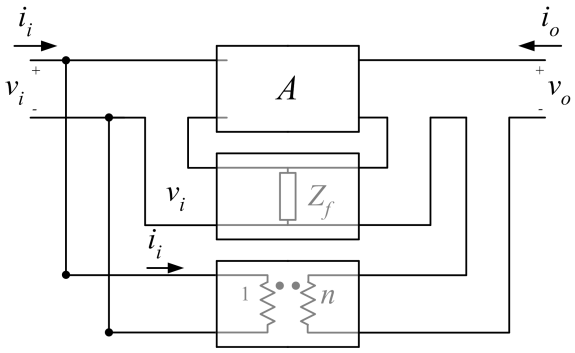

Figure 3.28: Amplifier having series-series feedback inside shunt-series feedback.

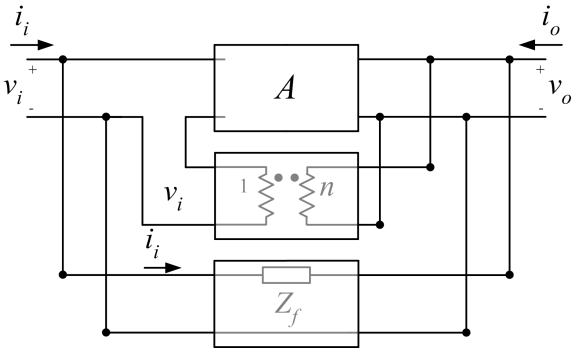

Figure 3.29: Amplifier having series-shunt feedback inside shunt-shunt feedback.

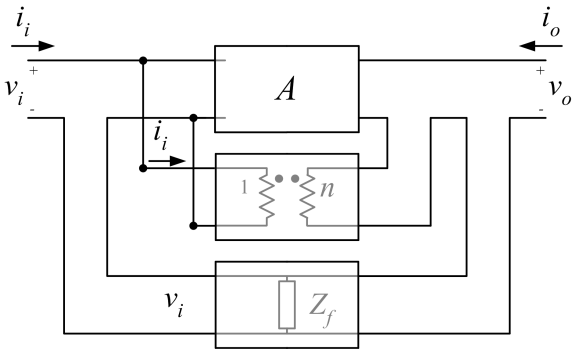

Figure 3.30: Amplifier having shunt-series feedback inside series-series feedback.

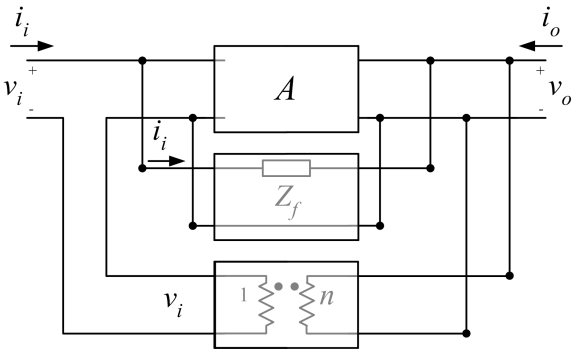

Figure 3.31: Amplifier having shunt-shunt feedback inside series-shunt feedback.

These DLF LNAs using lumped elements are now analyzed in terms of input impedance, gain and noise factor. For convenience, the order by which these topologies are analyzed does not respect the order of figures 3.28 to 3.31.

3.5.5 DLF LNA Topologies

The first two DLF LNA topologies that will be analyzed sample the output voltage with both feedback blocks. In this analysis, the transformer is ideal, and the amplifying block is an unilateral and ideal voltage amplifier with a voltage gain of A, an infinite input impedance and a zero output impedance. All LNAs are

analyzed in terms of input impedance, gain and noise factor and only the resistive element of the feedback network is noisy.

DLF LNA type 1 - DLF LNA having shunt-shunt feedback inside series-shunt feedback

The DLF LNA type 1 is represented in figure 3.32.

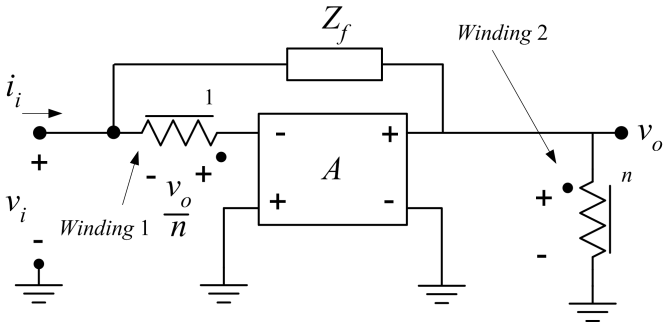

Figure 3.32: DLF LNA type 1.

The input impedance of the DLF LNA of figure 3.32 is determined considering the following equations:

$$\begin{cases} v_i = -\dfrac{v_n}{n} - \dfrac{v_o}{A} \\ \\ i_i = (v_i - v_o)\dfrac{1}{Z_f} \end{cases} \tag{3.23}$$

where A is the voltage gain of the amplifying block. The input impedance Z_{in} and the voltage gain v_o/v_i are:

$$Z_{in} = \frac{v_i}{i_i} = \frac{A+n}{A(n+1)+n} Z_f \tag{3.24}$$

$$A_v = \frac{v_o}{v_i} = -n\frac{A}{A-n} \tag{3.25}$$

If the amplifying block is ideal (infinite voltage gain A), the input impedance and the voltage gain become:

$$\lim_{A\to\infty} Z_{in} = \frac{Z_f}{n+1} \tag{3.26}$$

$$\lim_{A\to\infty} A_v = -n \tag{3.27}$$

Observing the input impedance (3.26) and knowing that the transformer ratio n is real and positive, it is concluded that the only way to obtain a positive and finite real input impedance using an ideal amplifying block is by having a real feedback impedance Z_f. From now on, Z_f will be replaced by R_f in this topology.

Concerning the noise performance, it is assumed that R_f is the only noise source of the circuit, with noise power spectral density:

$$N_{R_f}(f) = 4k_BTR_f \tag{3.28}$$

In figure 3.33 is represented the DLF LNA with the voltage noise source due to the thermal noise generated in R_f.

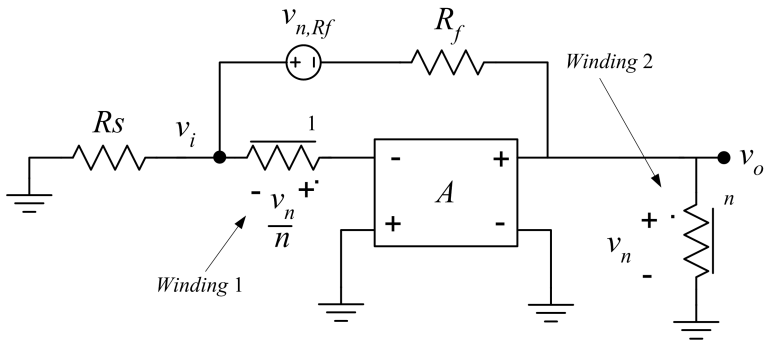

Figure 3.33: DLF LNA type 1 and the R_f noise source.

Using the source transformations of appendix C, the noise voltage source is first converted into a current source $i_{n,Rf} = v_{n,Rf}/R_f$ - step (1). By its turn, this current source is split into two sources, one connected to the LNA input and one connected to the LNA output - step (2). The current source connected to the output is in parallel with the (zero) output impedance of the amplifying block and thus its effect is canceled. These transformations are represented in figure 3.34.

The equivalent input noise source due to the feedback resistance corresponds to a current source $i_{n,i}$ in accordance with figure 3.35.

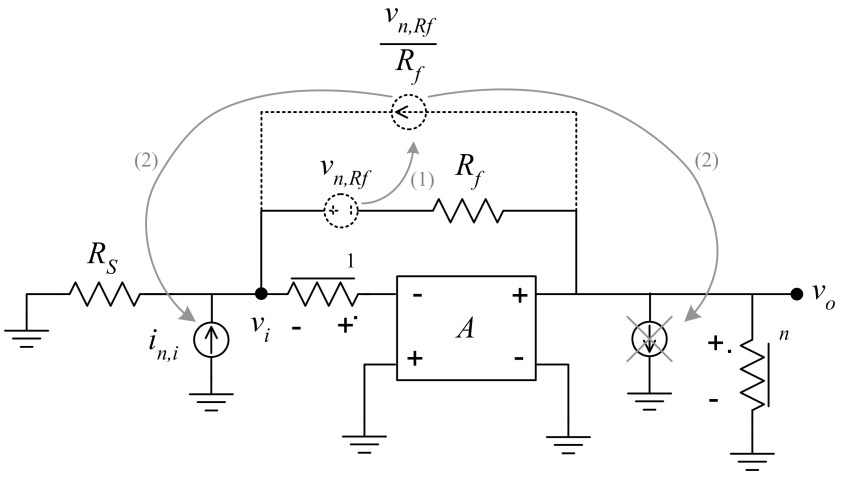

Figure 3.34: Noise transformations to determine the equivalent LNA input noise source.

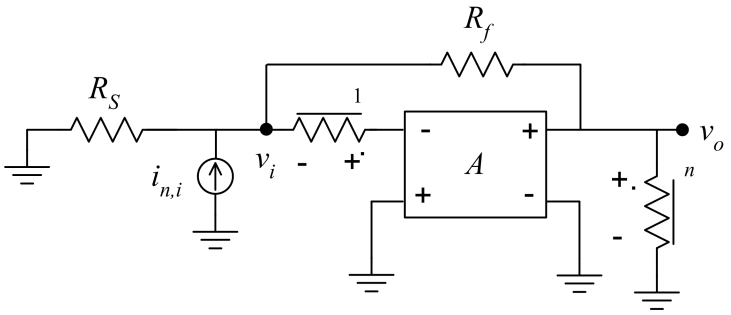

Figure 3.35: DLF LNA type 1 with equivalent input noise source.

$i_{n,i}$ is

$$i_{n,i} = \frac{v_{n,R_f}}{R_f} \tag{3.29}$$

This equivalent noise current can be converted to a noise voltage by multiplying it by the input resistance R_S:

$$v_{n,i} = i_{n,i} R_S = v_{n,R_f} \frac{R_S}{R_f} \tag{3.30}$$

If a matched condition is considered, $R_f/(n+1) = R_S$, the noise power spectral density due to the feedback resistor, and reported to the DLF LNA input, becomes:

$$N_i = 4k_B T R_f \left| \frac{R_S}{R_f} \right|^2 = \frac{4k_B T R_S}{n+1} \tag{3.31}$$

and the minimum achievable noise factor becomes:

$$F_{\min} = \frac{N_{R_S} + N_i}{N_{R_S}} = 1 + \frac{1}{n+1} \tag{3.32}$$

If n is higher than 1, F is much less than 2, which is the value that would be obtained if the LNA used a single resistor in parallel with its input to realize the impedance matching. If n is very high, F tends to its absolute minimum of 1, meaning that the LNA could be considered (approximately) noiseless.

DLF LNA type 2 - DLF LNA having shunt-shunt feedback inside series-shunt feedback

The DLF LNA type 2 is represented in figure 3.36.

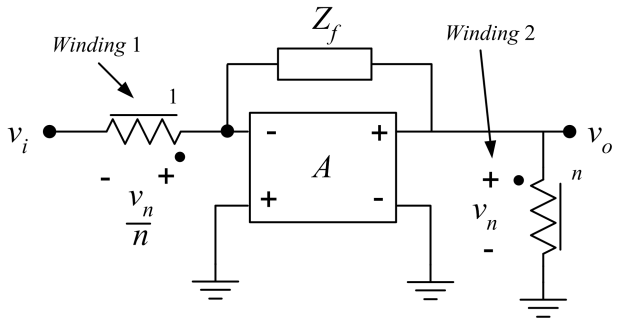

Figure 3.36: DLF LNA type 2.

Concerning the DLF LNA of figure 3.36, its equations are,

$$\begin{cases} v_i = -\dfrac{v_o}{n} - \dfrac{v_o}{A} \\ \\ i_i = \left(v_i + \dfrac{v_o}{n} - v_o\right) \dfrac{1}{Z_f} \end{cases} \tag{3.33}$$

The LNA input impedance is

$$Z_{\text{in}} = \frac{v_i}{i_i} = Z_f \frac{A+n}{An+n} \tag{3.34}$$

Considering an ideal amplifying block with infinite gain, the input impedance becomes:

$$Z_{in} = \frac{Z_f}{n} \tag{3.35}$$

Again in this topology Z_f has to be real to obtain a real input impedance. The

voltage gain is the same as for the previous circuit.

It can be shown that the noise factor is [24]:

$$F_{\min} = 1 + \frac{1}{n} \tag{3.36}$$

Comparing the two DLF LNAs analyzed before, one sees that the only difference between them is the input impedance denominator, which is $n + 1$ in the first DLF LNA and is just n in the second. This is a minor difference if $n \gg 1$.

The following two DLF LNA topologies that will be analyzed sample the output current with both feedback blocks. The transformer is again ideal and the amplifying block is, in this case, an unilateral and ideal current amplifier with infinite current gain, input and output impedances. The input impedance, the current gain and the noise factor are determined and only the resistive element of the feedback network is considered noisy.

DLF LNA type 3 - DLF LNA having series-series feedback inside shunt-series feedback

The DLF LNA type 3 is represented in figure 3.37.

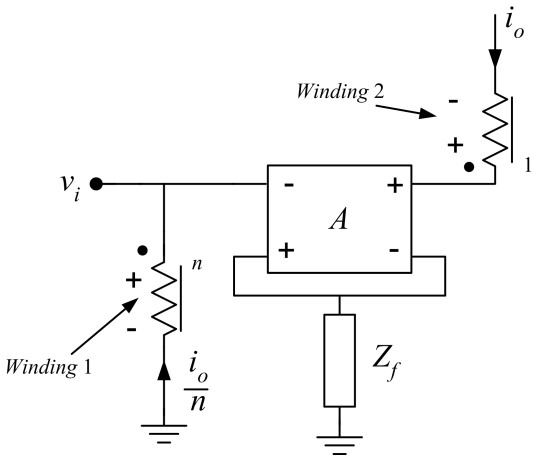

Figure 3.37: DLF LNA type 3.

In the DLF LNA with current output the parameter that should be maximized is the transconductance instead of the voltage gain. Assuming an ideal amplifying

block,

$$\begin{cases} v_i = Z_f i_o \\ i_i = \dfrac{i_o}{n} \end{cases} \tag{3.37}$$

The input impedance and transconductance are:

$$Z_{in} = nZ_f \tag{3.38}$$

$$\frac{i_o}{v_i} = \frac{1}{Z_f} \tag{3.39}$$

Again in this case, the feedback impedance Z_f has to be real. Since R_f is multiplied by the transformer ratio n, R_f is lower than 50 Ω, assuming that $n > 1$.

Concerning the noise factor, it can be shown that [24]:

$$F_{\min} = 1 + \frac{1}{n} \tag{3.40}$$

DLF LNA type 4 - DLF LNA having shunt-series feedback inside series-series feedback

The DLF LNA type 4 is represented in figure 3.38.

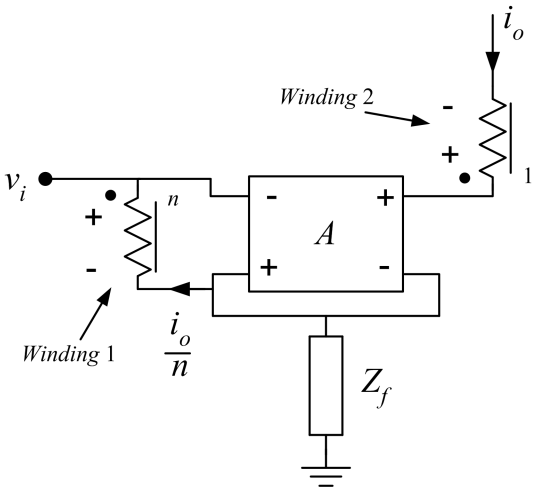

Figure 3.38: DLF LNA type 4.

Assuming an ideal amplifying block,

$$\begin{cases} v_i = Z_f(i_i + i_o) \\ i_i = \dfrac{i_o}{n} \end{cases} \tag{3.41}$$

The input impedance and transconductance are

$$Z_{in} = (n+1)Z_f \tag{3.42}$$

$$\frac{i_o}{v_i} = \frac{n}{n+1}\frac{1}{Z_f} \tag{3.43}$$

As an image of the other DLF LNA topologies, the feedback impedance Z_f must be real to obtain a real input impedance. The input impedance and the current gain are close to that determined for last topology. It can be shown that the noise factor is

$$F_{\min} = 1 + \frac{1}{n+1} \tag{3.44}$$

Assuming that n is equal in the two last topologies, this topology achieves a slightly lower noise factor than the other one.

Discussion:

Using two feedback loops, it is possible to obtain four different LNA topologies, two of them sampling the output voltage and the others sampling the output current. These topologies are suitable for LNA design because it is possible to have gain with a real input impedance and noise performance is acceptable.

In chapter 6 the DLF LNA of figure 3.32, which samples the output voltage is analyzed in more detail, considering an improved feedback network model. The implementation of the amplifying block will also be developed.

3.6 Conclusions

The most important LNA parameters are input impedance, gain, and noise factor and the LNA design results from the tradeoff between these parameters. There are several LNA topologies that have these three parameters simultaneously, and among them the one that achieves the best tradeoff is the cascode LNA using inductive degeneration. Theoretically, this topology achieves a real input impedance and a high gain with the lowest noise figure.

If the LNA is realized as a feedback amplifier having a single feedback loop, it is shown that a finite input impedance is achieved only if the amplifying block has a finite gain.

Another form of obtaining a finite input impedance, with gain and low noise figure consists of using double loop feedback. Only the DLF amplifiers sampling the same variable at the output and comparing different variables at the input have a finite input impedance independent from the load impedance. It is shown that they have additionally gain and low noise factor.

With lumped elements, four different DLF LNA topologies can be designed: two sampling current and two sampling voltage.

Chapter 4

Multi-band LNA using Cascode Transistors for Band Selection

4.1 Introduction

Conventional receiver architectures use narrowband low noise amplifiers (LNAs), with impedance matching to the antenna for maximum power transfer, and which isolate the antenna from the rest of the receiver and amplify the input signal with minimum addition of noise. However, narrowband LNAs are limited to a single frequency band. The demand for more functionality, like the reception with different wireless standards, leads to the research of new multi-band LNA topologies. This chapter is dedicated to the study of multi-band LNAs.

A multi-band CMOS LNA, which receives two or more frequency bands simultaneously, and separates them into different outputs using replicated cascode transistors, is presented in this chapter. This LNA does not have switches in the signal path. Either only one band or two or more bands simultaneously can be selected. This LNA is suitable for receivers using multi-band antennas, and where each band has to be processed by a dedicated circuit; i.e., the circuits ahead of the multi-band LNA are narrowband.

In section 4.2, the multi-band LNA having independent outputs activated by cascode transistors, is presented and analyzed. In section 4.3, simulation results are presented to demonstrate the circuit performance. Finally, in section 4.4 some conclusions are drawn.

4.2 A New Multi-Band Low Noise Amplifier

In this section, some topics on multi-band LNAs are discussed, and a multi-band LNA having independent outputs activated by cascode transistors is presented and analyzed.

4.2.1 Topics on Multi-band Low Noise Amplifiers

Figure 4.1 presents two forms of obtaining multi-band receivers (from the LNA point of view). In figure 4.1 a) there is a complete duplication of the narrowband receiving circuits [107], while in figure 4.1 b) a single multi-band LNA with two different narrow frequency bands splits the received dual-band signal through different paths [108]. The last solution has the advantage of using a single antenna and may also lead to die area and power savings. Other forms of designing multi-band receivers and multi-band LNAs are developed in the next chapter.

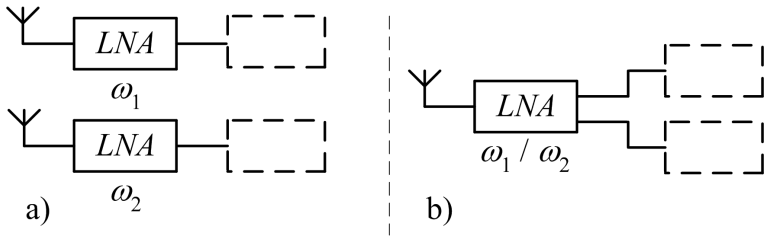

Figure 4.1: Two multi-band receiver architectures.

In this thesis, the multi-band LNAs of interest can operate at different frequencies, without a large increase in power or area, compared with a narrowband LNA [6]. A multi-band LNA is not a collection of several independent narrowband LNAs, so the solution of figure 4.1 a) is ruled out, and the approach of figure 4.1 b) will be the object of study. Most multi-band CMOS LNAs are based on the cascode topology with inductive degeneration (figure 4.2), which was studied in section 3.4.

The inductive degeneration provides a real input impedance and signal gain at a specific frequency band, without significant noise addition. Cascode transistor M_2 is used in this circuit to reduce the Miller effect due to the gate-drain capacitance of M_1 (C_{gd1}). When the effect of C_{gd1} is neglected, the input impedance can be written as:

$$Z_{in} = \frac{g_{m1} L_S}{C_t} + \frac{1}{sC_t} + sL_S \tag{4.1}$$

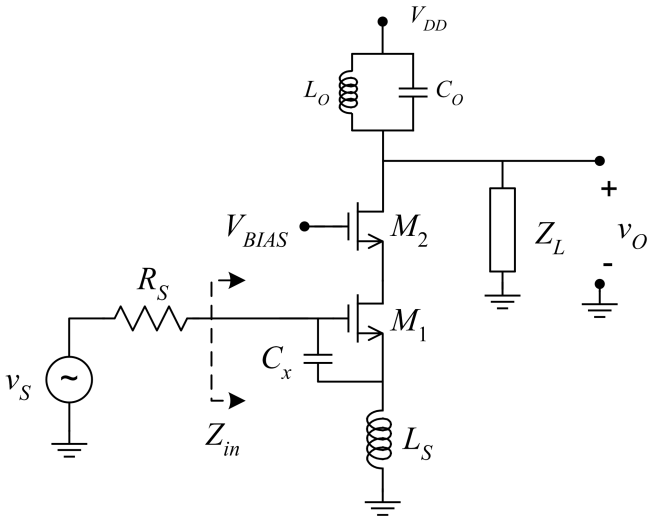

Figure 4.2: Cascode LNA with inductive degeneration (biasing of M_1 not represented).

where $C_t = C_{gs1} + C_x$. When C_t and L_S resonate, the input impedance is real. Other advantages of using M_2 are improved reverse isolation between input and output, high output resistance, and better noise performance [86]. M_1 converts the input voltage into a current, that is converted back to an amplified voltage by the output network, formed by inductor L_O and capacitor C_O. This output network is tuned to a frequency equal to:

$$\omega_0 = \frac{1}{L_O C_O} \tag{4.2}$$

The input and output networks should be tuned to the same frequency.

This LNA topology is widely studied in literature, and several studies on how to optimize different LNA parameters like noise performance, linearity or voltage supply are found in [83, 90, 92, 99, 109, 110].

4.2.2 A New Multi-Band LNA

The LNA in figure 4.3 is based on the cascode LNA topology with inductive degeneration. It has wide-band input matching obtained with a resonant filter (L_1 and C_1) added to the LNA of figure 4.2. At the output, this LNA has two independent resonant circuits tuned to distinct frequencies and connected to M_1 through different cascode transistors. Each cascode transistor can be used to switch off the corresponding output branch by lowing the gate voltage (which is usually constant

and typically equal to the supply voltage in the conventional circuit of figure 4.2).

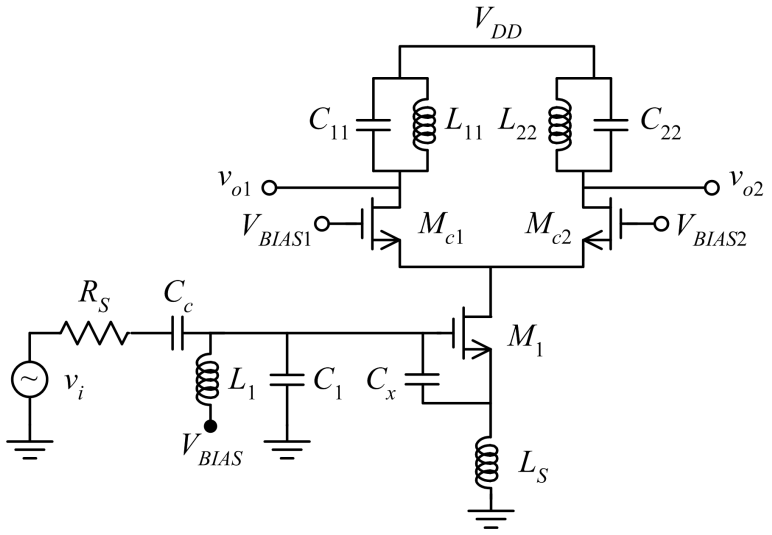

Figure 4.3: Dual-band LNA based on cascode switching (M_1 bias not included).

The circuit of figure 4.3 is represented with two output networks, but it can have more output branches, each one tuned to a different frequency and selected by the corresponding cascode transistor.

When several input signal bands are present simultaneously, each output network is only sensitive to the frequency band for which it is tuned. When only one cascode transistor is on, the LNA works as a normal single-band LNA and, apart from parasitic coupling effects, the inactive outputs will not affect the active one.

The input impedance matching network is built with inductor L_1 and capacitor C_1 providing wideband impedance matching that embraces the multiple tuning frequencies [108, 111]. It has lower and upper 3 dB cutoff frequencies, ω_{lower} and ω_{upper}, determined by:

$$\begin{cases} \omega_{lower} = \dfrac{R_{in}}{L_1} \\ \\ \omega_{upper} = \dfrac{1}{R_{in}C_1} \end{cases} \tag{4.3}$$

where R_{in} is given by

$$R_{in} = \frac{g_{m1}L_S}{C_t} \tag{4.4}$$

The LNA of figure 4.3, having only one input, can be connected to a multi-band antenna. This LNA does not have switches in the signal path, because each output is activated by the corresponding cascode transistor.

There is also the possibility of controlling the gain of one output simply by varying the cascode transistor gate voltage (and consequently varying its quiescent current).

4.2.3 Noise Analysis

In chapter 3, the noise factor of the cascode LNA using inductive degeneration was obtained considering a single-band matching network. In this chapter the input matching network is wideband and is determined by L_1 and C_1. Figure 4.4 represents the incremental model of the input part of the multi-band LNA of figure 4.3. The noise sources considered are the thermal noise voltage due to the gate resistance $v_{n,Rg}$ and the noise current source due to the channel resistance $i_{n,d1}$.

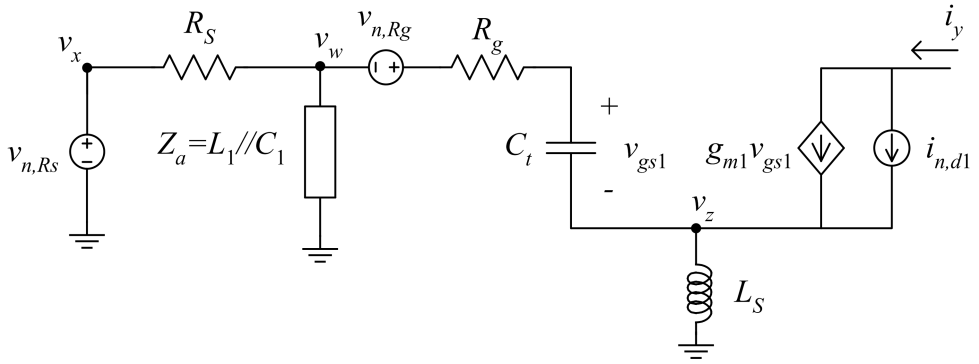

Figure 4.4: Incremental model of the input part of the multi-band LNA with noise sources.

In figure 4.5, noise source transformations (appendix D) are used to determine the noise voltage $v_{n,i}$, referred to the LNA input.

In step 1 the current source $i_{n,d1}$ is split into two current sources. In step 2, one of the current sources is converted into a voltage source $Z_S i_{n,d1}$, where Z_S is the impedance due to L_S. $Z_S i_{n,d1}$ is referred to the input, by dividing it by the voltage gain $A_v = v_z/v_x$, in step 3. In step 4, the other current source $i_{n,d1}$ is referred to the input by using the LNA transconductance $G_m = i_y/v_x$. Finally, in step 5, the voltage source $v_{n,Rg}$ is translated to the input by dividing it by the voltage gain $A'_v = v_w/v_x$.

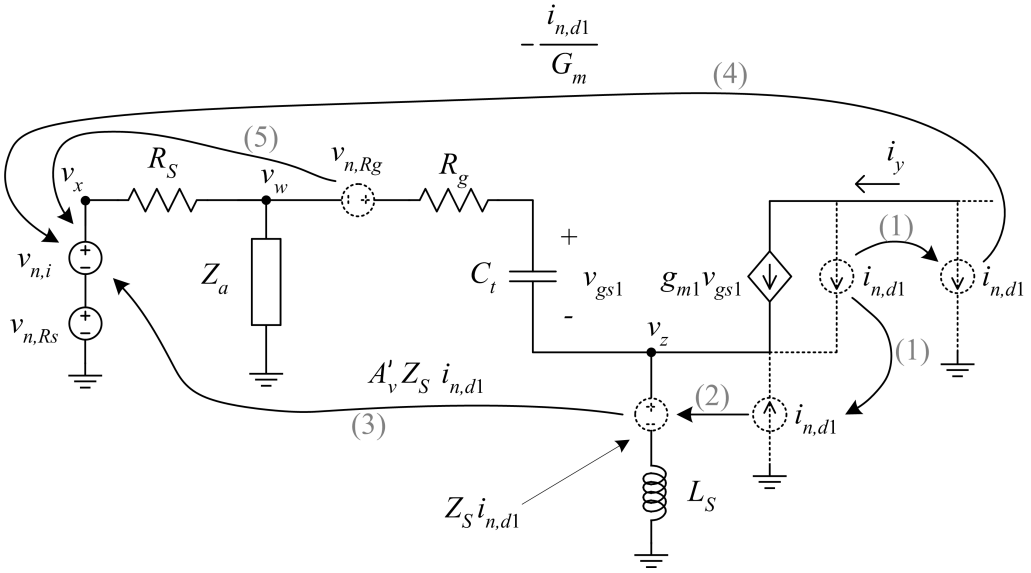

Figure 4.5: Incremental model of the multi-band LNA showing noise source transformations.

$v_{n,i}$ is:

$$v_{n,i} = \left(A_v'^{-1}\right) v_{n,R_g} + \left(A_v^{-1} Z_S - \frac{1}{G_m}\right) i_{n,d1} \tag{4.5}$$

where A'_v, A_v and G_m are:

$$A'_v = \frac{v_w}{v_x} = \frac{Z_a \| Z_{in}}{R_S + Z_a \| Z_{in}} \tag{4.6}$$

$$A_v = \frac{v_z}{v_x} = \frac{v_w}{v_x}\frac{v_z}{v_w} = A'_v \left(\frac{(g_{m1} + Y_t) Z_S}{R_g Y_t + 1 + (g_{m1} + Y_t) Z_S}\right) \tag{4.7}$$

$$G_m = \frac{i_y}{v_x} = \frac{v_w}{v_x}\frac{i_y}{v_w} = A'_v \frac{g_{m1}}{1 + R_g Y_t + g_{m1} Z_S + Y_t Z_S} \tag{4.8}$$

where $Y_t = Y_{gs} + Y_x$ is the admittance due to C_{gs} and C_x. Z_{in} is

$$Z_{in} = R_g + \frac{1}{Y_t} + Z_S + \frac{g_{m1} L_S}{C_t} \tag{4.9}$$

and Z_a is

$$Z_a = \frac{sL_1}{s^2 L_1 C_1 + 1} \tag{4.10}$$

The noise power spectral density is determined using (4.5) and the Wiener-Khintchine theorem:

$$N_i(f) = \left|A_v'^{-1}\right|^2 N_{R_g}(f) + \left|A_v^{-1} Z_S - \frac{1}{G_m}\right|^2 N_d(f) \tag{4.11}$$

The noise factor is finally:

$$F(f) = 1 + \frac{N_i(f)}{N_S} \tag{4.12}$$

Analyzing (4.11) and (4.12), it is visible that the noise performance improves if the LNA transconductance is high. The degeneration increases the noise factor; and thus, L_S should be low. These two specifications are in accordance with what is found in literature concerning the cascode LNA with inductive degeneration [56]. However, it is expected a different frequency response to that verified in the narrowband cascode LNA due to the presence of Z_a. The presence of several cascode transistors (one for each output network) could mean an increase in the noise figure; however, the current that bias the gain transistor (M_1 of figure 4.3) is divided by each cascode transistors reducing their transconductance, and consequently the thermal noise generated. Thus, it is expected a small difference between the different operating modes.

4.3 Simulation Results

To evaluate the feasibility of the dual-band LNA of figure 4.3, a circuit was designed using AMS 0.35 μm CMOS technology with 3 V supply. The frequencies of 900 MHz and 1.8 GHz are chosen because they are two widely used frequencies. The cascode transistors have the same dimensions, so their bias currents are the same when both outputs are active. All transistors are designed with the minimum length to improve the transition frequency. The output inductor series resistance affects the voltage gain characteristic. The output network inductors L_{11} and L_{22} and their series resistances correspond to integrated spirals provided by the AMS technology. Inductors L_S and L_1 of the input network are assumed to be ideal. The values used in the simulations are listed in table 4.1.

Table 4.1: Element values used in simulations and theoretical curves.

Parameter	Value	Parameter	Value	
W_{M1}	800 μm	L_S	1.2 nH	
$W_{M_{c1}}$	36 μm	L_{11}	13.2 nH	(r_{11}=14 Ω)
$W_{M_{c2}}$	36 μm	C_{11}	2.2 pF	
L_1	9.0 nH	L_{22}	6.4 nH	(r_{22}=7 Ω)
C_1	700 fF	C_{22}	1.1 pF	
C_x	1.2 pF	g_{m1}	101 mS	
c_{gs1}	743 fF	R_{g1}	4.5 Ω	

Figure 4.6 shows the voltage gain at the two outputs, when only one output is active, i.e., when M_{c1} works in saturation and M_{c2} is cutoff, or vice-versa. The voltage gain has a peak at approximately the desired frequency, determined by the resonance of L_{ii} and C_{ii}. There is no significant influence from the inactive output. Figure 4.7 presents the same curves of figure 4.6 together with the gain at the inactive outputs. If a cascode transistor is cutoff, the voltage gain at the corresponding output is below -70 dB for all the frequency range, which is low enough to consider that output inactive.

Figure 4.8 shows the curves of figure 4.6 compared with those obtained when both outputs are active: the gain at each output drops approximately 6 dB in comparison with the case where only one output is active (the gain reduces to a half). Since both cascode transistors are equal, the current from M_1 is divided equally by the two output branches.

Figure 4.9 represents the voltage gain at output 2, when V_{BIAS1} of M_{c1} is varied.

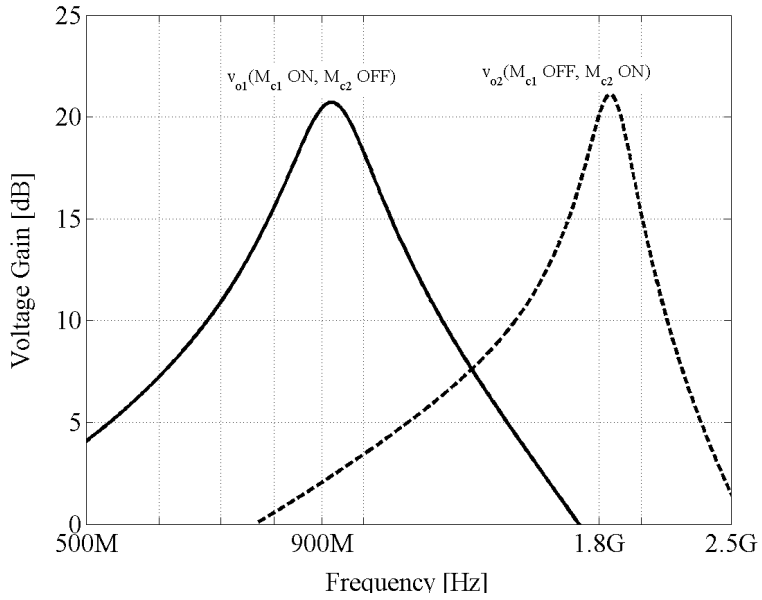

Figure 4.6: Voltage gain at "active" outputs 1 and 2 when one cascode transistor is in saturation and the other is cutoff.

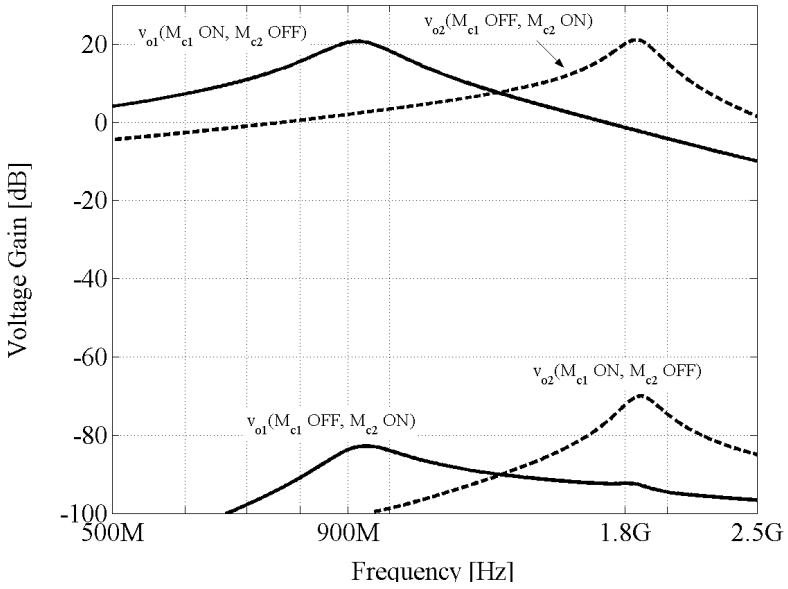

Figure 4.7: Comparison of voltage gain at active and inactive outputs.

This shows that it is possible to vary significantly the gain.

The input matching, measured by parameter S_{11}, is represented in figure 4.10 in three different operating modes (both outputs active, or only one). In all three cases S_{11} is close to -10 dB at the two frequencies of interest, without significant differences between them. This means that the input impedance is not significantly

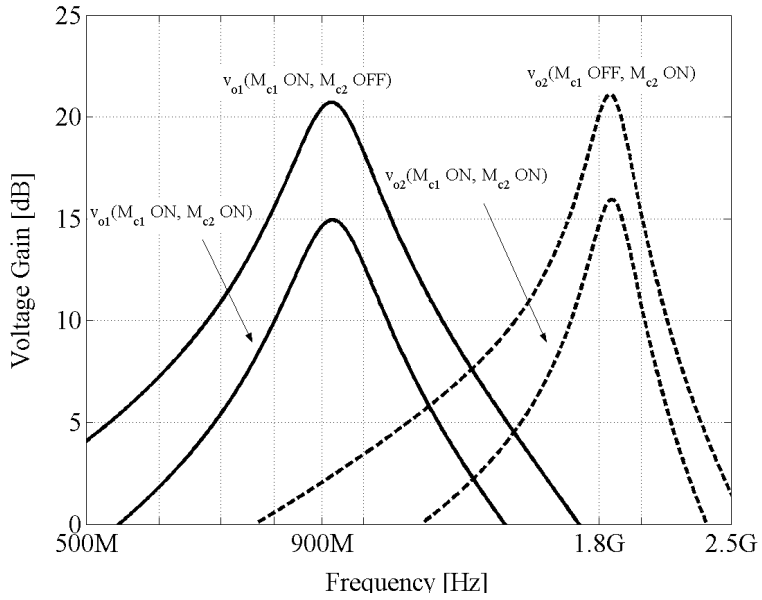

Figure 4.8: Voltage gain at outputs 1 and 2, with both outputs active and with only one output active.

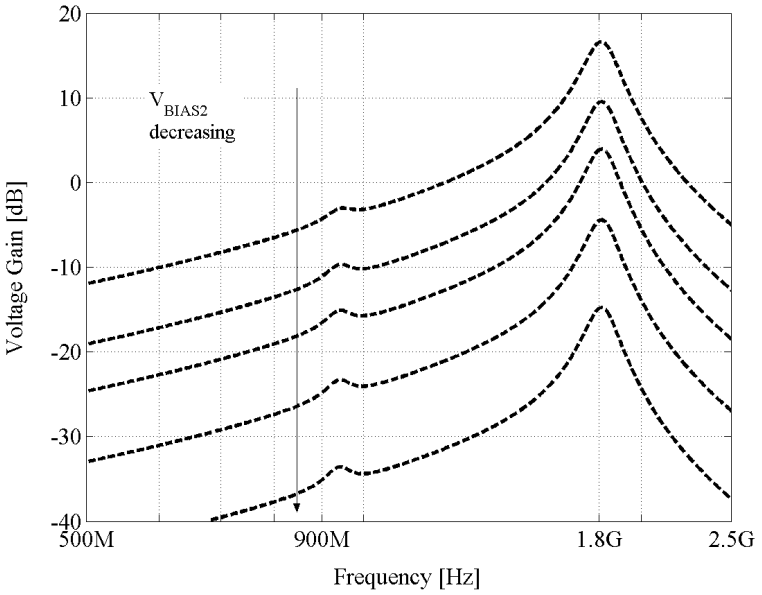

Figure 4.9: Voltage gain at output 2 when V_{BIAS2} varies and $V_{BIAS1} = V_{DD}$.

affected by the different operating modes.

In figure 4.11, the LNA noise figure obtained by simulation is compared with the theoretical value. The values used to determine the NF curves are listed in table 4.1. The noise figure at 900 MHz and 1.8 GHz is, respectively, 1.5 dB and 2.5 dB, which is well below the 3 dB reference value, giving a margin for other noise sources

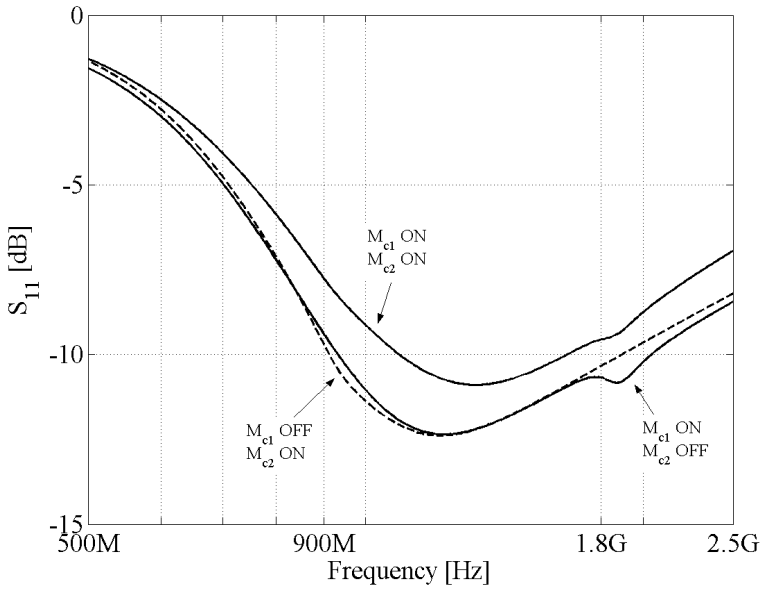

Figure 4.10: S_{11} plots in three different situations, showing the low influence of the different operating modes.

to be considered. The small difference between the theoretical and simulated curves is due to the high transconductance of M_1 that attenuates significantly the influence of the noise sources ahead of M_1, like the noise sources originated at the cascode transistors. There is no significant difference between the different modes of operation. This is due to the much higher transconductance of M_1 in comparison with the transconductance of the cascode transistors.

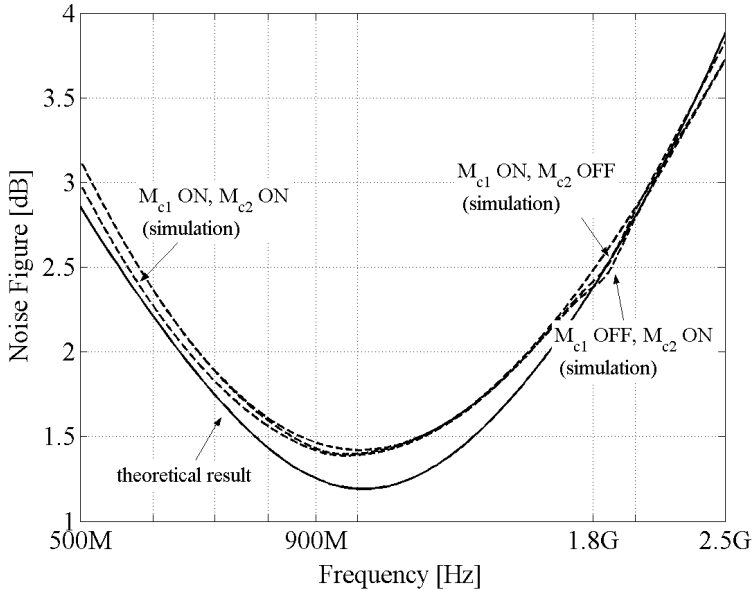

Figure 4.11: Simulated noise figure of the complete dual-band LNA circuit.

4.4 Conclusions

In this chapter, a new multi-band LNA is presented. This circuit has two (or more) resonant output networks tuned to different frequencies which are switched on and off by cascode transistors. The outputs are activated when the cascode transistors are in saturation. The input impedance is wideband to embrace all working bands and is not significantly affected by the number of active outputs. This is possible because the cascode transistors provide a good output-input isolation and because the current through the input transistor (M_1 in figure 4.3) is kept constant.

When implementing a dual-band CMOS LNA, the voltage gain at one output has a decrease of approximately 3 dB when both output networks are active with respect to the case where only one output is active. It is possible to obtain a noise figure below 3 dB between the central frequencies of the two bands, and the different modes of operation do not affect significantly the noise figure, meaning that this dual-band LNA keeps the good noise performance of the cascode LNA with inductive degeneration which inspired this dual-band LNA.

Chapter 5

Concurrent Dual-Band LNA using Magnetically Coupled Inductors

5.1 Introduction

In this chapter, concurrent multi-band LNAs are studied. Concurrent multi-band LNAs work simultaneously at different frequency bands (non-concurrent multi-band LNAs operate at different frequency bands, but one at a time) [6].

A new concurrent dual-band LNA, based on the multi-band LNA studied in last chapter, is proposed in this chapter. Both circuits have the same wideband input impedance matching network; however, this new topology has the inductors of the output networks magnetically coupled. By magnetically coupling the inductors, this LNA will have two bands simultaneously at the output. By balancing the current between both output networks, it is also possible to vary the voltage gain at both bands.

In section 5.2 a short overview of concurrent multi-band LNAs is presented. In section 5.3 a new concurrent dual-band LNA is presented and, its frequency response is analyzed considering ideal elements. The frequency response is reanalyzed, in section 5.4, accounting for the parasitic series resistance of some inductors. In section 5.5 the LNA dimensioning is described and some simulation results are presented. In section 5.6 an alternative LNA circuit is proposed. It has a different voltage gain variation, in comparison with the first circuit presented. Finally, some conclusions are drawn in section 5.7.

5.2 Concurrent Multi-Band LNAs

Figure 5.1 presents two forms of obtaining multi-band receiver architectures, from the LNA point of view. In figure 5.1 a) the LNAs are narrowband, have different inputs and are connected through switches to the subsequent blocks [20]. In this architecture two narrowband LNAs are needed; thus, this is not an optimal solution, due to the duplication of blocks (LNAs, and(or) antennas), which leads to an increase in power and die area. Figure 5.1 b) consists of a single-input, single-output, multi-band LNA that has a frequency response with different pass-bands [6]. One advantage of this last solution is the use of a single antenna and only one LNA circuit which may have lower area and power than two narrowband LNAs.

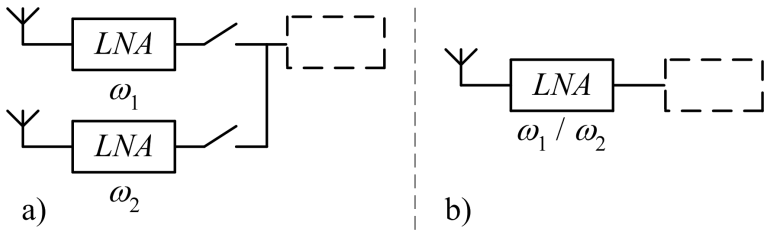

Figure 5.1: Two multi-band receiver architectures.

As referred in last chapter, most multi-band LNAs (including concurrent LNAs) are based on the cascode topology with inductive degeneration of figure 4.2.

The LNA of figure 5.1 b) can be concurrent or non-concurrent, depending on the use of both bands simultaneously or not, respectively. One technique to obtain a non-concurrent multi-band LNA using the cascode topology, consists of varying the LNA tuning frequency by changing the value of passive elements using transistor switches, as shown in figures 5.2 a) and b) [112, 113]. The (transistor) switches sizing has to trade between a small resistance and a large capacitance. The transistor equivalent resistance has to be lower than the series parasitic resistance of the inductance in parallel, to ensure the DC current will flow through the transistor when it is active. However to obtain a small resistance, the transistor has to be large, which increases the transistor parasitic capacitances, affecting the resonant circuit tuning frequencies [114, 115].

One technique to design a concurrent multi-band LNA, consists of tuning the input and output networks to different frequencies by using multi-resonant circuits, as happens in LNAs of figure 5.3 [6, 116, 117]. However, one problem of this solution

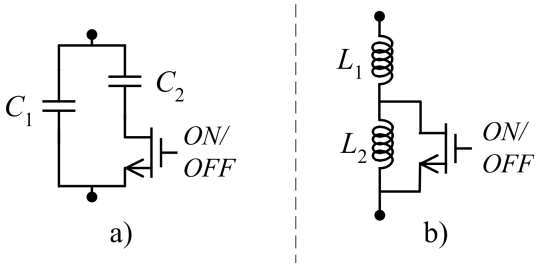

Figure 5.2: a) Variable capacitor. b) Variable inductor.

is a high LNA die area, mainly due to the inductors, that must have enough space between them to ensure a negligible magnetic coupling. Other works concerning the LNA bandwidth extension, mainly that of the cascode LNA can be found in literature [6, 108, 112, 113, 115, 118, 119].

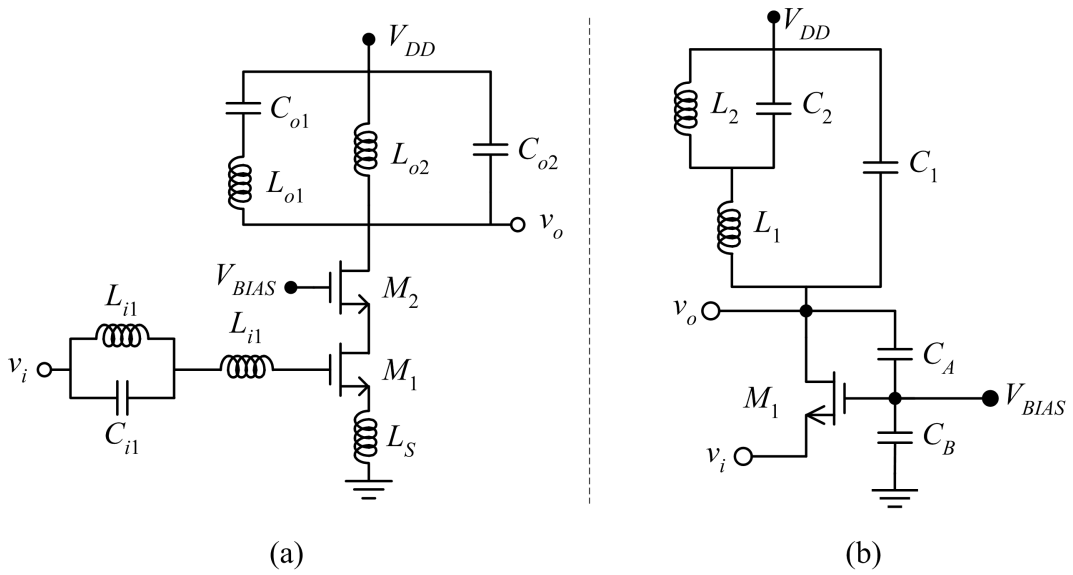

Figure 5.3: Dual-band LNAs using multi-resonant circuits. (a) LNA based on cascode topology with inductive degeneration. (b) LNA based on the common-gate stage (C_A and C_B realize a series-shunt feedback). Biasing of M_1 not presented.

In next section a new concurrent dual-band LNA is presented and its frequency response analyzed.

5.3 Concurrent Dual-Band CMOS LNA using Magnetically Coupled Inductors

The proposed concurrent dual-band CMOS LNA is presented in figure 5.4. It is similar to that of figure 4.3; however, magnetic coupling between the output inductors changes significantly the overall characteristics.

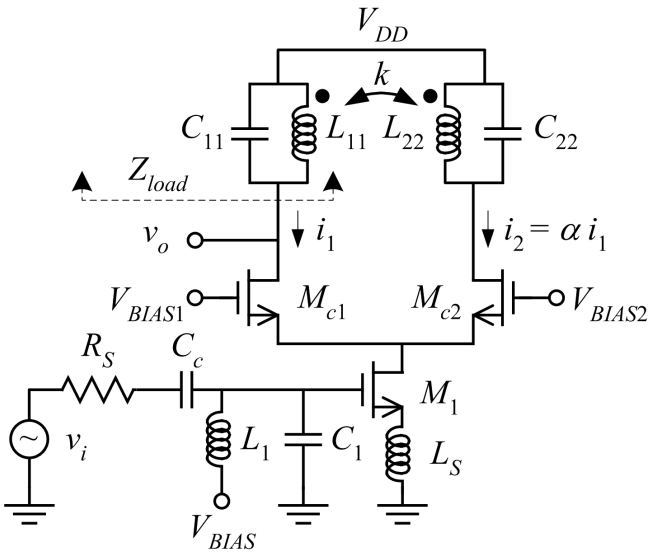

Figure 5.4: Concurrent dual-band LNA based on inductor magnetic coupling.

5.3.1 Working Principle

The LNA of figure 5.4 has a wideband input stage built with transistor M_1, L_S, L_1, and C_1, which has already been studied in chapter 4. The two output resonant networks, with L_{ii} and C_{ii}, are magnetically coupled, with a magnetic coupling coefficient k. The magnetic coupling leads to the presence of two bands at the output, making this LNA a concurrent dual-band LNA. The relative gain of the two bands can be varied simply by changing the cascode transistor gate bias voltage.

The two magnetically coupled inductors together with the capacitors form a double tuned filter, with two different resonant frequencies, that was often used in past in tuned amplifiers [37, 120, 121]. This double tuned filter in the output of LNA of figure 5.4 gives it its dual-band feature; however, using it alone, it is not possible to have relative gain variation. This is achieved by the additional cascode transistor M_{c2}. By varying the gate voltage of M_{c2}, while keeping the gate voltage of M_{c1} constant, it is possible to change the current distribution between the two output

branches. Another advantage of having magnetically coupled inductors, is that when they are integrated, they use less area than uncoupled inductors, since the inductors can be overlapped.

5.3.2 Frequency Response

In figure 5.5 the schematic of the double tuned circuit with coupled inductors is represented. Considering both cascode transistors in saturation, their currents, i_1 and i_2 are proportional, $i_2 = \alpha i_1$, according to the ratios of their W/L and of their V_{GS} bias voltages.

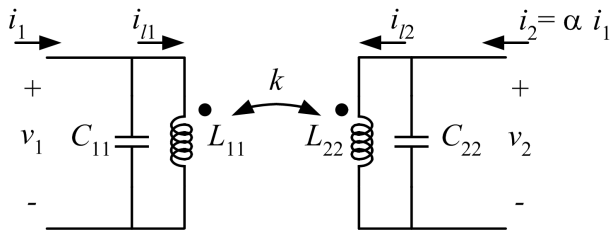

Figure 5.5: Double tuned circuit with coupled inductors.

The equations for the circuit in figure 5.5 are:

$$V_1 = sL_{11}I_{l1} + sMI_{l2} \tag{5.1a}$$

$$V_2 = sMI_{l1} + sL_{22}I_{l2} \tag{5.1b}$$

$$I_{l1} = I_1 - V_1 sC_{11} \tag{5.1c}$$

$$I_{l2} = I_2 - V_2 sC_{22} \tag{5.1d}$$

$$I_2 = \alpha I_1 \tag{5.1e}$$

$$M = k\sqrt{L_{11}L_{22}} \tag{5.1f}$$

The load impedance $Z_{load} = V_1/I_1$, as represented in figure 5.5, is:

$$Z_{load} = \frac{C_{22}(L_{11}L_{22} - M^2)s^3 + (L_{11} + \alpha M)s}{C_{11}C_{22}(L_{11}L_{22} - M^2)s^4 + (C_{11}L_{11} + C_{22}L_{22})s^2 + 1} \tag{5.2}$$

The voltage gain v_o/v_i of the LNA of figure 5.4 is proportional to Z_{load}, being

maximum at the frequency of the poles of Z_{load} and minimum at the zeros frequency. The load impedance (5.2) has two pole pairs located at:

$$\omega_{1,2}^2 = \frac{C_{11}L_{11} + C_{22}L_{22} \pm \sqrt{\zeta}}{2C_{11}C_{22}(L_{11}L_{22} - M^2)} \tag{5.3}$$

where

$$\zeta = (C_{11}L_{11} + C_{22}L_{22})^2 + 4C_{11}C_{22}(M^2 - L_{11}L_{22}) \tag{5.4}$$

The load impedance has also one zero at the origin and a pair of imaginary zeros $j\omega_z$, with

$$\omega_z^2 = \frac{L_{11} + \alpha M}{C_{22}(L_{11}L_{22} - M^2)} = \frac{L_{11} + \alpha M}{C_{22}L_{11}L_{22}(1 - k^2)} \tag{5.5}$$

The pole pairs are independent from the current ratio α, while the zero pair depends on it. This means that the current ratio can be used to adjust the zero pair position relatively to the pole pairs.

Observing (5.2), there is a case of particular interest that is when $k^2 \ll 1$. In this case, the load impedance simplifies to:

$$Z_{load} \approx \frac{C_{22}L_{22}(L_{11})s^3 + (L_{11} + \alpha M)s}{C_{11}C_{22}(L_{11}L_{22})s^4 + (C_{11}L_{11} + C_{22}L_{22})s^2 + 1} \tag{5.6}$$

and the two pole pairs are located at

$$\begin{cases} \omega_1^2 \approx \dfrac{1}{L_{11}C_{11}} \\ \\ \omega_2^2 \approx \dfrac{1}{L_{22}C_{22}} \end{cases} \tag{5.7}$$

while the zero pair is placed approximately at:

$$\omega_z^2 \approx \frac{L_{11} + \alpha M}{C_{22}L_{11}L_{22}} \approx \frac{1}{C_{22}L_{22}} + \frac{\alpha M}{C_{22}L_{11}L_{22}} \approx \omega_2^2 + \frac{\alpha M}{C_{22}L_{11}L_{22}} \tag{5.8}$$

Figure 5.6 represents a possible plot of the load impedance module as a function of frequency. To ensure that the zero is placed between the two poles, the pole at ω_2 has to be placed at the lower frequency, because, from (5.8), the zero is placed at a higher frequency than ω_2.

The current ratio α can be used to control the complex zero position. This ratio is changed by changing the cascode transistors size or by varying their gate bias voltages.

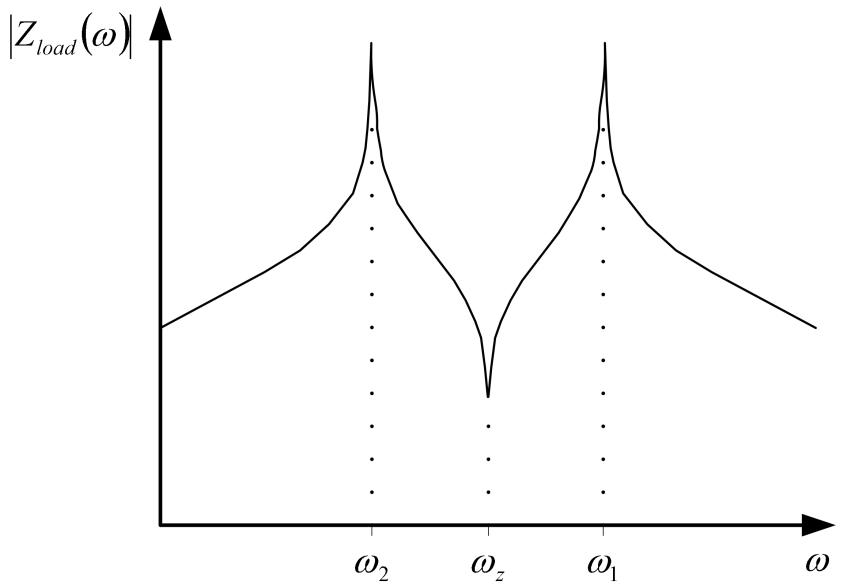

Figure 5.6: Possible plot of the absolute value of the load impedance Z_{load}.

5.4 Effect of the Inductors Parasitic Resistance

In the last section, the frequency response was determined assuming that the inductors have zero resistance. In this section, the inductors have a parasitic resistance, meaning that sL_{ii} is replaced by $sL_{ii}+r_{ii}$, where r_{ii} is the series resistance. Making this substitution in (5.6),

$$Z_{load} = \frac{sC_{22}(sL_{22}+r_{22})(sL_{11}+r_{11})+(sL_{11}+r_{11}+\alpha sM)}{(sC_{11}(sL_{11}+r_{11})+1)(sC_{22}(sL_{22}+r_{22})+1)} \tag{5.9}$$

To simplify the analysis of (5.9), it is assumed that the lower frequency zero is still located at the origin, i.e. the first zero is at a much lower frequency than the first pole ω_2.

$$\omega_z = \frac{r_{11}}{L_{11}+\alpha M} \ll \omega_2 \tag{5.10}$$

Z_{load} becomes

$$Z_{load} = \frac{v_1}{i_1} = s\frac{C_{22}L_{11}L_{22}s^2+C_{22}(L_{11}r_{22}+L_{22}r_{11})s+L_{11}+\alpha M}{(C_{11}L_{11}s^2+r_{11}C_{11}s+1)(C_{22}L_{22}s^2+r_{22}C_{22}s+1)} \tag{5.11}$$

The quality factor of the poles can be obtained by comparison of the two factors of the denominator of (5.11) with $s^2+\frac{\omega_p}{Q_p}s+\omega_p^2$:

$$Q_1 = \frac{1}{r_{11}}\sqrt{\frac{L_{11}}{C_{11}}} \tag{5.12}$$

$$Q_2 = \frac{1}{r_{22}}\sqrt{\frac{L_{22}}{C_{22}}} \tag{5.13}$$

The pole pair frequencies are

$$\omega_1^2 \approx \frac{1}{L_{11}C_{11}} \tag{5.14}$$

$$\omega_2^2 \approx \frac{1}{L_{22}C_{22}} \tag{5.15}$$

The same procedure is used to determine the zeros' quality factor and frequency:

$$Q_z = \frac{\sqrt{L_{11}L_{22}}\sqrt{L_{11}+\alpha M}}{L_{11}r_{22}+L_{22}r_{11}} \tag{5.16}$$

$$\omega_z^2 = \frac{L_{11}+\alpha M}{C_{22}L_{22}L_{11}} \tag{5.17}$$

The frequencies of the poles and zeros are equal to those in last subsection, where the inductor series resistance is neglected. This means that the LNA gain is affected, but the poles location is not altered. In figure 5.7 the effect caused by the inductor series resistances is represented.

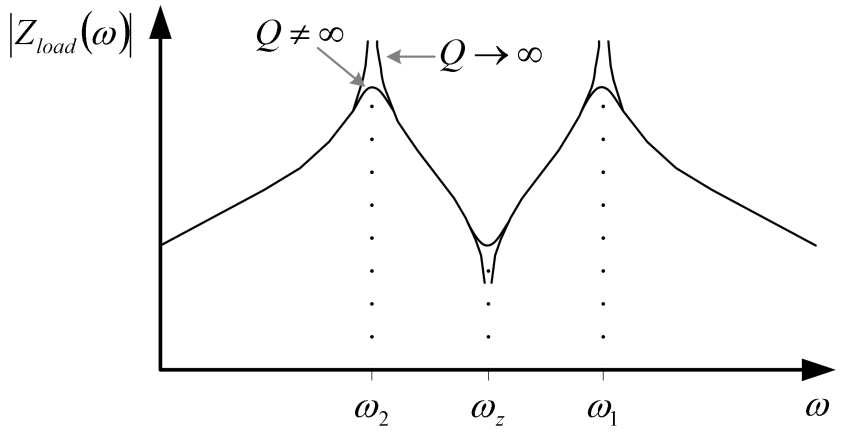

Figure 5.7: Possible plot of the load impedance Z_{load}, considering the inductor series resistances.

5.5 Simulation Results

To evaluate the feasibility of this dual-band LNA, the circuit of figure 5.4 is designed using the AMS 0.35 μm CMOS technology and a 3 V supply. The frequencies of 900 MHz and 1.8 GHz are again chosen. The cascode transistors are designed with the same dimensions and the gate of M_{c1} is connected to V_{DD}. All transistors are designed with minimum length to improve the transition frequency, and the parasitic series resistance of the output network inductors is taken into account.

5.5.1 Circuit Dimensioning

The magnetic coupling coefficient is choosen as $k = 0.35$, to make k^2 much lower than 1, but still with significant magnetic coupling.

Inductances $L_{11} = 6.4$ nH and $L_{22} = 10.0$ nH are implemented, respectively, in metal layers 3 and 4 (top metal). They use different metal layers to be overlapped, to obtain the desired value of k, which is adjusted by shifting horizontally one inductor with respect to the other [68]. The magnetic coupling is not determined by Spectre models, and it is necessary to use an electromagnetic simulator: ASITIC is used in this example [67].

As $k^2 \ll 1$, equations (5.7) can be used to obtain $C_{11} = 1.2$ pF and $C_{22} = 3.1$ pF.

The cascode transistors are equal, $V_{BIAS1} = V_{DD}$, and V_{BIAS2} can be varied 0 and V_{DD} (α varies between 0 and 1). Using (5.5), the zero pair frequency will be between 1.05 GHz for $\alpha = 0$ and 1.26 GHz for $\alpha = 1$. The geometrical mean between the two resonant frequencies, $\sqrt{\omega_1\omega_2}$, is approximately 1.27 GHz; thus, to place the zero frequency between the pole frequencies, α should be 1; i.e., both cascode transistors should be equal and have the same gate bias voltage. After some iterations, the required values listed in table 5.1 were obtained.

Figure 5.8 shows the voltage gain, in which the two maxima are approximately at the desired frequencies. The minimum voltage gain is located at approximately 1.3 GHz, which corresponds to the expected value. Figure 5.9 presents the input matching impedance, in terms of parameter S_{11}. The circuit is correctly matched at the desired frequencies (S_{11} is close to -10 dB). Finally, figure 5.10 represents the noise figure simulation compared with the theoretical result (4.12) obtained in chapter 4, using the values of table 5.1.

Table 5.1: Element values of the concurrent dual-band CMOS LNA using coupled inductors.

Parameter	Value	Parameter	Value	
W_{M1}	800 μm	L_S	1.2 nH	
$W_{M_{c1}}$	36 μm	L_{11}	6.4 nH	($r_{11} = 7\ \Omega$)
$W_{M_{c2}}$ ($\alpha \in [0,1]$)	36 μm	C_{11}	1.3 pF	
L_1	9.0 nH	L_{22}	10.0 nH	($r_{22} = 12\ \Omega$)
C_1	700 fF	C_{22}	2.6 pF	
V_{BIAS1}	V_{DD}	V_{BIAS2}	[0,V_{DD}]	
C_x	1.2 pF	k	0.35	

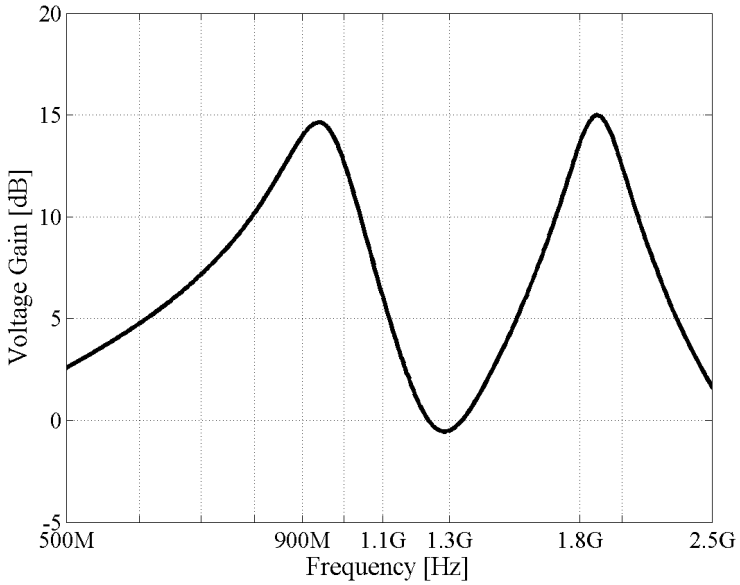

Figure 5.8: Voltage gain.

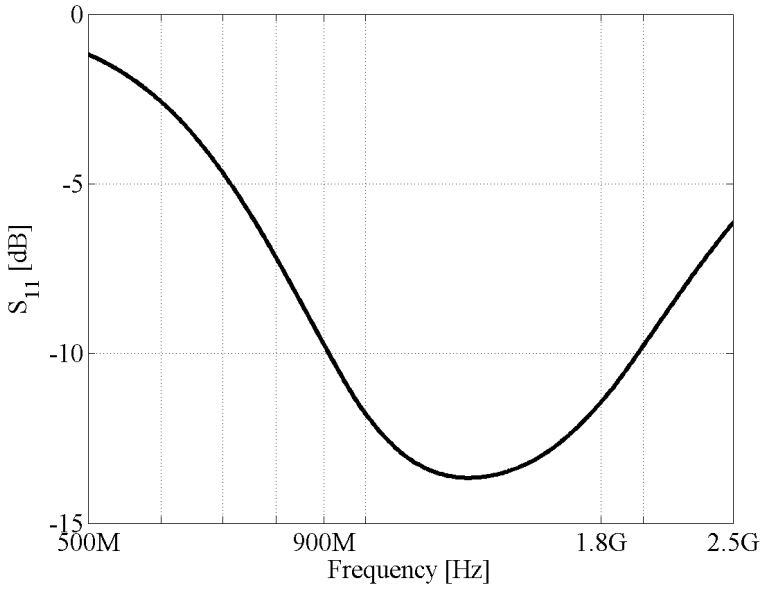

Figure 5.9: S_{11} simulation of the concurrent dual-band LNA.

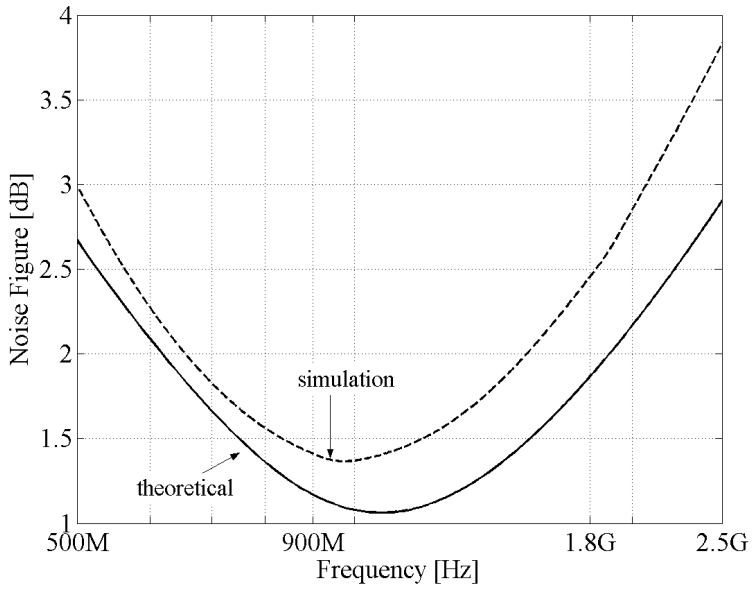

Figure 5.10: Noise figure: theoretical values compared with the simulation results.

5.5.2 Voltage Gain Variation

As determined in (5.7) and (5.8), and considering $k^2 \ll 1$, the pole frequencies are independent of α:

$$\begin{cases} \omega_1 \approx \sqrt{\dfrac{1}{L_{11}C_{11}}} \\ \\ \omega_2 \approx \sqrt{\dfrac{1}{L_{22}C_{22}}} \end{cases} \tag{5.18}$$

and the zero frequency depends on α:

$$\omega_z^2 = \frac{L_{11} + \alpha M}{C_{22}(L_{11}L_{22} - M^2)} \tag{5.19}$$

By varying α it is possible to change the zero pair position and place it over one of the pole pairs in order to cancel it. α is changed by varying V_{BIAS2}, while keeping $V_{BIAS1} = V_{DD}$, or by keeping the bias voltages constant and varying the transistors sizes. Varying V_{BIAS2} while keeping V_{BIAS1} constant ensures that the cascode transistor connected directly to the output is always in saturation. If both cascode transistors are equal, α can only vary between 0 and 1; however, if the W/L ratio between the cascode transistors is increased, it is possible to obtain a wider range of variation for α, when varying the bias voltage V_{BIAS2}. From now on, when α varies, it is always assumed that the cascode transistor sizes and V_{BIAS1} are fixed and only V_{BIAS2} changes.

The zero pair frequency has a minimum for $\alpha = 0$, which from (5.5) is:

$$\omega_z^2 = \frac{L_{11}}{C_{22}(L_{11}L_{22} - M^2)} = \frac{1}{C_{22}L_{22}(1 - k^2)} \tag{5.20}$$

Thus, the zero pair, cannot cancel the pole pair due to L_{22} and C_{22}. Note that (5.20) is not valid for $k = 0$ because the output network inductors are independent. As α increases, the zero approaches the higher frequency pole, and there is compensation, $\omega_z = \omega_1$, if:

$$\alpha = \frac{1}{M}\left(\frac{C_{22}L_{22}(1 - k^2)}{C_{11}} - L_{11}\right) \tag{5.21}$$

In figure 5.11 the zero frequency variation with α is represented, using (5.5) and the values listed in table 5.1.

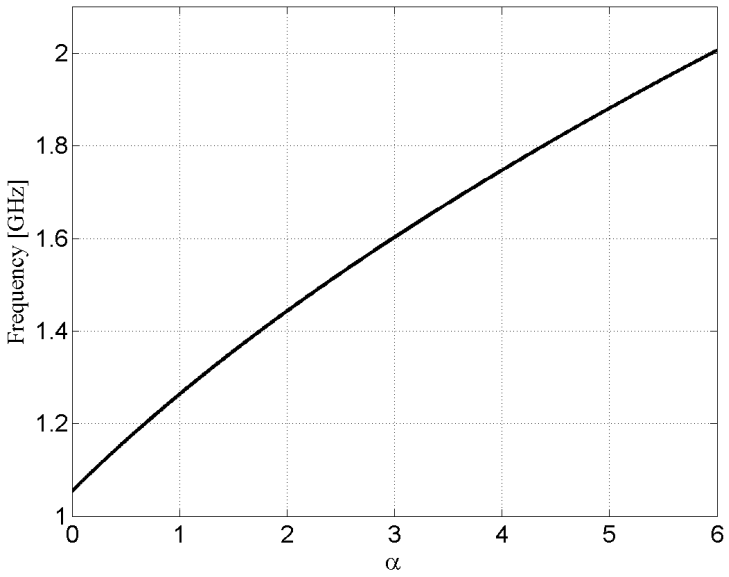

Figure 5.11: Zero frequency versus α.

If the two cascode transistors are equal, α ranges between 0 and 1 and the zero frequency is between 1.1 GHz and 1.3 GHz approximately. This is a small variation, illustrated in figure 5.12. The gain variation at both maxima frequencies reaches almost 7 dB.

When M_{c2} is six times larger than M_{c1}, α ranges from 0 to 6. Observing figure 5.11, the zero frequency is expected to range between 1.1 GHz ($\alpha = 0$) and 2.0 GHz ($\alpha = 6$). It is now possible to cancel the pole pair placed at the higher frequency. There is a large variation of the gain at 1.8 GHz, as shown in figure 5.13, where the second maximum varies around 22 dB, while the first maximum only varies 10 dB, approximately. It is possible to observe the zero frequency moving from 1.1 GHz to 1.8 GHz approximately (the last zero pair frequency is not clear due to the pole cancelation).

By using the output network of figure 5.4 it is not possible to cancel the lower frequency pole, but this is possible by reversing the direction of the magnetic coupling as shown in the next section.

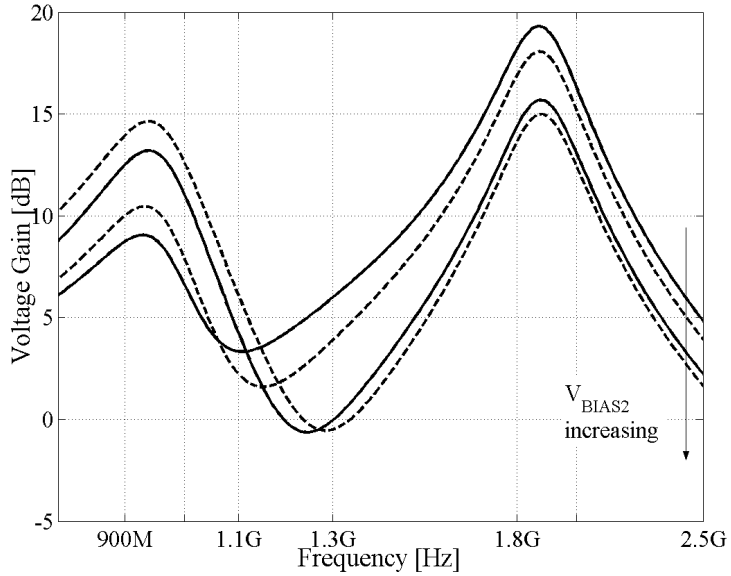

Figure 5.12: Voltage gain with equal cascode transistors: α varies from 0 to 1 ($V_{BIAS1} = V_{DD}$ and $0 \leq V_{BIAS2} \leq V_{DD}$).

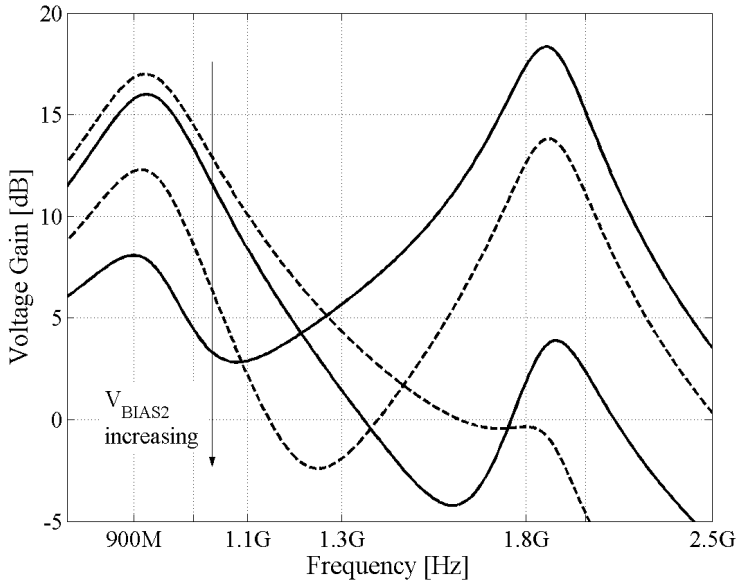

Figure 5.13: Voltage gain with unequal cascode transistors : α varies from 0 to 6 ($V_{BIAS1} = V_{DD}$ and $0 \leq V_{BIAS2} \leq V_{DD}$).

5.6 Effect of Reversing the Orientation of the Magnetic Coupling

One limitation of the dual-band LNA presented in figure 5.4 is that only gain at the higher frequency band can be significantly reduced, since the zero pair cannot overlap the lower frequency pole pair. Canceling the lower frequency pole pair is possible simply by reversing the magnetic inductors coupling orientation, as shown in figure 5.14.

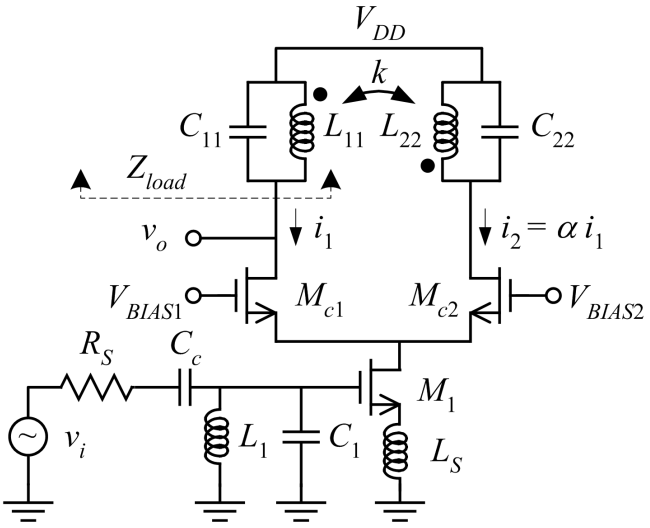

Figure 5.14: Concurrent dual-band LNA topology with opposite magnetic coupling.

Equations (5.1c) to (5.1f) still apply to the circuit of figure 5.14. Only equations (5.1a) and (5.1b) are different:

$$V_1 = sL_{11}I_{l1} - sMI_{l2} \tag{5.22a}$$

$$V_2 = -sMI_{l1} + sL_{22}I_{l2} \tag{5.22b}$$

The load impedance $Z_{load} = V_1/I_1$ becomes

$$Z_{load} = \frac{C_{22}(L_{11}L_{22} - M^2)s^3 + (L_{11} - \alpha M)s}{C_{11}C_{22}(L_{11}L_{22} - M^2)s^4 + (C_{11}L_{11} + C_{22}L_{22})s^2 + 1} \tag{5.23}$$

The only difference between (5.23) and (5.2) is in the sign of the αM term, in the numerator. The poles are the same as before; however, the zero pair is different:

$$\omega_z^2 = \frac{L_{11} - \alpha M}{C_{22}(L_{11}L_{22} - M^2)} = \frac{L_{11} - \alpha M}{C_{22}L_{11}L_{22}(1 - k^2)} \tag{5.24}$$

Using the same values as in the last example, it is shown in figure 5.15 - curve 1 that the zero pair frequency decreases with α (instead of increasing as in figure 5.11). The decreasing slope is higher than the increasing slope; meaning that the same variation in current produces a larger zero frequency variation in this case.

In figure 5.16 the gain variation is represented, and it is visible that the zero pair frequency is always too close to the first pole pair frequency. Consequently the maximum voltage gain at 900 MHz is low even for the lowest value of V_{BIAS1}.

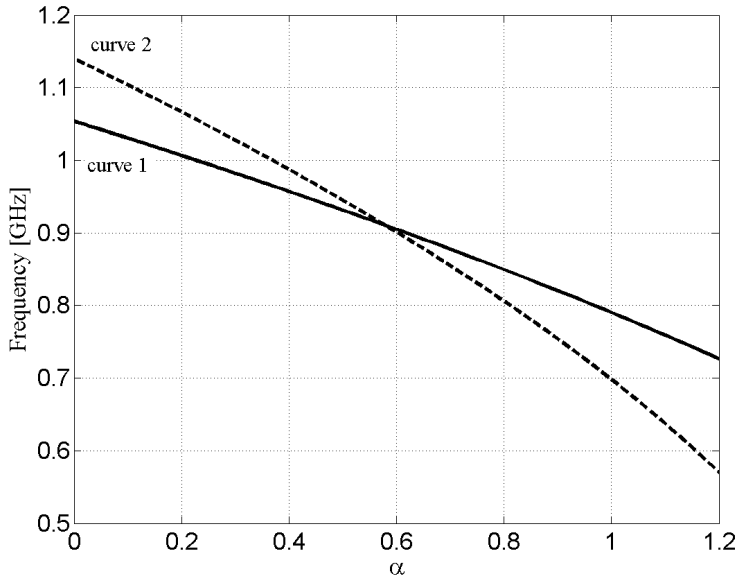

Figure 5.15: Zero position versus α. Curve 1: $k = 0.35$. Curve 2: $k = 0.50$.

Observing (5.24) it is possible to increase the zero pair frequency, when $\alpha = 0$ by increasing k, or by decreasing C_{22} or L_{22}. Since L_{22} is difficult to vary and the value of C_{22} depends on L_{22}, it is simpler to change k. By using $k = 0.50$, the curve 2 of figure 5.15 is obtained. The zero frequency increases almost 100 MHz when $\alpha = 0$. The trade-off of curve 2 is an increase in the slope of the the zero frequency as a function of α. In figure 5.17 the new voltage gain curves variation as function of α are represented. The zero frequency, when $\alpha = 0$, is now closer to the geometrical mean of the pole frequencies, which is approximately 1.27 GHz. In this situation the voltage gain maxima have approximately the same value of 10 dB. The voltage gain variation of the first pole pair frequency is now around 12 dB. Due to the variation of k the lower frequency pole reduced slightly its frequency.

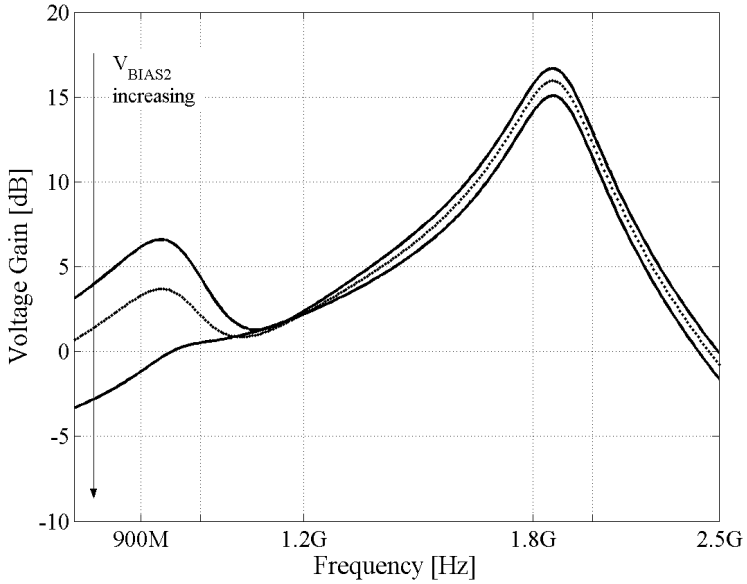

Figure 5.16: Voltage gain frequency response versus α. α in the range 0 to 1 ($V_{BIAS2} \in [1, 1.9]$ V) and $k = 0.35$.

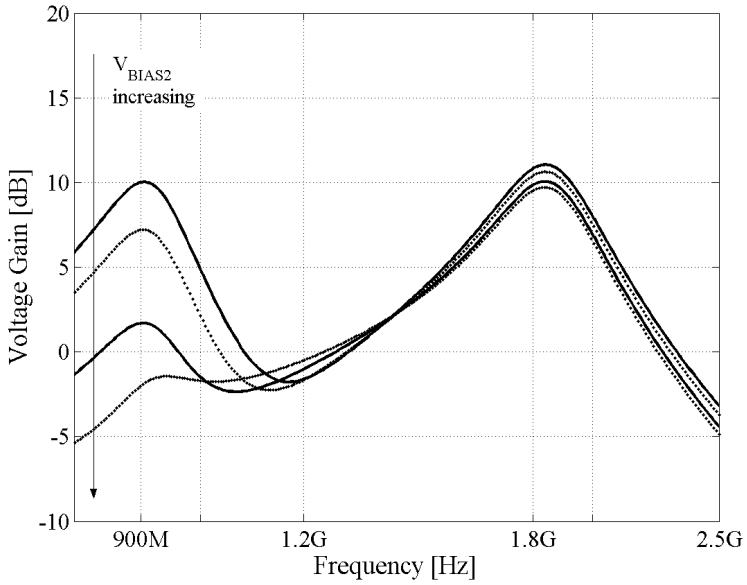

Figure 5.17: Voltage gain frequency response versus α. α in the range 0 to 1 ($V_{BIAS2} \in [1, 1.2]$ V) and $k = 0.50$.

5.7 Conclusions

In this chapter, a new concurrent dual-band LNA with a single input and single output is presented. It is based on a cascode stage using inductive degeneration, with a wideband input impedance matching and two resonant output branches which are magnetically coupled. This circuit allows the current balancing between the two output branches.

Equations for the frequency of the maxima and minimum of the frequency response have been determined. It was shown that the maxima of the frequency response are independent of the current ratio between output branches, but the minimum depends on it. This fact allows the gain variation at each maximum by varying the current ratio.

The current ratio is determined by the DC voltage at the gate of the cascode transistors and by the relative size between those transistors. Thus, by changing the ratio between the cascode transistors width, it is possible to control the range of variation of the current ratio, and with that, obtain a different frequency response. Under certain conditions, it is possible to cancel the voltage gain maximum located at the higher frequency; however, the maximum located at the lower frequency cannot be canceled, which is a limitation of this circuit.

To overcome the problem of canceling the maximum located at the lower frequency, it is proposed a new circuit, which differs only in the magnetic coupling orientation, when compared with the first circuit analyzed. It is shown, that with this circuit it is possible to cancel the lower frequency maximum; however, the ratio of frequency variation of the voltage gain minimum is higher than the first circuit.

Chapter 6

Double Loop Feedback LNA

6.1 Introduction

In chapter 3, it was shown that double loop feedback (DLF) can be applied in the design of low noise amplifiers (LNAs) to have a finite input impedance, suitable gain and good noise performance. Four topologies have been considered, two of which sampling the output voltage and the remaining sampling the output current - figures 3.32, 3.36, 3.37 and 3.38. In this chapter the design of a double loop feedback low noise amplifier (DLF LNA) is developed. The design is divided into two major parts:

1. the feedback network design;
2. the amplifying block design;

In section 6.2 the DLF LNA is analyzed considering all blocks ideal. In section 6.3 the amplifying block is assumed to be ideal, and the influence of the main feedback network non-idealities on the DLF LNA performance is analyzed. After analyzing the feedback network, the possibility of designing an amplifying block, that meets the performance limits determined in section 6.3, is evaluated in section 6.4. In section 6.5 the feedback network and the amplifying block are replaced by real elements, and the DLF LNA is simulated in order to evaluate the reliability of the LNA. In section 6.6 the noise performance of the DLF LNA is evaluated. Finally, in section 6.7, some conclusions are drawn.

6.2 DLF LNA with Ideal Blocks

From the four DLF LNA topologies determined, two of them were partially analyzed at the date of this work (DLF LNAs of figures 3.36 and 3.37). From the remaining topologies, it was chosen the DLF LNA sampling the output voltage because LNAs have more often outputs in voltage suitable to be connected to mixers. The DLF LNA to be analyzed is presented in figure 6.1.

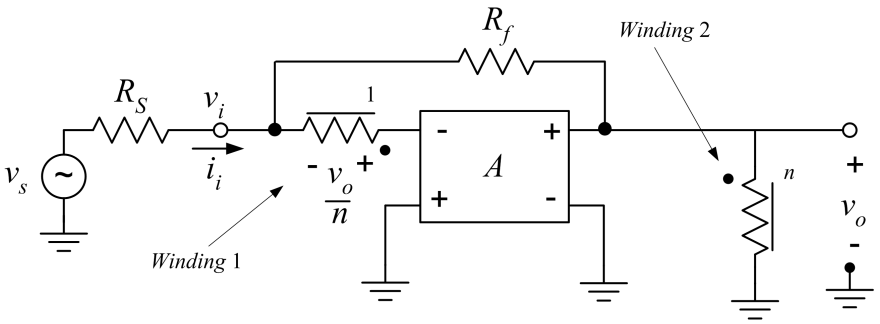

Figure 6.1: DLF LNA type 1, sampling the output voltage.

In this circuit, the transformer samples the output voltage v_o (winding 2), divides it by a factor n, and compares it with the input voltage v_i (winding 1). The resistor R_f samples the output voltage v_o, converts it into a current, which is compared with the input current i_i. The current through R_f is injected at the node between the voltage source and the transformer winding 1; thus, no current flows through this winding. The double loop feedback allows this amplifier to have a finite input impedance, which can be matched to the source impedance.

The input impedance Z_{in} and the voltage gain A_v, assuming an ideal transformer and an ideal amplifying block, are:

$$Z_{in} = \frac{v_i}{i_i} = \frac{R_f}{n+1} \tag{6.1}$$

$$A_v = \frac{v_o}{v_s} = -\frac{n}{2} \tag{6.2}$$

The input impedance matching condition $Z_{in} = R_S = R_f/(n+1)$ will be assumed throughout this chapter. The input referred noise power spectral density, determined

in chapter 3, due exclusively to the feedback resistance R_f is

$$N_i = 4k_BTR_f\left(\frac{R_S}{R_f}\right)^2 = \frac{4k_BTR_S}{n+1} \tag{6.3}$$

which leads to a minimum achievable noise factor of

$$F_{\min} = 1 + \frac{1}{n+1} \tag{6.4}$$

The three main LNA parameters (input impedance (6.1), voltage gain (6.2), and noise factor (6.4)) are all constant and frequency independent. This means that this circuit can be applied to the design of wideband LNAs. Equations (6.2) and (6.4) show that a large n benefits the gain and the noise performance. This is an important design guideline for this LNA.

The transformer model is now complemented with some non-idealities in order to evaluate the performance degradation caused by them.

6.3 Feedback Network Analysis

Assuming an ideal amplifying block, the DLF LNA performance depends only on the feedback network, (6.1) to (6.4). This means that the feedback network should be designed first, considering an ideal amplifying block. Regarding the feedback network, the major concern is the transformer non-idealities.

In figure 6.2 the transformer model to be used in the further analysis is presented. This model corresponds to the ideal transformer (used in last section), to which inductances are added. Using two inductors magnetically coupled (figure 2.26) difficults the analysis. The 2-port **H** matrix of the transformer model of figure 6.2 is:

$$\mathbf{H} = \begin{pmatrix} sL_{w1} & \frac{1}{n} \\ -\frac{1}{n} & \frac{1}{sL_{w2}} \end{pmatrix} \tag{6.5}$$

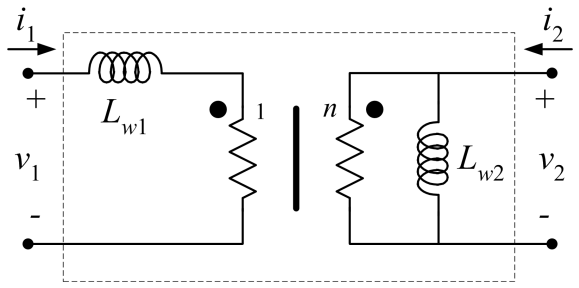

Figure 6.2: Transformer model.

To make the equivalence between the transformer model of figure 6.2 and the transformer model corresponding to two inductors magnetically coupled and discussed in sub-section 2.5.2.2, their **H** matrixes have to be made equal. The equivalence between both matrixes results in next equalities:

- $L_{w1} = L_{11}(1 - k^2)$,
- $L_{w2} = L_{22}$,

The complete transformer model to be used in the DLF LNA analysis is presented in figure 6.3. The non-idealities considered are: the series resistances R_{wi} and the inter-winding capacitances C_{wi}. The transformer non-idealities will establish the lower and upper limit frequencies for the amplifier pass-band.

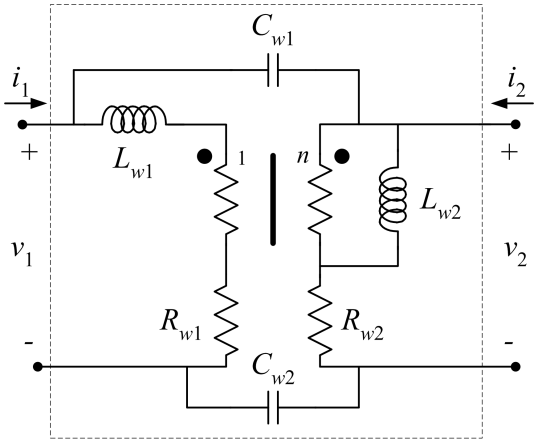

Figure 6.3: Transformer model including winding resistances R_{wi} and inter-winding capacitances C_{wi}

6.3.1 Effect of Inductances L_{wi} and Resistances R_{wi}

Figure 6.4 represents the DLF LNA using a non-ideal transformer modeled by an ideal transformer complemented with inductances L_{wi} and resistances R_{wi}.

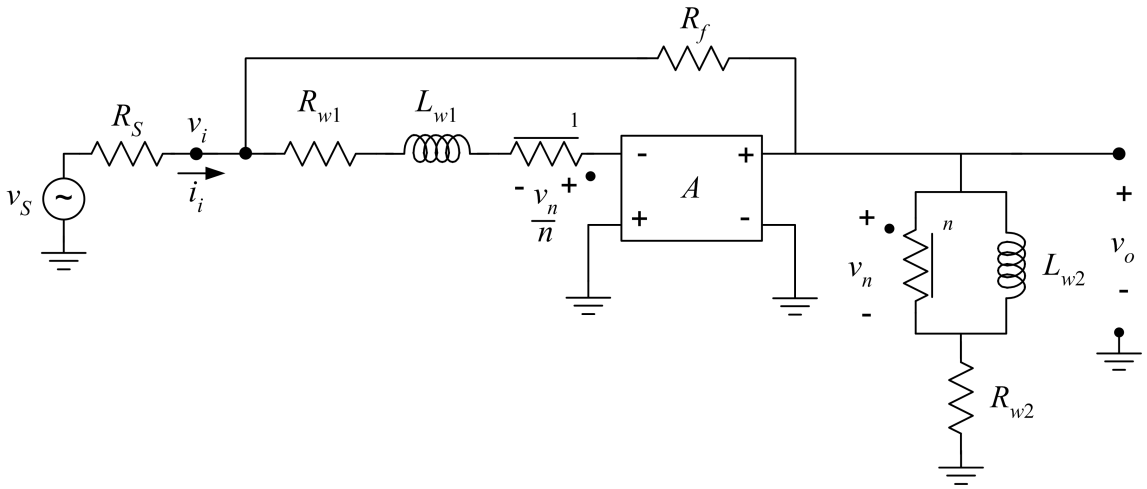

Figure 6.4: DLF LNA with transformer model including inductances L_{wi} and resistances R_{wi}.

The input impedance $Z_{in}(s)$ and the voltage gain $A_v(s)$ are:

$$Z_{in}(s) = \frac{V_i}{I_i}(s) = \frac{R_f s L_{w2}}{(n+1)sL_{w2} + nR_{w2}} = \frac{R_f L_{w2}}{nR_{w2}} \frac{s}{1 + \frac{s}{\omega_{p1,Zin}}} \tag{6.6}$$

$$A_v(s) = \frac{V_o}{V_s}(s) = -\frac{n(n+1)(sL_{w2} + R_{w2})}{2(n+1)sL_{w2} + nR_{w2}} = -(n+1)\frac{\left(1 + \dfrac{s}{\omega_{z1,Av}}\right)}{\left(1 + \dfrac{s}{\omega_{p1,Av}}\right)} \tag{6.7}$$

where $\omega_{p1,Zin}$, $\omega_{z1,Av}$ and $\omega_{p1,Av}$ are

$$\omega_{p1,Zin} = \frac{nR_{w2}}{(n+1)L_{w2}} \tag{6.8}$$

$$\omega_{p1,Av} = \frac{1}{2}\frac{n}{n+1}\frac{R_{w2}}{L_{w2}} \tag{6.9}$$

$$\omega_{z1,Av} = \frac{R_{w2}}{L_{w2}} \tag{6.10}$$

The first major difference between the input impedance and voltage gain equations determined for the ideal case and equations (6.6) and (6.7) is the frequency dependence of these two network functions. L_{w1} and R_{w1} do not appear in these equations, because the input impedance of the amplifying block is infinite and no current flows through winding 1. This is an advantage that results from the injection of the feedback current on the node between the voltage source and the transformer winding 1. L_{w2} and R_{w2} produce a pole and a zero in both functions, and the asymptotic Bode plots are shown in figures 6.5 and 6.6.

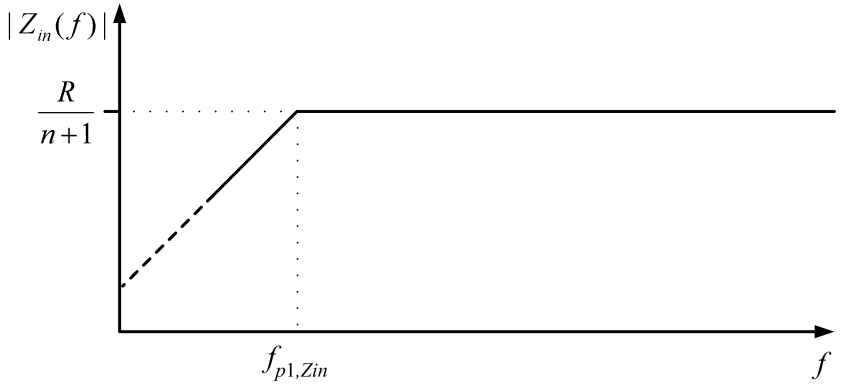

Figure 6.5: Asymptotic Bode plot of the input impedance $|Z_{in}(f)|$ of the DLF LNA considering the transformer inductances L_{wi} and resistances r_{wi}.

Among the poles and zeros of both functions (input impedance and voltage gain),

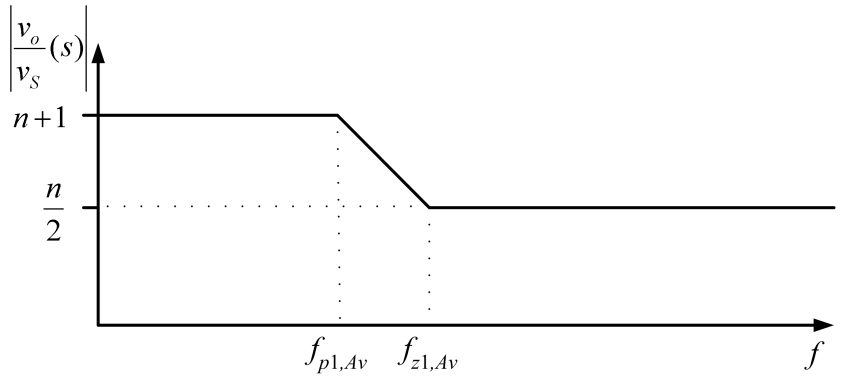

Figure 6.6: Asymptotic Bode plot of the DLF LNA voltage gain $|A_v|$ considering the transformer inductances L_{wi} and resistances r_{wi}.

the zero $\omega_{z1,Av}$ of the voltage gain is placed at the highest frequency. For frequencies above $f_{z1,Av}$, the DLF LNA voltage gain and input impedance equal the constant values determined in (6.1) and (6.2); thus $f_{z1,Av}$ determines the lower frequency of the DLF LNA pass-band.

$$f_{\min} = \frac{1}{2\pi}\frac{R_{w2}}{L_{w2}} \tag{6.11}$$

Concerning noise, the parasitic resistances r_{wi} are a new source of noise, as represented in figure 6.7.

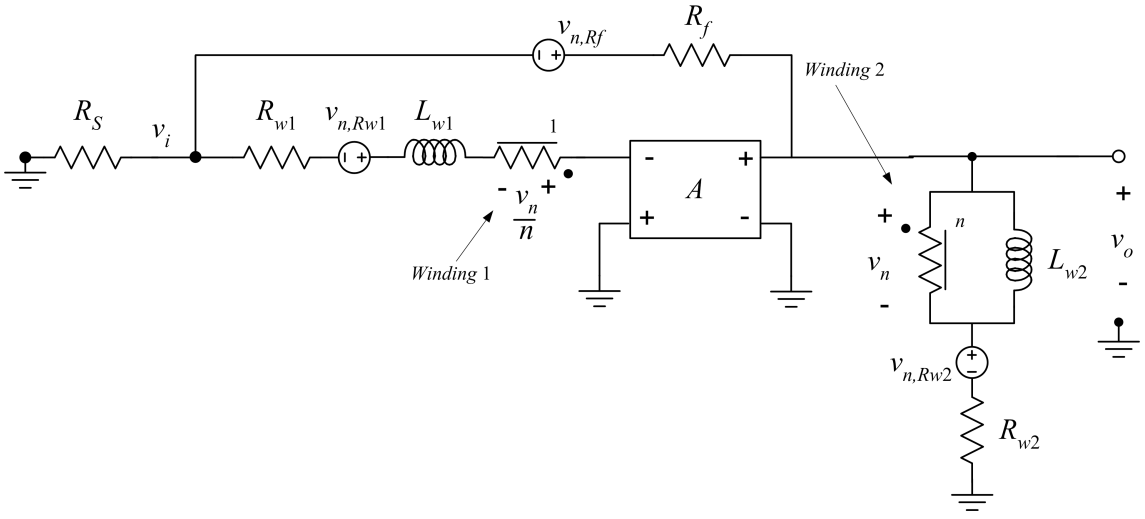

Figure 6.7: DLF LNA noise sources.

This extra noise is accounted for the following equation of the input noise power

spectral density:

$$N_i = 4k_BT[R_f + R_{w2} + R_{w1}]\left(\frac{1}{n+1}\right)^2 + 4k_BTR_{w1} \tag{6.12}$$

(6.12) is demonstrated in appendix D. Considering that $R_f \gg R_{wi}$ and $i \in \{1, 2\}$, these resistances can be neglected in the first term. R_{w2} is not relevant to the overall noise; however, the noise contribution of R_{w1} is fully present at the input (there is no attenuation by the topology). The minimum noise factor achievable by this topology is now:

$$F = 1 + \frac{N_i}{N_S} \approx 1 + \frac{1}{n+1} + \frac{R_{w1}}{R_S} \tag{6.13}$$

which shows the importance of keeping R_{w1} with a low value.

6.3.2 Effect of Inter-Winding Capacitances C_{wi}

The inter-winding parasitic capacitances C_{w1} and C_{w2} model the capacitance existing between the two transformer windings and are represented in figure 6.8. Assuming that $n \gg 1$, $C_{w2} = C_{w1}$, and $R_f = R_S(n+1)$, the position of poles and zeros of the input impedance $|Z_{in}(s)|$ and voltage gain $A_v(s)$ is defined by (6.14) and (6.15). The complete determination of poles and zeros of (6.14) and (6.15) is described in appendix B.

$$\text{Input Impedance:} \begin{cases} \omega_{z1,Zin} = 0 \\ \omega_{p1,Zin} = -\dfrac{n}{n+1}\dfrac{R_{w2}}{L_{w2}} \\ \omega_{p2,Zin} = -\dfrac{1}{R_f C_{w1}} \\ \omega^2_{p3,Zin} \approx \dfrac{1}{nL_{w1}C_{w1}}, \qquad Q_{p2,Zin} \approx \dfrac{1}{R_{w1}}\dfrac{1}{\sqrt{n}}\sqrt{\dfrac{L_{w1}}{C_{w1}}} \\ \omega^2_{z2,Zin} \approx \dfrac{1}{L_{w1}C_{w1}}, \qquad Q_{z2,Zin} \approx \dfrac{1}{R_{w1}}\sqrt{\dfrac{L_{w1}}{C_{w1}}} \end{cases} \tag{6.14}$$

$$\text{Voltage Gain:} \begin{cases} \omega_{p1,Av} = \dfrac{1}{2}\dfrac{n}{n+1}\dfrac{R_{w2}}{L_{w2}} \\ \omega_{z1,Av} = \dfrac{R_{w2}}{L_{w2}} \\ \omega^2_{p2,Av} \approx \dfrac{1}{nL_{w1}C_{w1}}, \qquad Q_{p2,Av} \approx \dfrac{1}{R_S}\sqrt{\dfrac{2}{n}}\sqrt{\dfrac{L_{w1}}{C_{w1}}} \\ \omega_{p3,Av} \approx -\dfrac{1}{R_S C_{w1}} \end{cases} \tag{6.15}$$

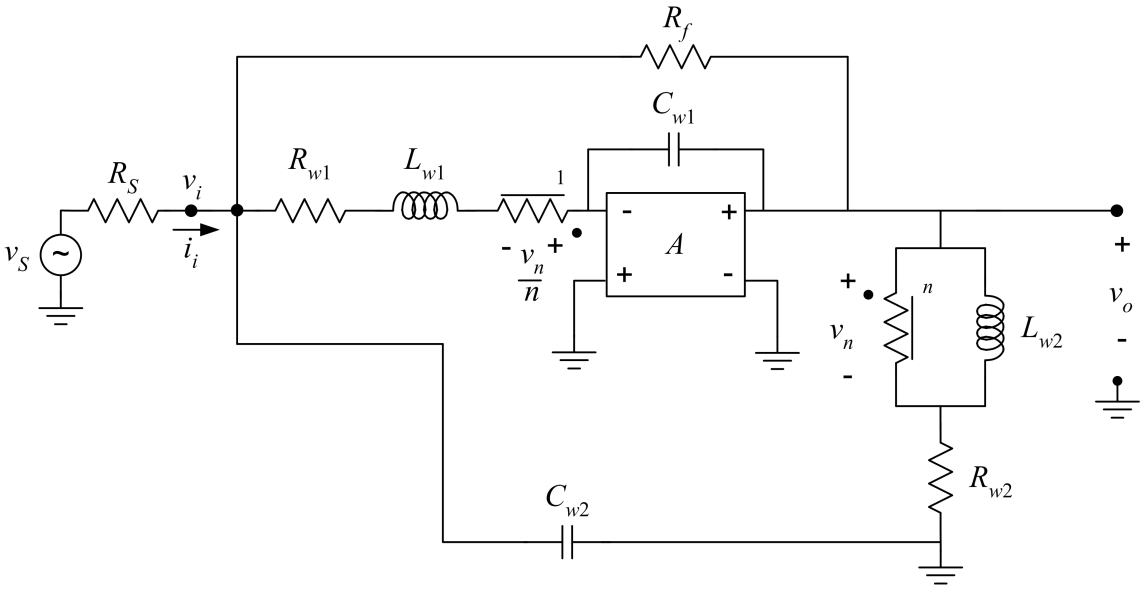

Figure 6.8: DLF LNA with transformer model including inductances L_{wi}, resistances R_{wi} and, inter-winding capacitances C_{wi}.

Figures 6.9 and 6.10 show possible plots of the input impedance $|Z_{in}(s)|$ and the voltage gain $(v_o/v_s)(s)$ of the DLF LNA.

The input impedance has a zero at the origin and a low frequency pole, both caused by L_{w2} and R_{w2}. This pole defines the lower limit of the frequency range in which the input impedance has the desired value for impedance matching. The upper limit of this range is determined by another pole caused by the source resistance R_S and parasitic capacitances C_{w1} and C_{w2}. Above this frequency, one pair of complex poles and one pair of complex zeros are observed. The influence of the

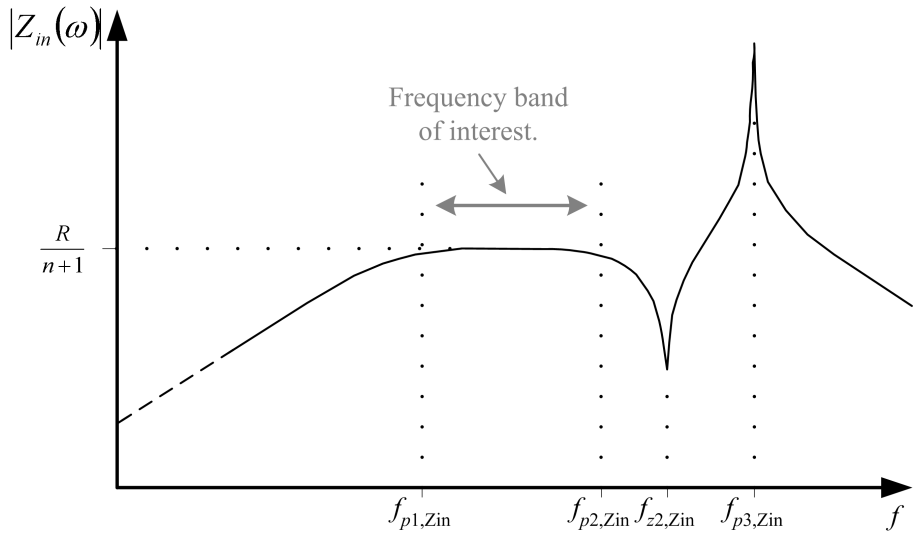

Figure 6.9: Possible plot of the DLF LNA input impedance considering the complete transformer model including inductances, resistances and capacitances.

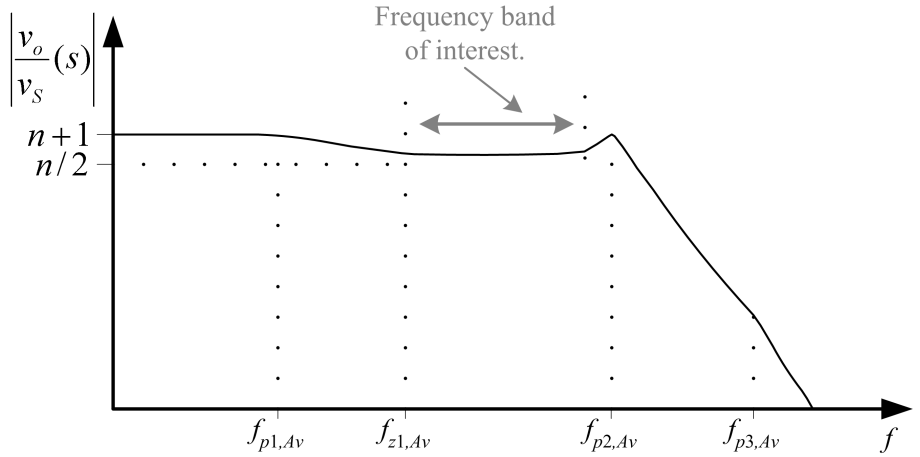

Figure 6.10: Possible plot of the DLF LNA voltage gain considering the complete transformer model including inductances, resistances and capacitances.

transformer winding 1 is now present, due to the leakage of current through it and via the parasitic capacitances; thus, these capacitances are an important design variable and should be minimized in the transformer implementation. The transfer function $A_v(s)$ has one pole and one zero at low frequencies, both caused by the winding 2 inductance L_{w2} and its series resistance R_{w2}. The amplifier bandwidth is upper limited by a complex pole pair, with a frequency determined by L_{w1}, the parasitic capacitances between windings, and n. This shows again the influence of these capacitances and the importance of reducing their value. An additional pole, caused by the source resistance R_S and the capacitances C_{w1} and C_{w2} is visible, but it is out of the frequency range of interest.

The bandwidth for which the input impedance is approximately $R_f/(n+1)$ is determined by poles $\omega_{p1,Zin}$ and $\omega_{p2,Zin}$; the bandwidth where the voltage gain has approximately the expected value of $n/2$ is determined by the first zero, of frequency $\omega_{z1,Av}$, and the complex poles of frequency $\omega_{p2,Av}$. The LNA useful bandwidth is determined by the intersection of these two ranges.

Until now, the DLF LNA analysis has been made considering an ideal amplifying block (nullor). The analysis in the following section considers the amplifying block non-idealities and their influence on the DLF LNA performance. The objective is to establish the specifications for the amplifying block, so that it can be considered as a nullor.

6.4 Amplifying Block Analysis

In this section the consequences of having a non-ideal amplifying block are analyzed. The emphasis of this analysis is on the effect of the amplifying block non-idealities on the main LNA parameters.

6.4.1 Input Impedance and Voltage Gain Evaluation using a Non-Ideal Amplifying Block

The amplifying block is represented by the model in figure 6.11.

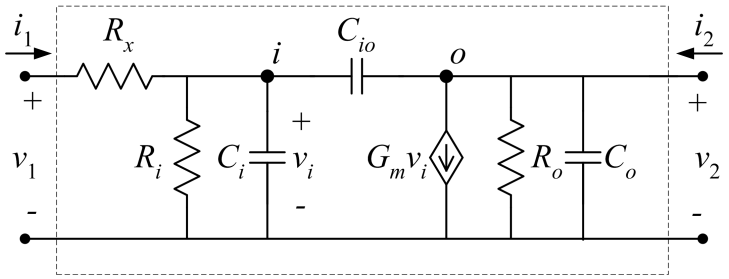

Figure 6.11: General amplifier model.

The 2-port **H** parameter matrix of the general amplifier model of figure 6.11 is:

$$\mathbf{H}_{Amp} = \begin{pmatrix} R_x + \dfrac{1}{Y_i + sC_{io}} & \dfrac{sC_{io}}{Y_i + sC_{io}} \\ \dfrac{G_m - sC_{io}}{Y_i + sC_{io}} & Y_o + sC_{io} + \dfrac{(G_m - sC_{io})sC_{io}}{Y_i + sC_{io}} \end{pmatrix} \tag{6.16}$$

where

$$Y_o = \frac{1}{R_o} + sC_o \tag{6.17}$$

and

$$Y_i = \frac{1}{R_i} + sC_i \tag{6.18}$$

From (6.16) it is possible to determine all the other matrix descriptions, using transformation rules [43]. In practical implementations, R_x has a low value compared with $\left|\frac{1}{Y_i+sC_{io}}\right|$ and, thus, it can be neglected in circuit analysis; however, it should

be considered in noise analysis, because the noise generated by it is not negligible in comparison with the other noise sources. The amplifying block without R_x is shown in figure 6.12 and its **H** matrix is

$$\mathbf{H}_A = \begin{pmatrix} \dfrac{1}{Y_i + sC_{io}} & \dfrac{sC_{io}}{Y_i + sC_{io}} \\ \dfrac{G_m - sC_{io}}{Y_i + sC_{io}} & Y_o + sC_{io} + \dfrac{(G_m - sC_{io})sC_{io}}{Y_i + sC_{io}} \end{pmatrix} \tag{6.19}$$

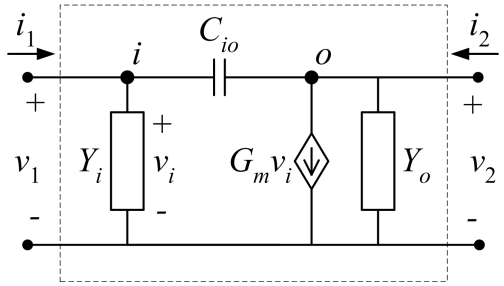

Figure 6.12: Simplified amplifier model for circuit analysis.

The most suitable matrix description for the series-shunt feedback configuration is the **H** matrix, while for the shunt-shunt configuration is the **Y** matrix [43]. The **H** matrices of the amplifier and transformer are determined first, because the transformer feedback loop is inside the resistor feedback loop. The **H** matrices are added and convert into an **Y** matrix, that will be added to the feedback resistor **Y** matrix.

The transformer is represented in figure 6.13 and its **H** matrix is

$$\mathbf{H}_T = \begin{pmatrix} sL_{11}(1-k^2) & -\dfrac{1}{n} \\ \dfrac{1}{n} & \dfrac{1}{sL_{22}} \end{pmatrix} \tag{6.20}$$

Addition of (6.19) and (6.20) results in:

$$\mathbf{H}_{A,T} = \mathbf{H}_A + \mathbf{H}_T \tag{6.21}$$

$$\begin{pmatrix} \dfrac{1}{Y_i + sC_{io}} + sL_{11}(1-k^2) & \dfrac{sC_{io}}{Y_i + sC_{io}} - \dfrac{1}{n} \\ \dfrac{G_m - sC_{io}}{Y_i + sC_{io}} + \dfrac{1}{n} & Y_o + sC_{io} + \dfrac{(G_m - sC_{io})sC_{io}}{Y_i + sC_{io}} + \dfrac{1}{sL_{22}} \end{pmatrix}$$

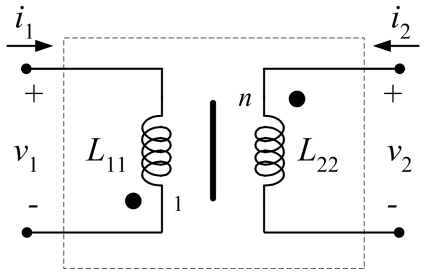

Figure 6.13: Transformer used in the DLF LNA of figure 6.1.

In practical cases,

$$\left|\frac{1}{Y_i + sC_{io}}\right| \gg \left|sL_{11}(1-k^2)\right| \tag{6.22}$$

The matrix $\mathbf{H}$ of (6.21) is now converted to the corresponding $\mathbf{Y}$ matrix [43], in order to be added to the $\mathbf{Y}$ matrix of the feedback block formed by R_f:

$$\mathbf{Y}_{A,T} = \begin{pmatrix} \dfrac{1}{h_{11}} & -\dfrac{h_{12}}{h_{11}} \\ \dfrac{h_{21}}{h_{11}} & \dfrac{\det \mathbf{H}}{h_{11}} \end{pmatrix} = \tag{6.23}$$

$$= \begin{pmatrix} sC_{io} + Y_i & \dfrac{1-n}{n} sC_{io} + \dfrac{Y_i}{n} \\ G_m + \dfrac{1-n}{n} sC_{io} + \dfrac{Y_i}{n} & \dfrac{G_m}{n} + Y_o + \dfrac{1}{sL_{22}} + \dfrac{n^2-1}{n^2} sC_{io} + \dfrac{Y_i}{n^2} \end{pmatrix}$$

The feedback block formed by R_f is represented in figure 6.14 and its $\mathbf{Y}$ matrix is

$$\mathbf{Y}_{R_f} = \begin{pmatrix} \dfrac{1}{R_f} & -\dfrac{1}{R_f} \\ -\dfrac{1}{R_f} & \dfrac{1}{R_f} \end{pmatrix} \tag{6.24}$$

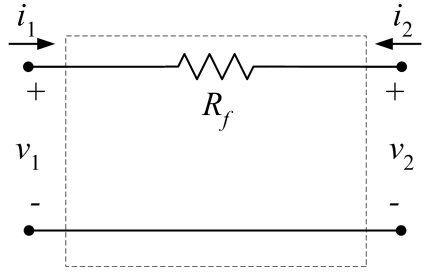

Figure 6.14: Feedback block formed by R_f used in the DLF LNA of figure 6.1.

Adding $\mathbf{Y}_{Amp,T}$ of (6.23) and $\mathbf{Y}_{R_f}$ of (6.24), and assuming that $n^2 \gg 1$, results in:

$$\begin{aligned}\mathbf{Y}_{\text{LNA}} &= \mathbf{Y}_{A,T} + \mathbf{Y}_{R_f} = \\ &= \begin{pmatrix} sC_{io} + Y_i + \dfrac{1}{R_f} & \xi sC_{io} + \dfrac{Y_i}{n} - \dfrac{1}{R_f} \\ \\ G_m + \xi sC_{io} + \dfrac{Y_i}{n} - \dfrac{1}{R_f} & \dfrac{G_m}{n} + Y_o + \dfrac{1}{sL_{22}} + sC_{io} + \dfrac{1}{R_f} \end{pmatrix}\end{aligned} \tag{6.25}$$

where $\xi = \frac{1-n}{n}$.

This matrix is used to determine the input admittance:

$$Y_{in} = \frac{I_i}{V_i} = y_{11} - \frac{y_{12}y_{21}}{y_{22} + Y_l} \tag{6.26}$$

and voltage gain of the DLF LNA:

$$A_v = \frac{V_o}{V_i} = -\frac{y_{21}}{y_{22} + Y_l} \tag{6.27}$$

where Y_l is the load admittance. As the DLF LNA has a low output impedance it is assumed that $Y_l \ll y_{22}$. Y_{in} and A_v are:

$$\begin{aligned}Y_{in}(s) &= nsC_{io} + Y_i + \frac{1}{R_f} + \\ &- \frac{sL_{22}(Y_iR_f + (1-n)R_fsC_{io} - n)(Y_iR_f + nG_mR_f + (1-n)R_fsC_{io} - n)}{nR_f(nR_f + sL_{22}(n + G_mR_f + nsC_{io}R_f + nY_oR_f))}\end{aligned} \tag{6.28}$$

$$A_v(s) = -\frac{sL_{22}(Y_iR_f + nG_mR_f + (1-n)R_fsC_{io} - n)}{nR_f + sL_{22}(n + G_mR_f + nsC_{io}R_f + nY_oR_f)} \tag{6.29}$$

If the amplifying block transconductance G_m is very high:

$$\lim_{G_m \to \infty} Y_{in} = \frac{1+n}{R_f} + nsC_{io} \tag{6.30}$$

$$\lim_{G_m \to \infty} \frac{V_o}{V_i} = -n \tag{6.31}$$

Equation (6.30) shows that it is not possible to obtain a purely resistive input admittance, due to C_{io}, even if the amplifying block gain is infinite; Thus, C_{io} should be reduced, or canceled. From (6.31) it is noted that when the amplifer transconductance is very high the voltage gain does not depend on C_{io}.

If C_{io} can be neglected in (6.30),

$$\frac{n+1}{R_f} \gg |nsC_{io}| \tag{6.32}$$

Then,

$$Y_{in} \approx Y_i + \frac{1}{R_f} - \frac{sL_{22}(Y_iR_f - n)(Y_iR_f + nG_mR_f - n)}{nR_f(nR_f + sL_{22}(n + G_mR_f + nY_oR_f))} \tag{6.33}$$

$$A_v \approx -\frac{sL_{22}(Y_iR_f + nG_mR_f - n)}{nR_f + sL_{22}(n + G_mR_f + nY_oR_f)} \tag{6.34}$$

In the following, it is assumed that C_{io} is negligible, and, the conditions for which the gain of the amplifying block is high enough, for it to be assumed to be ideal, will be determined.

6.4.2 Conditions for an Ideal Amplifying Block

In equation (6.33) the terms with G_m will dominate if G_m is higher than a certain value. When G_m is high enough, the third term tends to $n/R_f - Y_i$, leading to $Y_{in} = (n+1)/R_f$. To approach this limit three conditions have to be satisfied:

- condition 1: $|nG_mR_f| \gg |Y_iR_f - n| \Leftrightarrow G_m \gg \left|\frac{Y_i}{n} - \frac{1}{R_f}\right|$
- condition 2: $|G_mR_f| \gg |nR_fY_o + n| \Leftrightarrow G_m \gg \left|n\left(Y_o + \frac{1}{R_f}\right)\right|$

If condition 2 is satisfied then a third condition has to be verified to guarantee an approximation to (6.1):

- condition 3: $|G_m R_f s L_{22}| \gg |nR_f| \Leftrightarrow |G_m| \gg \left|\frac{n}{sL_{22}}\right|$

Using (2.55), condition 3 can be rewritten as:

- condition 3: $G_m \gg \left|\frac{1}{k}\frac{1}{s\sqrt{L_{11}L_{22}}}\right|$

Condition 3 gives a guideline for the transformer design: for a given n, large inductances are preferable, since the condition is satisfied for a lower G_m[1].

If Y_i and Y_o are negligible in conditions 1 and 2, they can be reduced to:

- condition 1': $G_m \gg \left|-\frac{1}{R_f}\right|$
- condition 2': $G_m \gg \left|\frac{n}{R_f}\right|$

In conditions 1 to 3, three inequations are determined. The second term of these three conditions is represented in figure 6.15 together with a dotted line representing the maximum of these three terms. Condition 3 dominates at low frequencies, while condition 2 dominates at high frequencies (the graphic assumes that $|nY_o| > |Y_i/n|$). The point **A** of figure 6.15 corresponds to the point where both conditions intercept. If the intercept point **A** happens at a frequency lower than the point from which the influence of $|nY_o|$ starts, then **A** corresponds to an admittance of n/R_f. This value is approximately the source impedance R_S in an impedance matching condition, $Z_{in} = R_f/(n+1) = R_S$. It is concluded that, in an input impedance matching situation, the amplifying block transconductance G_m must be at least one decade above the source admittance $1/R_S$ to consider the amplifying block as ideal. The minimum value of G_m dominates for the minimum bandwidth (between ω_1 and ω_2). If an higher value of G_m is used, then the bandwidth, for which the amplifying block can be considered ideal, increases (band between ω_1' and ω_2').

[1] In other words, having two transformers with same n it is preferable to use the one that has larger inductances because it lowers the transconductance needed; and thus, (eventually) saving power - G_m is typically directly related to power. This should be traded with other transformer non-idealities and their influence on the overall DLF LNA performance.

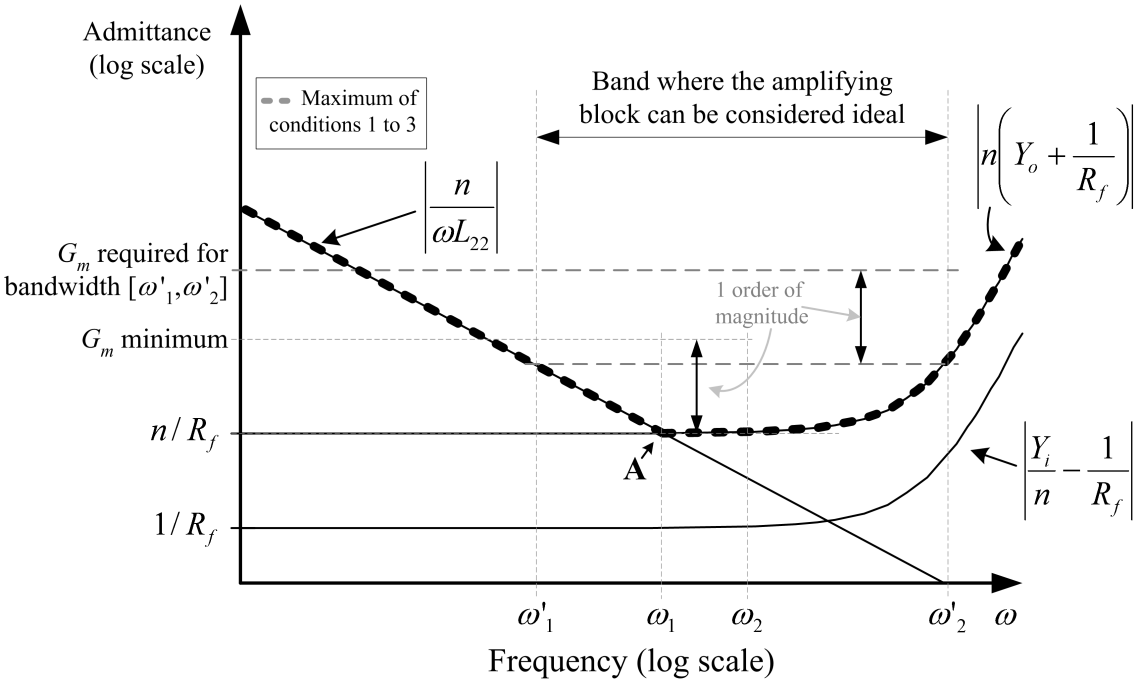

Figure 6.15: Conditions 1 to 3 along frequency and representation of the minimum G_m determination.

With respect to the voltage gain and using (6.34), the transconductance boundaries, where amplifying block can be considered ideal, lead also to conditions 1 to 3.

In next section, a complete DLF LNA is sized and simulated. The transformer is sized using technology parameters and the amplifying block is replaced by a circuit using transistors. Simulations will evaluate the theory developed in this section and will attest if the DLF LNA is realizable.

6.5 Simulation Results

In this section, practical considerations concerning the design of a DLF LNA are developed. The DLF LNA design is divided into two successive tasks:

1. feedback network design;
2. amplifying block design.

In the example here, the AMS 0.35 μm BiCMOS SiGe technology is choosen because it was available (under the project RF Chameleon). Bipolar transistors were preferred since they have higher transconductance than CMOS transistors for the same bias current.

6.5.1 Feedback Network Design

Assuming an ideal amplifying block and an ideal transformer the DLF LNA input impedance is given by (6.1):

$$Z_{in} = \frac{R_f}{n+1} \tag{6.35}$$

To have matched input impedance, Z_{in} must equal the source impedance R_S, which leads to

$$R_f = (n+1)R_S \tag{6.36}$$

The voltage gain, $A_v = -n/2$, given by (6.2), is proportional to $n = \frac{1}{k}\sqrt{\frac{L_{22}}{L_{11}}}$, which in an integrated circuit is limited. A large n requires either large L_{22} or small L_{11}, but a large inductance leads to a large series resistance and a large area, and a small inductance is not accurate (reliably feasible in integrated circuits). An alternative is to have a low magnetic coupling coefficient k; however, if it is made too low, inductors become independent. The integrated transformer dimensioning will be presented in chapter 7. Its parameters are listed in table 6.1, and will be used in the LNA design.

Using the values of table 6.1, and considering the standard 50 Ω value for the source impedance, $R_f = 457.5\ \Omega$ is obtained from (6.36). The poles and zeros of the input impedance and voltage gain determined by (6.14) and (6.15), are listed in table 6.2. With these values, it is possible to estimate the band in which the DLF LNA has a constant impedance at high gain. This band is from 140 MHz to 5.8 GHz.

Table 6.1: Transformer parameters.

Parameter	Value
L_{11}	0.98 nH
$L_{w1} = L_{11}(1 - k^2)$	0.64 nH
$L_{22} = L_{w2}$	22.65 nH
r_{w1}	9.8 Ω
r_{w2}	20.5 Ω
C_{w2}	60 fF
k	0.59
n	8.15

Table 6.2: Frequencies of the poles and zeros determined in (6.14) and (6.15).

Input Impedance		Voltage Gain	
$f_{z1,zin}$	0 Hz	$f_{p1,av}$	64 MHz
$f_{p1,zin}$	120 MHz	$f_{z1,av}$	140 MHz
$f_{p2,zin}$	5.8 GHz	$f_{p2,av}$	9.0 GHz
$f_{p3,zin}$	9.0 GHz	$f_{p3,av}$	53.1 GHz
$f_{z2,zin}$	25.7 GHz		

6.5.2 Amplifying Block Design

The amplifying block can be designed in order to be approximately ideal using the guidelines obtained in section 6.4. The design flow can be divided into:

1. topology definition;

2. transistor sizing and biasing.

In the topology definition, the number of stages of the amplifying block and the configuration of each stage have to be choosen. A single stage topology is choosen for the following reasons:

- for high frequency performance, circuit complexity should be kept low;

- a single stage amplifier does not require frequency compensation;

- more than one stage increases the complexity of the biasing circuits.

The simplest choice is the common emitter stage; however, it is impossible to cancel the feed-forward effect of C_μ with it [122].

The cascode stage will be used to reduce the feed-forward effect of C_μ. The cascode stage is represented in figure 6.16 and its approximate incremental circuit is represented in figure 6.17 [42, 89].

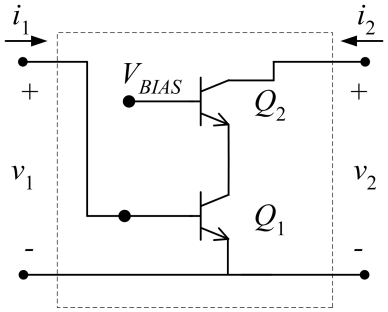

Figure 6.16: Cascode stage.

This topology reduces the Miller effect due to $C_{\mu 1}$, improves the reverse isolation of the amplifier, and increases the amplifying block output impedance in comparison with the common emitter stage [85–89]. Resistances R_{b1} and R_{b2} are neglected. It is also considered that the input-output capacitance (between b_1 and c_2) is negligible.

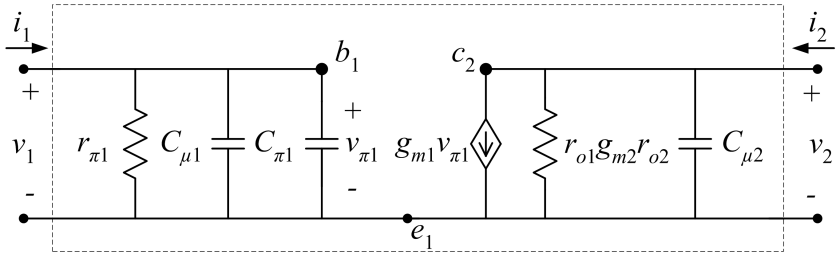

Figure 6.17: Simplified incremental model of the cascode stage.

Y_i and Y_o, are

$$Y_i = \frac{1}{R_{\pi 1}} + s(C_{\pi 1} + C_{\mu 1}) \tag{6.37}$$

and

$$Y_o = \frac{1}{r_{o1} g_{m2} r_{o2}} + sC_{\mu 2} \tag{6.38}$$

The transconductance g_m of a bipolar transistor is mainly proportional to its collector current I_C:

$$g_m = \frac{I_C}{V_T} \tag{6.39}$$

where V_T is the thermal voltage[2]. Thus, g_{m1} determines the power consumption of the amplifying block.

Conditions 1 to 3, in section 6.4 define the g_{m1} boundaries for which the amplifying block is approximately ideal. The minimum value of g_{m1} is determined by the three conditions, while the maximum value is limited by the power consumption. The g_{m1} minimum value is determined analytically by the minimum value that satisfies the three inequations of (6.40).

$$\begin{cases} g_{m1} \gg \left| \dfrac{Y_i}{n} - \dfrac{1}{R_f} \right| \\ g_{m1} \gg \left| nY_o + \dfrac{n}{R_f} \right| \\ g_{m1} \gg \left| \dfrac{n}{sL_{22}} \right| \end{cases} \tag{6.40}$$

Y_i and Y_o are given respectively by (6.37) and (6.38).

It was concluded in subsection 6.4.2 that g_{m1} should be much higher than the source admittance $1/R_S$. Assuming that a value for g_{m1} greater than one order above the source admittance is enough, means that the minimum g_{m1} that satisfies inequations (6.40) is approximately 0.2 S, obtainable with a current of approximately 5 mA for the bipolar transistor. In figure 6.18, $g_{m1} = 0.2$ mS is represented together with the second term of the three inequations of (6.40). Values used in inequations were determined by simulation, using a biasing collector current $I_{C1} = 5$ mA, and are listed in table 6.3. The transistor model used in simulations is the Gummel-Poon, Q_1 and Q_2 have an emitter length of 24 μm and 16 μm respectively, and both transistors have an emitter width of 0.4 μm [123]. From figure 6.18, it is visible that condition 3 is the most restrictive for low frequencies while condition 2 is the one that dominates at higher frequencies.

Figures 6.19 and 6.20 represent the real and the imaginary part of the input impedance. By comparing the theoretical curves (dotted lines) and the simulation curves (solid lines), it is visible that for a certain frequency range the real part is close to 50 Ω, while the imaginary has a lower value. This corresponds approximately to the zone where g_{m1} validates the three inequations of (6.40), as visible in figure 6.18. The different curves of figures 6.19 and 6.20 correspond to different

[2]The thermal voltage V_T is equal to $\frac{k_B T}{q}$ and is typically determined at a temperature T of 300 K giving approximately 25 mV.

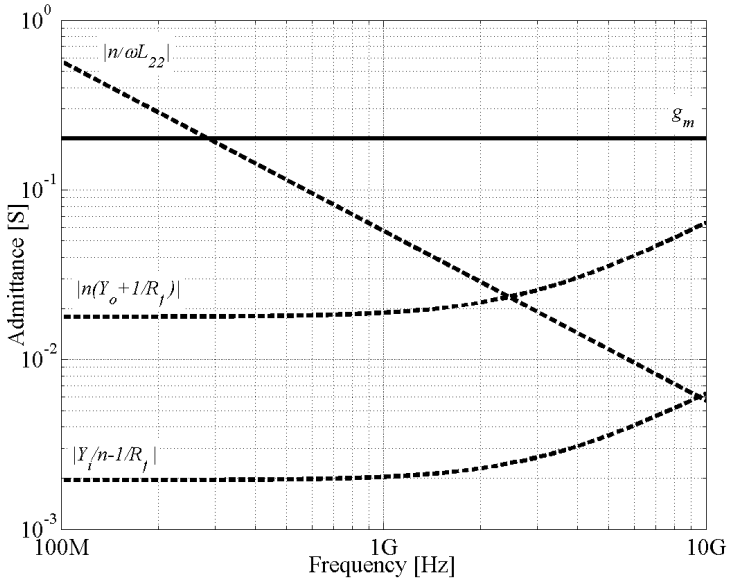

Figure 6.18: Amplifying block transconductance and conditions 1 to 3. Transconductance determined for a current of 5 mA and condition curves determined with values of table 6.3.

Table 6.3: Bipolar cascode incremental parameters.

Model Element	Value	Model Element	Value
r_{o2}	71.43 Ω	$R_{\pi 1}$	1021 Ω
g_{m2}	0.167 mS	$C_{\pi 1}$	346 fF
r_{o1}	94.25 Ω	g_{m1}	0.174 S
R_{b1}	20 Ω	$C_{\mu 2}$	60 fF

values of g_{m1} between 0.09 S and 0.33 S, that correspond to a collector current between 2.5 mA and 10.0 mA. It is visible that higher values of transconductance g_{m1} correspond to an input impedance closer to real 50 Ω. It is also visible that the theoretical model follows the simulation results, which means a good approximation between the theoretical and simulated curves. This means that the estimated minimum value of $g_{m1} \approx 0.2$ S is enough to consider the amplifying block as ideal. In figure 6.21 the S_{11} parameter is represented, which is well below -10 dB for the above referred frequency range. When g_{m1} increases, S_{11} decreases, meaning that the input impedance matching improves. Figure 6.22 represents the voltage gain and it can be seen that the theoretical model and the simulation plots have a difference of approximately 1 dB, for an absolute value above 16 dB, for the zone where g_{m1} dominates.

The simulations do not take into account the transformer inter-winding capacitances C_{wi}, because they have not been considered for the theoretical curves, and they only serve to validate the theory. In next chapter, the DLF LNA is simulated considering the complete models for the amplifying block and feedback network.

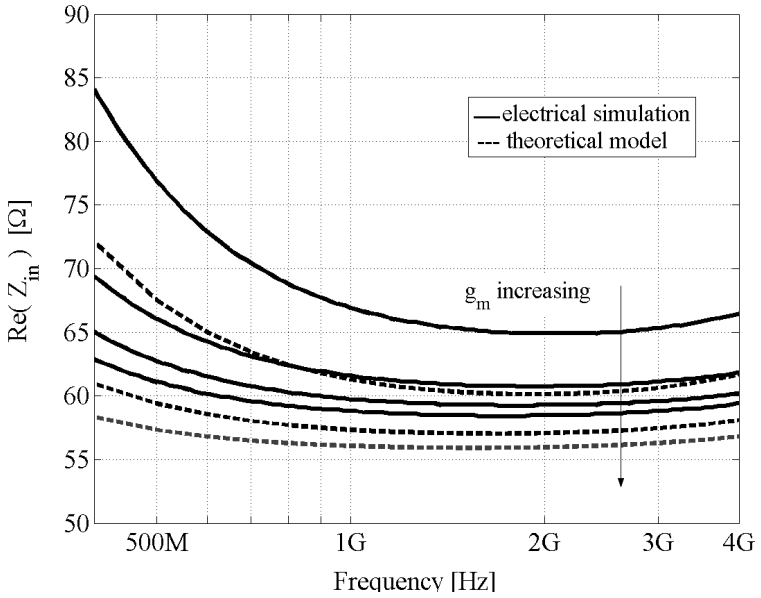

Figure 6.19: Real part of Z_{in}.

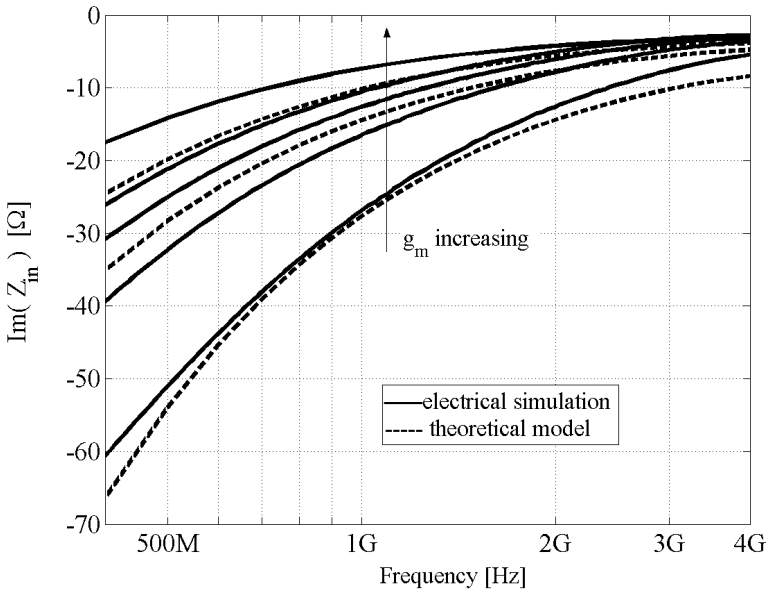

Figure 6.20: Imaginary part of Z_{in}.

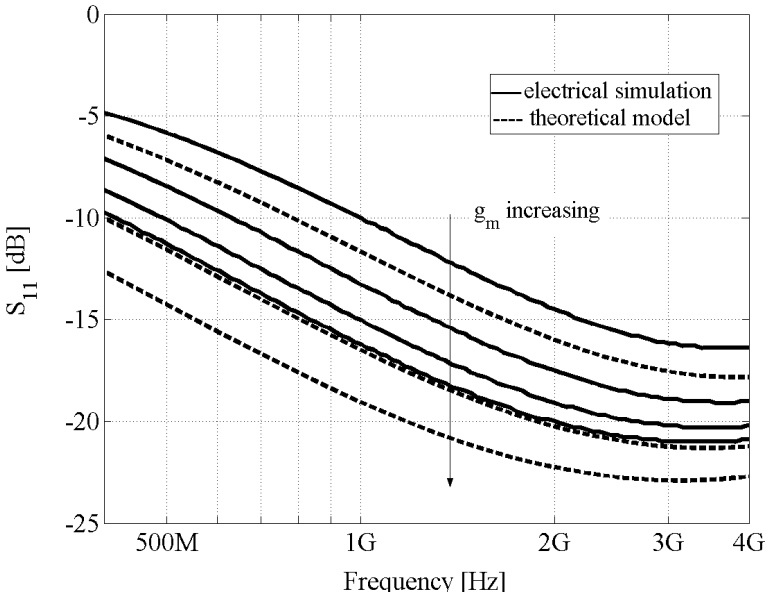

Figure 6.21: S_{11}.

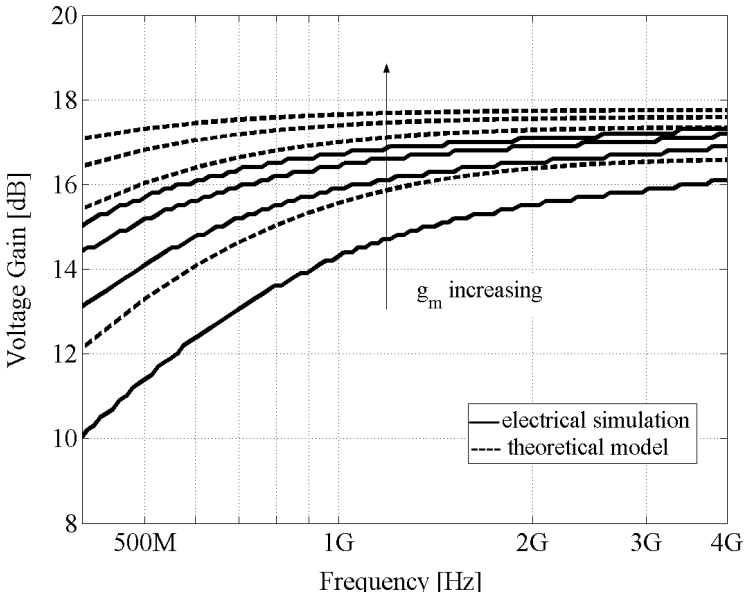

Figure 6.22: voltage gain.

6.6 Noise analysis

The objective of the LNA noise analysis is to determine the total equivalent noise power spectral density referred to the amplifier input [41], and to compare it with the noise power spectral density at the output of the preceding block. Usually the preceding block is an antenna with $R_S = 50\ \Omega$ output impedance, which has a noise power spectral density

$$N_S = 4k_B T R_S \tag{6.41}$$

where k_B is the Boltzmann constant and T is the absolute temperature.

In figure 6.23 the following noise sources are represented:

- $v_{n,A}$: equivalent noise voltage source due to the amplifying block and referred to its input;
- $i_{n,A}$: equivalent noise current source due to the amplifying block and referred to its input;
- $v_{n,R_{w1}}$: noise voltage source of the resistance R_{w1};
- v_{n,R_f}: noise voltage source of the feedback resistance R_f.

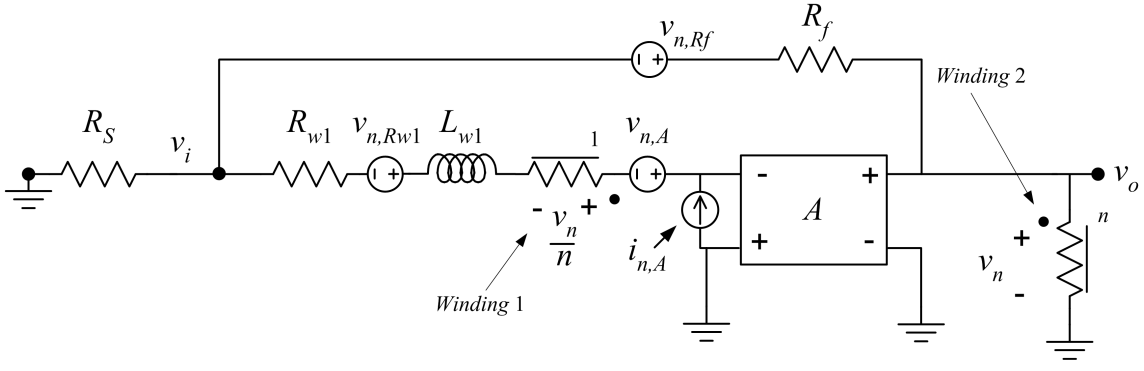

Figure 6.23: DLF LNA noise sources.

In order to simplify the analysis, but keep it reasonably accurate, the following approximations are considered:

1. the noise sources are reported to the amplifying block input, and the amplifying block is a nullor;

2. the noise analysis is performed at a frequency above the pole frequency due to L_{w2} and R_{w2} and below the frequency at which inter-winding capacitances C_{wi} starts to influence significantly the LNA parameters. This means that C_{wi}, L_{w2} and R_{w2} are neglected;

3. all noise sources are uncorrelated.

The amplifying block noise power is mainly due to the input transistor Q_1, it is assumed that Q_2 has little influence on the total input noise power [3]. Three independent noise sources are originated in the input transistor. These noise sources are represented in figure 6.24 and are:

- thermal noise voltage due to the base resistance R_b of transistor Q_1: $v_{n,b}$;
- base shot noise current $i_{n,b}$;
- collector shot noise current $i_{n,c}$.

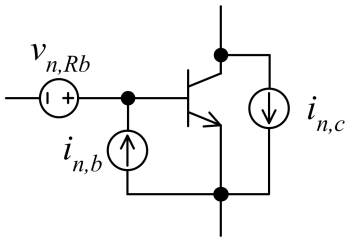

Figure 6.24: BJT noise sources for RF design.

The influence of resistor R_b has been neglected in the input impedance and gain analysis, however concerning noise, this approximation is no longer valid and is now considered. Their power spectral noise densities are respectively [57]:

$$\begin{cases} N_{Rb}(f) = 4k_B T R_b \\ N_{I_B}(f) = 2qI_B \\ N_{I_C}(f) = 2qI_C \end{cases} \tag{6.42}$$

where R_b is the base resistance of transistor Q_1, I_B and I_C are respectively the base and collector DC currents and q is the electron charge. It is possible to determine the equivalent current and voltage noise at the transistor input in accordance with figure 6.25. The noise sources $v_{n,A}$ and $i_{n,A}$ are given by:

$$\begin{cases} v_{n,A} = v_{n,Rb} + \dfrac{1}{g_m}(1 + Z_\pi R_b) i_{n,c} \\ \\ i_{n,A} = i_{n,b} + \dfrac{Y_\pi}{g_m} i_{n,c} \end{cases} \tag{6.43}$$

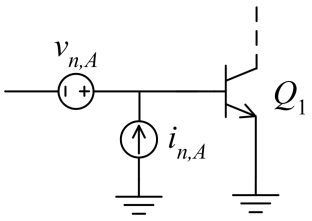

Figure 6.25: Equivalent noise sources at the transistor input.

Y_π is the admittance due to C_π.

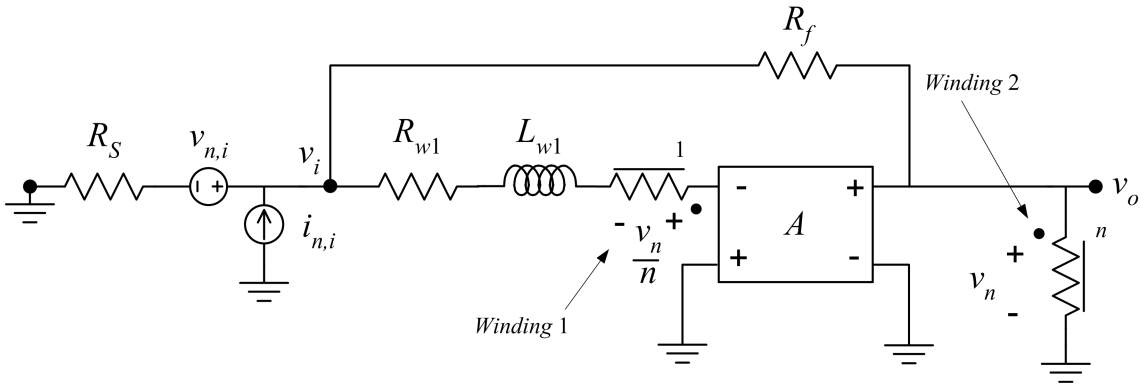

Figure 6.26: Equivalent noise sources at the LNA input.

The equivalent input noise voltage source $v_{n,i}$ and current noise source $i_{n,i}$, represented in figure 6.26, are determined using the source transformations presented in appendix C and are demonstrated in appendix D. The input noise voltage is:

$$v'_{n,i} = v_{n,i} + i_{n,i}R_S = \frac{1}{R_f}(R_f + R_S)(v_{n,A} + v_{n,R_{w1}}) + \\ + \left(\frac{Z_{w1}}{R_f}(R_f + R_S) + R_S\right) i_{n,A} + \frac{R_S}{R_f} v_{n,R_f} \tag{6.44}$$

$Z_{w1} = Z_{Lw1} + R_{w1}$, Z_{Lw1} is the impedance due to L_{w1}. Replacing (6.43) in (6.44) and considering $R_f = R_S(n+1)$:

$$v'_{n,i} \approx \frac{n+2}{n+1}\left(v_{n,Rb} + v_{n,Rw1} + \frac{1}{g_{m1}}(1 + Y_\pi R_b) i_{n,c}\right) + \\ + \left(\frac{n+2}{n+1} Z_{Lw1} + R_S\right)\left(i_{n,b} + \frac{Z_\pi}{g_{m1}} i_{n,c}\right) + \frac{1}{n+1} v_{n,R_f} \tag{6.45}$$

Rearranging (6.45) to put into evidence all noise sources:

$$\begin{aligned} v'_{n,i} \approx & \frac{n+2}{n+1}\left(v_{n,Rb}+v_{n,Rw1}\right)+ \\ & +\left[\frac{n+2}{n+1}\frac{1}{g_{m1}}+\frac{n+2}{n+1}\frac{Z_{Lw1}Z_\pi}{g_{m1}}+\frac{Y_\pi}{g_{m1}}\left(\frac{n+2}{n+1}(R_{w1}+R_{b1})+R_S\right)\right]i_{n,c}+ \\ & +\left(\frac{n+2}{n+1}R_{w1}+R_S+\frac{n+2}{n+1}Z_{Lw1}\right)i_{n,b}+\frac{1}{n+1}v_{n,R_f} \end{aligned} \tag{6.46}$$

Using (6.46) and the Wiener-Khintchine theorem (2.29) the equation of the equivalent input spectral noise density of this DLF LNA is obtained.

$$\begin{aligned} N_i(f) = & \left|\frac{n+2}{n+1}\right|^2\left(N_{Rb}(f)+N_{Rw1}(f)\right)+ \\ & +\left|\frac{n+2}{n+1}\left(\frac{1}{g_{m1}}-\frac{\omega^2 L_{w1}C_\pi}{g_{m1}}\right)+\frac{j\omega C_\pi}{g_{m1}}\left(\frac{n+2}{n+1}(R_{w1}+R_b)+R_S\right)\right|^2 N_{I_C}(f)+ \\ & +\left|\frac{n+2}{n+1}R_{w1}+R_S+\frac{n+2}{n+1}j\omega L_{w1}\right|^2 N_{I_B}(f)+\left|\frac{1}{n+1}\right|^2 N_{Rf}(f) \end{aligned} \tag{6.47}$$

Considering $n \gg 1$, (6.47) can be simplified to:

$$\begin{aligned} N_i(f) = & N_{Rb1}(f)+N_{Rw1}(f)+ \\ & +\left|\frac{1}{g_{m1}}-\frac{\omega^2 L_{w1}C_\pi}{g_{m1}}+\frac{j\omega C_\pi}{g_{m1}}\left(R_{w1}+R_{b1}+R_S\right)\right|^2 N_{I_C}(f)+ \\ & +\left|R_{w1}+R_S+j\omega L_{w1}\right|^2 N_{I_B}(f)+\left|\frac{1}{n+1}\right|^2 N_{Rf}(f) \end{aligned} \tag{6.48}$$

The noise factor is

$$F(f) = 1+\frac{N_i(f)}{N_S(f)} \tag{6.49}$$

It is possible to determine a noise figure value independent on frequency considering only the terms of (6.48) that are independent on frequency:

$$F = 1+\frac{R_{b1}+R_{w1}}{R_S}+\varphi\frac{I_C}{R_S g_{m1}^2}+\varphi\frac{(R_{w1}+R_S)^2}{R_S}I_B+\frac{1}{n+1} \tag{6.50}$$

where $\varphi = (2q)/(4k_BT) \approx 19.34\ \mathrm{V}^{-1}$. In (6.50) the importance of minimizing R_{b1} and R_{w1} is visible. Assuming that $g_{m1} \gg 10/R_S$ and $R_S \gg R_{w1}$, and by taking into

account that $I_C = g_m/V_T$ and $I_B = I_C/\beta$, (6.50) becomes:

$$F = 1 + \frac{R_{b1} + R_{w1}}{R_S} + \varphi\left(\frac{1}{10} + \frac{10}{\beta}\right) V_T + \frac{1}{n+1} \approx$$
$$\approx 1 + \frac{R_{b1} + R_{w1}}{R_S} + 0.5\left(\frac{1}{10} + \frac{10}{\beta}\right) + \frac{1}{n+1} \tag{6.51}$$

This result leads to several important guidelines for the DLF LNA design concerning noise:

- R_{w1} and R_b should be minimized;
- the amplifying block transconductance g_{m1} should be maximized;
- the transformer voltage ratio n should be maximized.

These guidelines are in accordance with the guidelines concerning the input impedance and voltage gain. Figure 6.27, obtained in the same conditions of figures 6.19 to 6.22, shows the noise figure obtained by (6.47) and by simulation. At low frequencies, as the transconductance increases, the noise figure tends to a constant value.

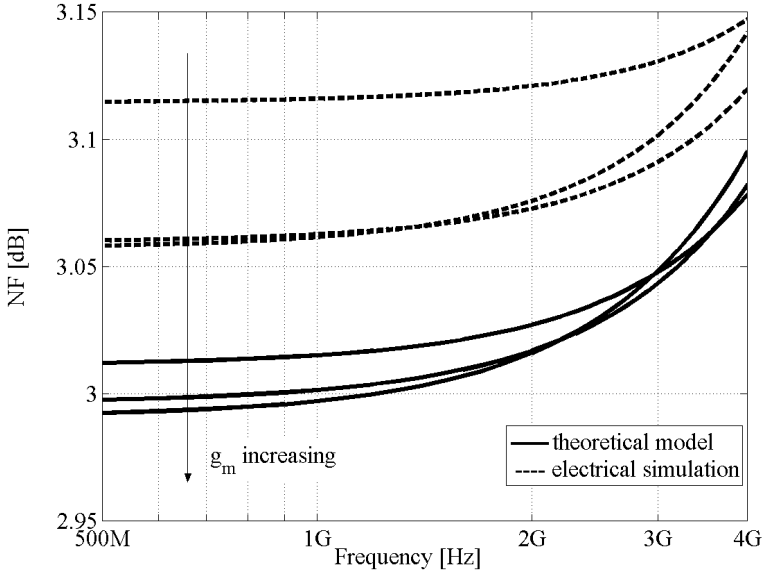

Figure 6.27: Noise figure.

6.7 Conclusions

When considering ideal blocks (ideal transformer and a nullor), the DLF LNA studied in this chapter has frequency independent and constant input impedance, voltage gain and noise figure. This indicates that this LNA is potentially wideband.

When a non-ideal transformer is considered, but the amplifying block is considered ideal, the DLF LNA has frequency dependent parameters. With proper design it is possible to obtain a frequency band where there is input impedance matching, with reasonable gain and low noise figure.

The amplifying block is designed so that it can be considered as ideal. It is shown that by using a single stage amplifying block (cascode stage preferably), it is possible to achieve the desired LNA performance.

Equations were determined for the input impedance, voltage gain and equivalent input spectral noise density of the DLF LNA. The amplifying block transconductance has a minimum value that allows the amplifying block to be considered as an ideal amplifier. The upper limit of the transconductance is set by the power consumption. These two limits indicate whether it is possible to implement the DLF LNA in a given technology with a reasonable power consumption.

The simulation of a complete LNA, considering non-ideal transformer, and an amplifying block designed using transistors, confirms that it is possible to split the LNA design into two distinct tasks: design of the feedback network and design of the amplifying block.

Chapter 7

LNA Prototype Design and Experimental Results

7.1 Introduction

This chapter is dedicated to the design of a prototype of the double loop feedback low noise amplifier (DLF LNA) studied in chapter 6 and to the presentation of experimental evaluation of a test chip. The DLF LNA was designed using the AMS SiGe BiCMOS 0.35 μm technology.

In section 7.2, the DLF LNA design is described from the specifications to the complete circuit layout. In section 7.3, the transformer layout is described, and some considerations about the complete LNA circuit layout are discussed. In section 7.4 the test board design and the chip bonding are described, and in section 7.5 experimental results are presented, and some improvement suggestions are proposed. Finally, in section 7.6, some conclusions are drawn.

7.2 DLF LNA Design

The DLF LNA circuit to be prototyped is represented in figure 7.1.

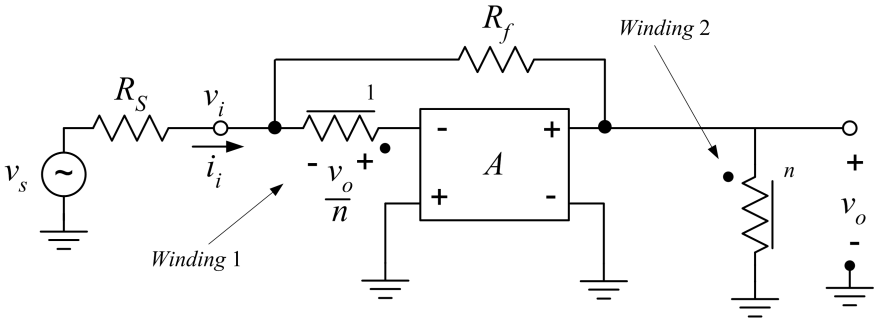

Figure 7.1: DLF LNA to be designed.

The LNA is to be tested using equipment with standard 50 Ω port impedances; thus, the LNA input and output must be connected to 50 Ω. The LNA is designed to have input impedance 50 Ω, but the output impedance is different from 50 Ω; thus, it is necessary to use a buffer with 50 Ω output. In figure 7.2 the different blocks that have to be sized are presented.

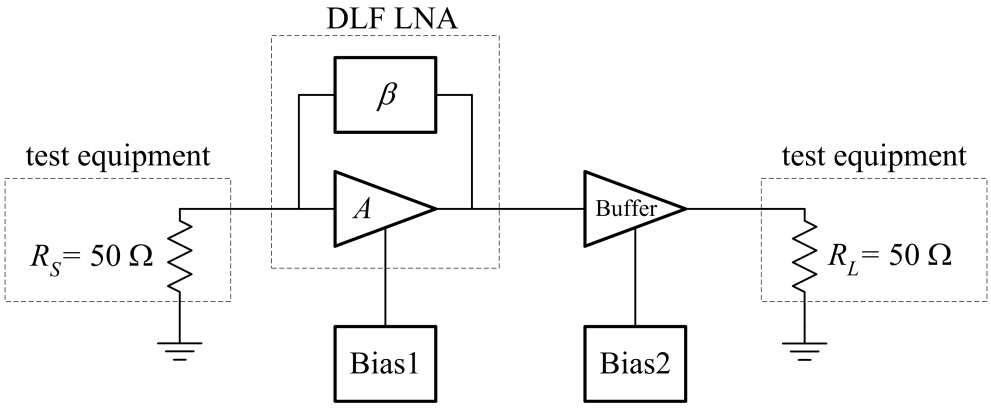

Figure 7.2: Block diagram of the prototype (A is the amplifying block and β is the feedback network).

The design is divided into three parts:

1. feedback network;
2. amplifying block and its biasing;
3. buffer and its biasing.

The feedback network is dimensioned firstly considering an ideal amplifying block. Then, the amplifying block (and its biasing circuit) is designed in order to be a good approximation to an ideal amplifying block. Since the DLF LNA has an output impedance different from the standard 50 Ω, a buffer is required with 50 Ω output impedance. The circuit is designed with the guidelines listed in table 7.1.

Table 7.1: LNA guidelines.

Technology	AMS 0.35 μm
Voltage Supply	3 V
S_{11}	$\lesssim -10$ dB
Voltage Gain	around 10 dB
Noise Figure	around 3 dB
Frequency Bandwidth	around 1 GHz

7.2.1 The Feedback Network Design

The DLF LNA performance, considering ideal blocks, depends only on the feedback network, and the input impedance, voltage gain, and noise factor are:

$$Z_{in} = \frac{R_f}{n+1}$$

$$A_v = \frac{v_o}{v_i} = -n \tag{7.1}$$

$$F = 1 + \frac{1}{n+1}$$

n should be maximized in order to improve the voltage gain, and then R_f is determined using the input matching condition $Z_{in} = R_S = 50\ \Omega$.

From

$$n = \frac{1}{k}\sqrt{\frac{L_{22}}{L_{11}}} \tag{7.2}$$

to maximize n, L_{22} should be maximized, while L_{11} and k should be minimized. The value of n is limited, since a large L_{22} leads to a large series resistance and a large area, and a small L_{11} is not feasible reliably in integrated circuits.

Considering the complete transformer windings model, including its most common

parasitics (figure 2.19), the design guidelines for the transformer are: r_{22} should be minimized to reduce the lower bound of the frequency band and r_{11} should be minimized to reduce the noise figure. C_{w1} and C_{w2} should be low, to increase the upper bound of the frequency band. The transformer layout is described in subsection 7.3.1 and its model element values are listed in table 7.2.

Table 7.2: Transformer parameters.

Parameter	Value
L_{11}	0.98 nH
$L_{w1} = L_{11}(1 - k^2)$	0.64 nH
$L_{w2} = L_{22}$	22.65 nH
r_{w1}	9.8 Ω
r_{w2}	20.5 Ω
C_{w1}	60 fF
k	0.59
n	8.15

Using the values listed in table 7.2 and equation (7.1), the feedback resistance R_f should be 457.5 Ω.

7.2.2 Amplifying Block Design

The amplifying block design follows the guidelines established in chapter 6. Some major decisions concerning the amplifying block design are:

- transistor type;
- number of stages;
- stage topology.

The SiGe BiCMOS AMS 0.35 μm technology provides both MOS and bipolar transistors. Due to the need of a high transconductance, bipolar transistors are chosen.

Using more than one stage leads to some problems concerning biasing, coupling between stages (coupling capacitors are not ideal), and stability. Thus, the amplifying block is designed using a single stage.

In chapter 6 it is concluded that a cascode configuration should be used. In figure 7.3 the amplifying block implemented with transistors is presented together with the feedback network. Winding 2 is connected to the supply voltage to bias the transistors. The LNA is designed in order to minimize components size, mainly the coupling capacitors size that increase significantly the die area[1].

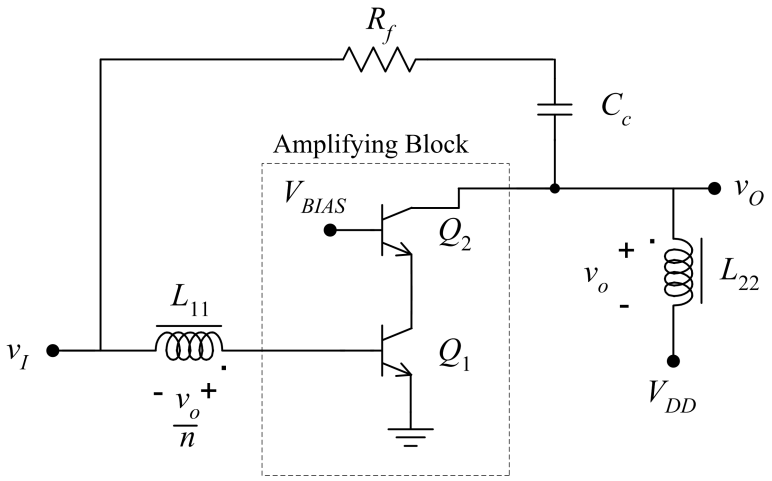

Figure 7.3: DLF LNA (biasing of Q_1 not shown).

In chapter 6 is was found that the amplifying block transconductance G_m should be much higher than the input admittance:

$$G_m \gg \frac{1}{R_S} \tag{7.3}$$

Choosing $G_m = 10R_S^{-1}$, with $R_S = 50\ \Omega$, the minimum value of G_m is 0.2 S. In the cascode stage G_m is equal to the transconductance g_m of transistor Q_1. In a bipolar,

$$g_m = \frac{I_C}{V_T} \tag{7.4}$$

Considering V_T approximately equal to 25 mV, the minimum DC current to achieve a transconductance of 0.2 S is approximately 5 mA. This value is reasonable in comparison with those used in other LNA architectures.

In figure 7.4 the amplifying block biasing circuit is represented. Transistor Q_{B1} has the same size of transistor Q_1. R_{B2} and C_B form a low-pass filter that prevents the input high frequency signal v_i from being injected into the biasing circuit. Q_{B2},

[1]The area is dominated by inductors, but good coupling capacitors have also large area.

R_{B1} and R_{B2} ensure that I_{Bias} is approximately equal to $I_{C,Q1}$ [89, 124]. Transistor Q_{B3} is used to ensure that the cascode transistor Q_2 never leaves the saturation region.

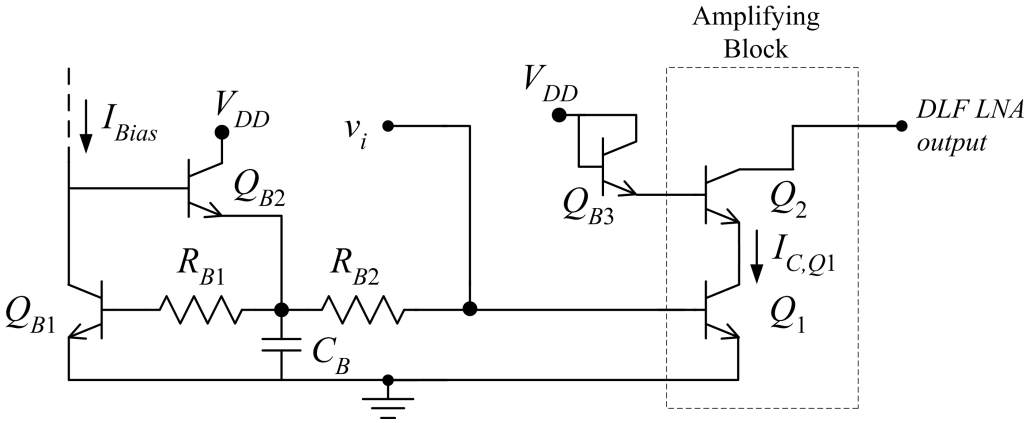

Figure 7.4: Amplifying block biasing.

7.2.3 Buffer Design

The DLF LNA has an output impedance that is not equal to 50 Ω. To connect the LNA output to the test equipment a buffer is used, that provides 50 Ω output impedance and has a high input impedance. An emitter-follower is used. It has a high input impedance and the output impedance is approximately g_m^{-1}, which can be made equal to 50 Ω. In figure 7.5 the LNA buffer is represented together with the biasing circuit. The biasing circuit is formed by Q_{B4}, Q_{B5}, R_{B3}, R_{B4}, C_{B1} , and is similar to the LNA biasing circuit discussed in the last subsection.

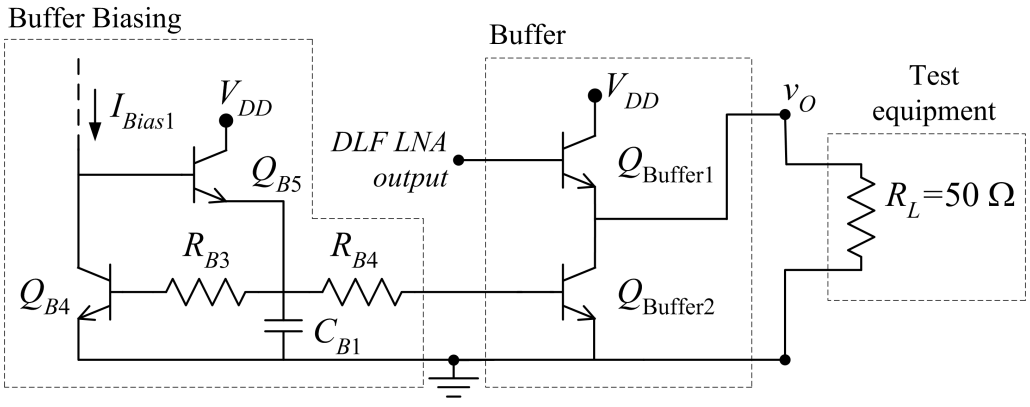

Figure 7.5: Buffer with biasing circuit.

7.2.4 Simulation Results

In figure 7.6 the complete DLF LNA circuit is represented, including the biasing circuit. Note that by using the external coupling capacitor there is no DC current through winding 1. There is no DC current through R_f, due to C_c.

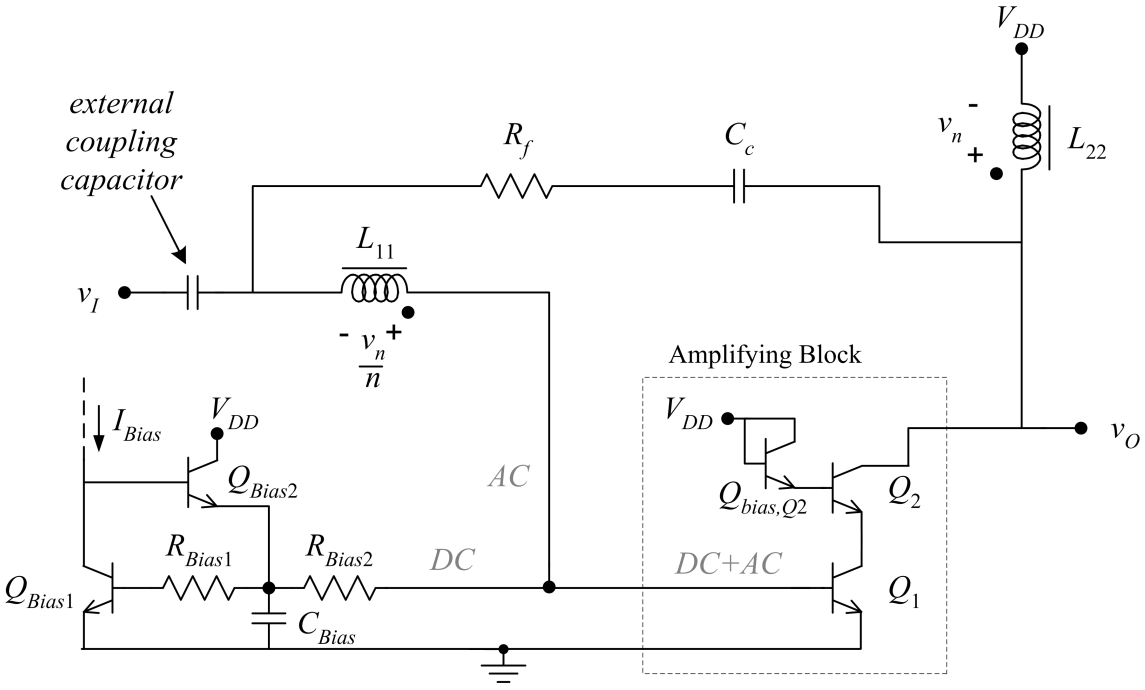

Figure 7.6: Complete DLF LNA circuit.

In figures 7.7 to 7.9 are represented, respectively, S_{11}, the voltage gain, and the noise figure, for different values of the bias current. The values used in the simulations are listed in table 7.3.

Typically, the input impedance matching is considered good when S_{11} is below -10 dB. Using this criterion, for all bias values the bandwidth of almost one decade is obtained. When the bias current increases, the first frequency at which S_{11} is -10 dB decreases, which is in accordance with the results obtained in chapter 6; however, there is not a clear rule for the higher frequency where S_{11} equals -10 dB.

In figure 7.8 the voltage gain is represented for the same bias current values. At low frequencies, g_{m1} is not dominant over $|n/(\omega L_{22})|$ (condition 3 of figure 6.15); thus the gain is low. However, when g_{m1} increases, the voltage gain tends to a constant value. The bandwidth where the voltage gain is almost constant increases as g_{m1} increases, meaning that g_{m1} satisfies all the three conditions of figure 6.15 when the

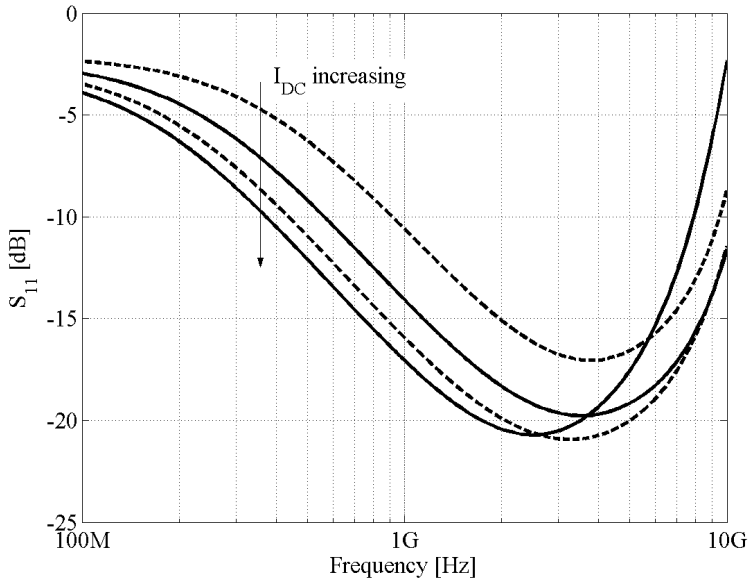

Figure 7.7: S_{11} with DC current values: 2.5, 5.0, 7.5, and 10.0 mA.

bias current increases.

Figure 7.9 displays the noise figure for the same bias conditions. The noise figure has a flat zone in a wide band; however the value decreases when the transconductance increases, reaching a value of approximately 2.4 dB for the two higher current values. This means that for high values of bias current the amplifying block behaves as an ideal block (high gain and low sensitivity to bias current variations).

Figures 7.10 to 7.12 represent S_{11}, voltage gain, and noise figure for the same bias conditions of figures 7.7 to 7.9, but considering the transformer resistances and inter-winding capacitances.

In figure 7.10, the input impedance matching is slightly degraded in comparison with figure 7.7, and this happens for all current values. Another difference is the decrease of the bandwidth. This is due to the resonance of L_{11} with the inter-winding capacitances, as demonstrated in chapter 6.

In figure 7.11, the voltage gain behavior is similar as in figure 7.8 at low frequencies; however, at high frequencies, there is again a resonance, due to L_{11} and the inter-winding capacitance.

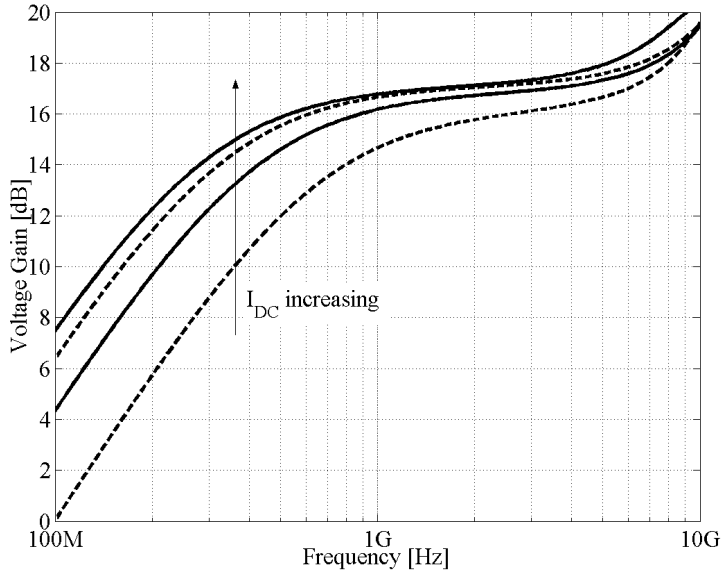

Figure 7.8: Voltage gain with DC current values: 2.5, 5.0, 7.5, and 10.0 mA.

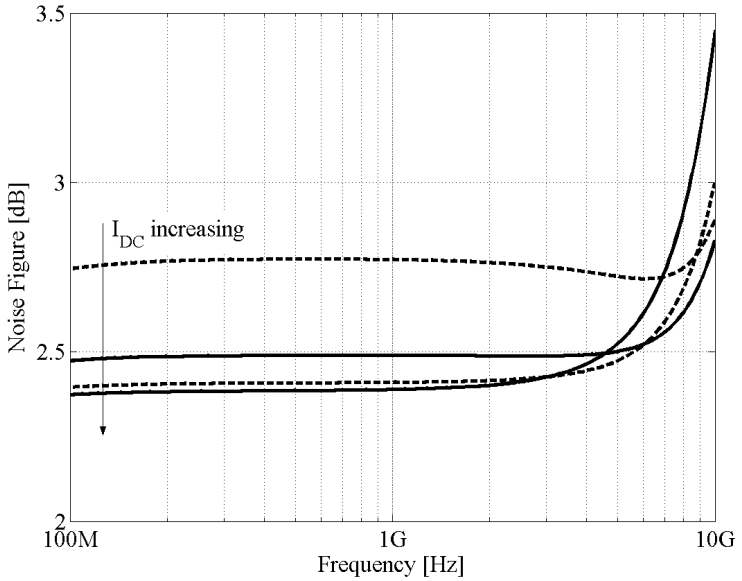

Figure 7.9: Noise figure with DC current values: 2.5, 5.0, 7.5, and 10.0 mA.

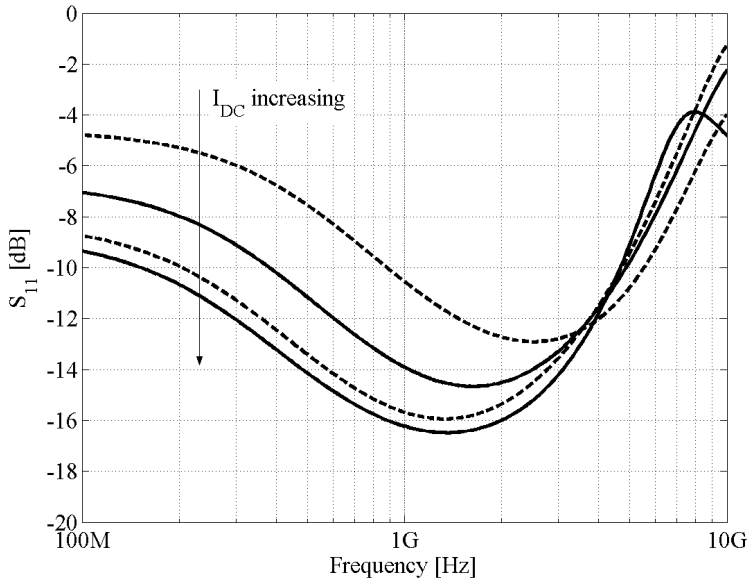

Figure 7.10: S_{11} considering resistances and inter-winding capacitances, with DC current values: 2.5, 5.0, 7.5, and 10.0 mA.

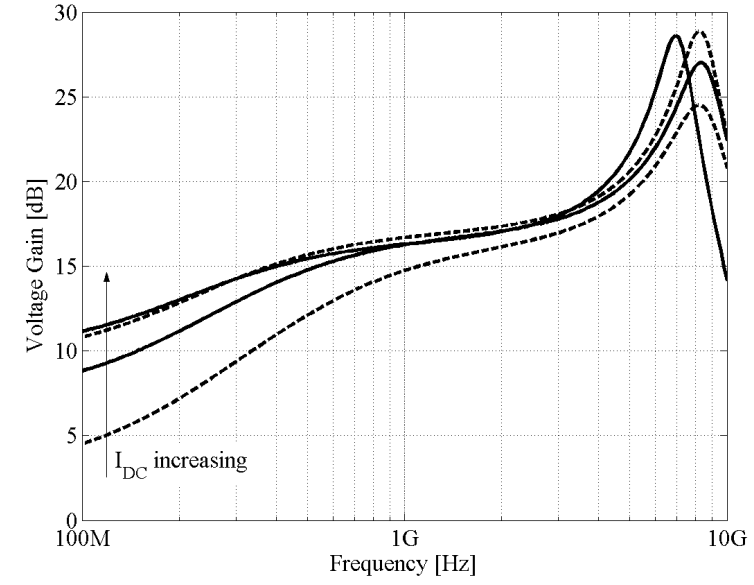

Figure 7.11: Voltage gain considering resistances and inter-winding capacitances, with DC current values: 2.5, 5.0, 7.5, and 10.0 mA.

The noise figure in figure 7.12 has the same behavior as in figure 7.9; however, all curves are approximately 0.6 dB higher within the wanted band. This difference is due to the series resistance of winding 1, and is approximately $10\log(1 + r_{11}/R_S)$, obtained from equation (6.13).

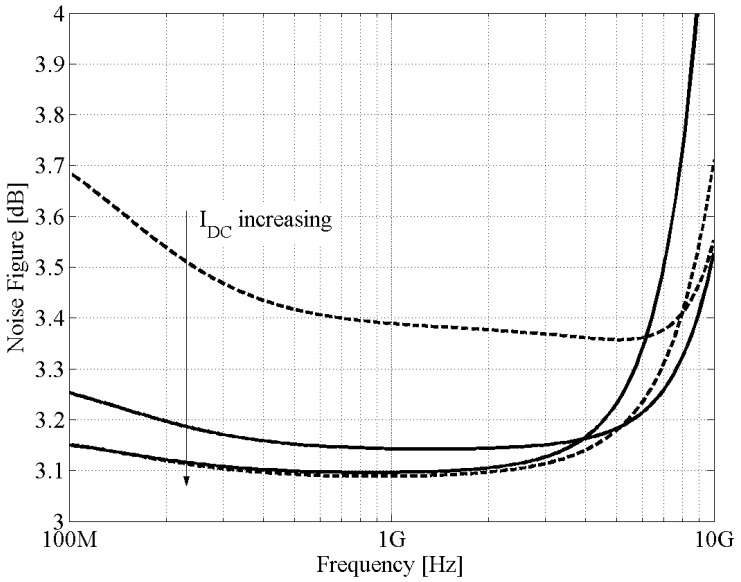

Figure 7.12: Noise figure considering resistances and inter-winding capacitances, with DC current values: 2.5, 5.0, 7.5, and 10.0 mA.

7.3 DLF LNA Layout

In this section, the transformer layout is described, and general considerations concerning the DLF LNA layout are presented.

7.3.1 Transformer layout

Concerning the transformer implementation, since the substrate is highly resistive, there is no need for a patterned ground shield which is used in low resistivity substrates. However, when the transformer was designed, this was unknown to the author, and the patterned ground shield represented in figure 7.13 was implemented (the design strategy used is explained in chapter 2).

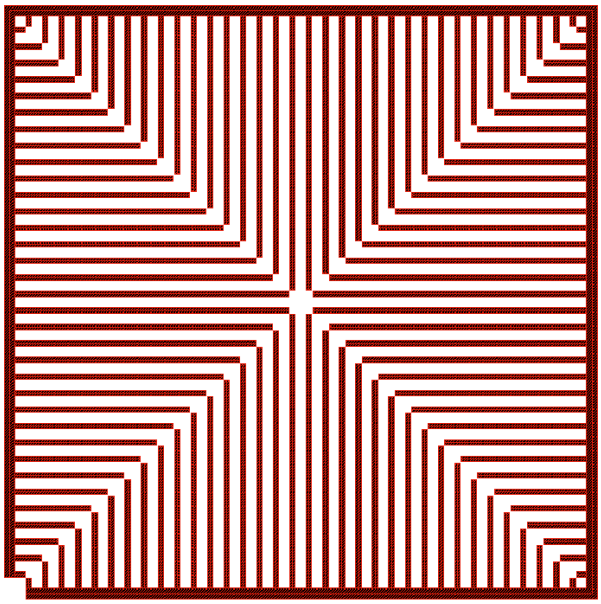

Figure 7.13: Patterned Ground Shield.

Concerning the design of the windings, several aspects should be taken into account. Area should be a concern, but the need for a large inductance L_{22} with a reduced series resistance leads to a large winding, due to the large line width required to minimize the series resistance. In [62] a table is presented with an extensive list of inductor values and corresponding dimensions; to obtain a large inductance, around 20 nH, an outer diameter above 200 μm and a large number of turns, around 10 are required. Also, in order to minimize the inductor series resistance, the top metal layer 4 is used, due to its larger thickness. The technology has the option of having a thicker layer for the top metal: layers 1, 2 and 3 have a typical thickness of 0.640 μm, while the top layer 4 has an average thickness of 0.925 μm. This option reduces the series resistance due to the lower metal resistivity and simultaneously reduces the substrate capacitance due to the higher distance to ground of this layer.

From the possible transformer topologies, the stacked transformer was chosen because it has a high magnetic coupling, it is suitable for asymmetric inductors, and its inter-winding capacitance can be minimized. Inductance L_{11} should be minimum. Metal layers 2 and 3 are used, and the inductance is placed below the other winding. This inductor has one turn. The two metal layers are short-circuited to reduce the winding series resistance [59, 60, 125]. The transformer layout is presented in figure 7.14. Winding 1 is between two turns of winding 2. This was done to reduce the inter-winding capacitance, that would be much higher if the turns of both winding were superimposed.

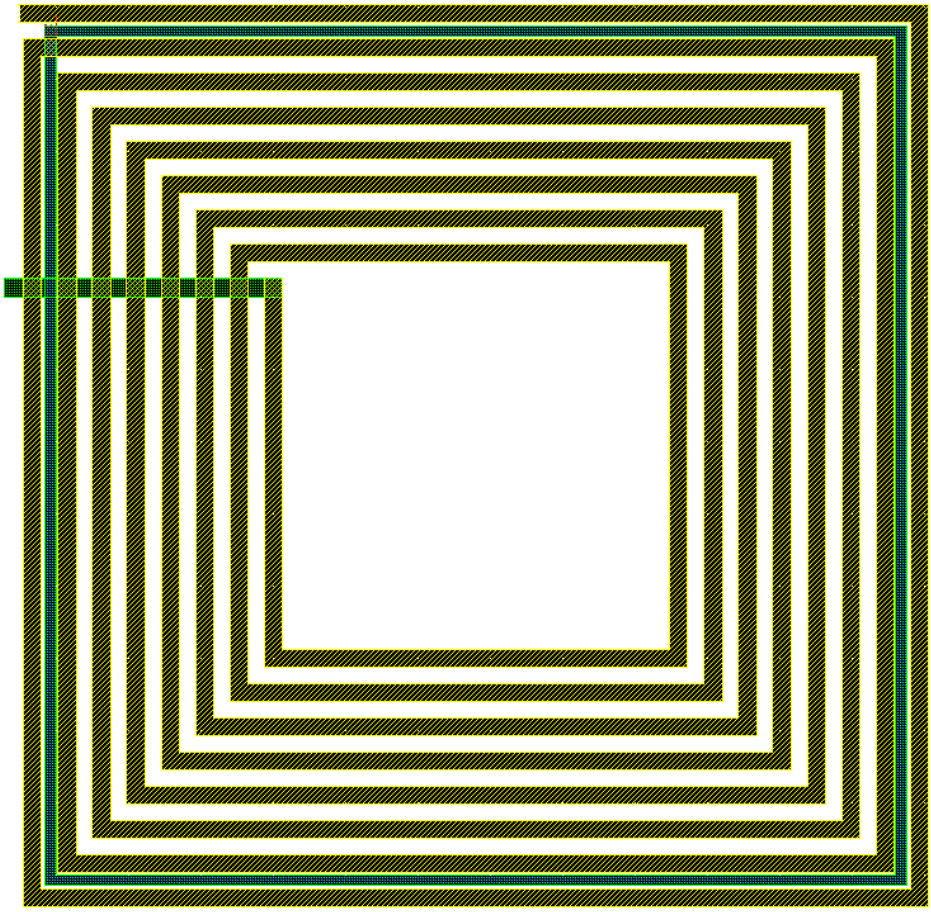

Figure 7.14: Transformer layout.

Simulations using the program ASITIC produced the output in figure 7.15 and in table 7.3.

Table 7.3: Main transformer parameters.

Parameter		Winding 1	Winding 2
External diameter	d_{out}	238 μm	250 μm
Spacing between turns	s	N/A	4.5 μm
Turn width	w	3.0 μm	5.0 μm
Winding inductance	L_{ii}	0.83 nH	22.65 nH
Series resistance	r_{ii}	9.8 Ω	20.5 Ω
Inductor magnetic coupling	k	0.63	
Inter-winding capacitance	C_{12}	134 fF	
	C_{wi}	$C_{12}/2 = 67$ fF	
Voltage ratio	n	8.29	

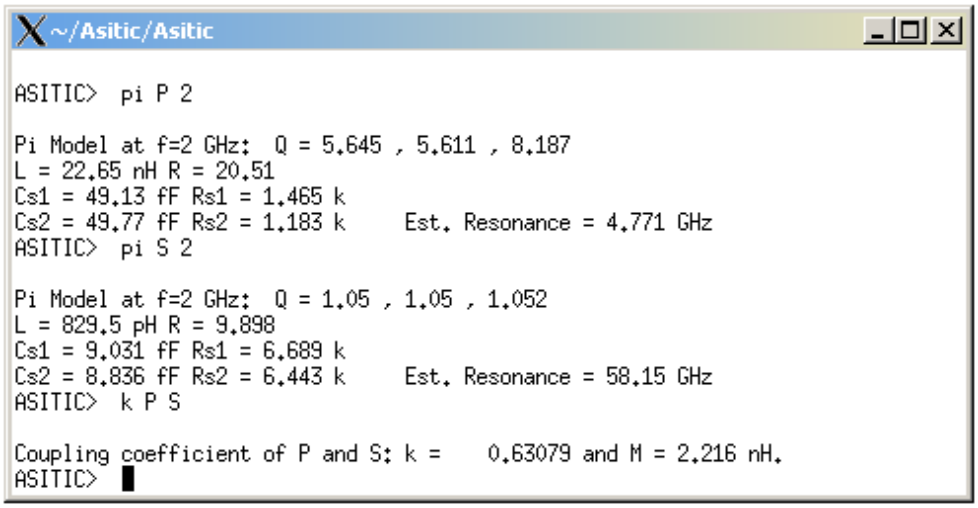

Figure 7.15: ASITIC results for the transformer.

7.3.2 General Layout Considerations

The final step of the LNA prototype design consists of the circuit layout. The layout of RF circuits is critical, and should respect some important rules that improve its reliability. Some of these rules are listed below:

- The ground lines should be distributed along the circuit, and connections to ground should be the shortest possible. The distributed ground improves the current flow. Several ground pads should be used to improve current distribution through the circuit.
- All lines should be designed to support a current higher than expected.
- The use of long connecting lines should be avoided, and current paths inside the layout should be designed to minimize parasitic inductances and unwanted parasitic magnetic fields.
- A safety distance between transformer and other devices should be used to reduce magnetic coupling between devices.
- A ground shield must be used below the transformer to prevent eddy currents in the substrate, if the substrate has a low resistivity.
- All devices should have a guard ring to improve the substrate biasing and reduce noise.

The DLF LNA layout is designed to allow both on wafer and board testing. Next, some specific layout aspects of this particular LNA are listed:

- The input and output pads are designed with minimum area and using only metal layer 3 and the thick top metal layer 4, to minimize parasitic capacitances. The estimated value of the input pads capacitance to ground is 150 fF,
- to allow on wafer testing, the input and output pads should have a minimum distance to other pads of at least 200 μm; thus, the layout is not optimized in terms of area.

The final DLF LNA layout is presented in figure 7.16, and has an area of 740 μm $\times$ 890 μm = 0.659 mm^2.

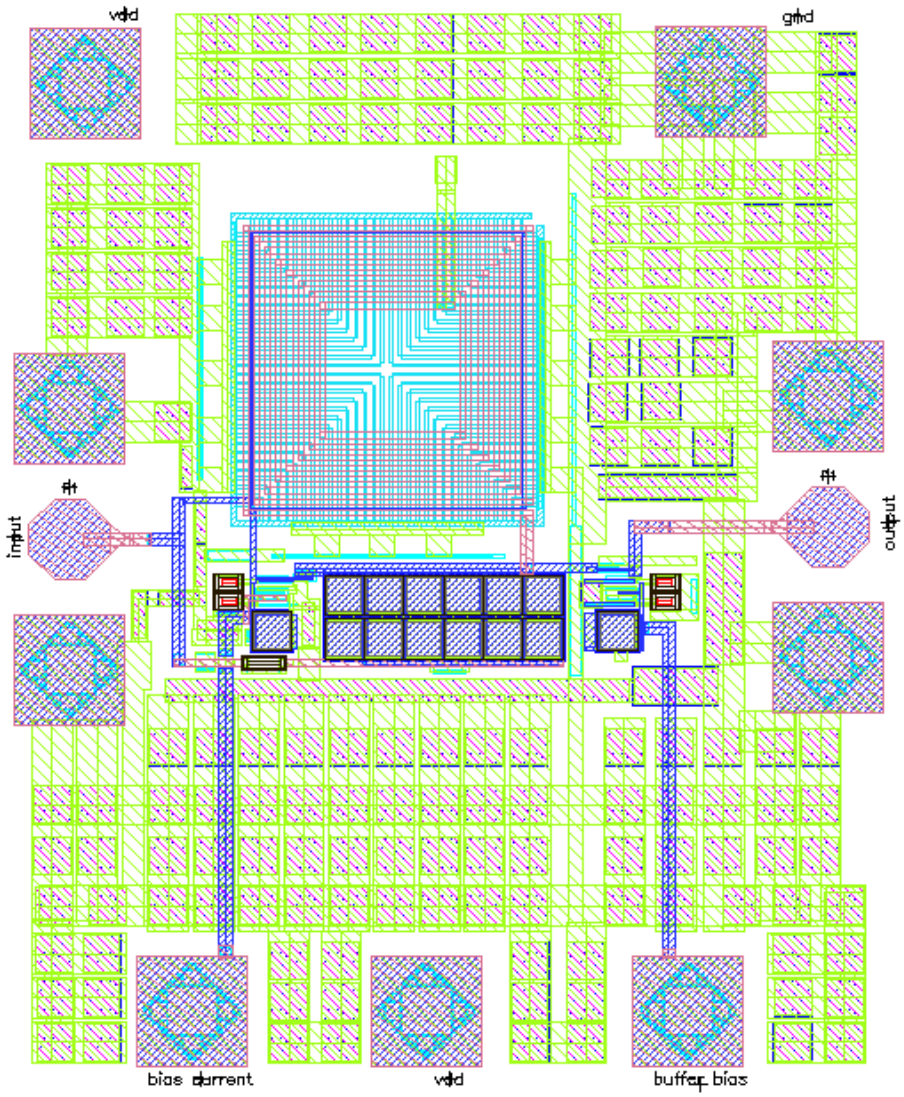

Figure 7.16: Complete DLF LNA and buffer layout.

7.3.3 Post-Layout Simulations

In figures 7.17 to 7.20 the S-parameters of the DLF LNA plus buffer are represented. The DLF LNA is biased with 10 mA and the buffer with 0.5 mA. Two simulation results are plotted: original circuit simulation and post-layout simulation.

It is visible that the post-layout simulation of S_{11} is higher than the original simulation in the higher frequency region, due to layout parasitic capacitances. The remaining S-parameters are approximately unaltered by the layout parasitics.

In figure 7.21 the noise figure is represented. The simulated noise figure presented in figure 7.21 is slightly higher than in figure 7.9 where only the DLF LNA is considered. This means that the noise generated by the buffer is not negligible. Comparing the pre with the post-layout results, there is an increase in the noise figure and the frequency behavior is also altered, due to parasitic capacitances and resistances resulting from the layout.

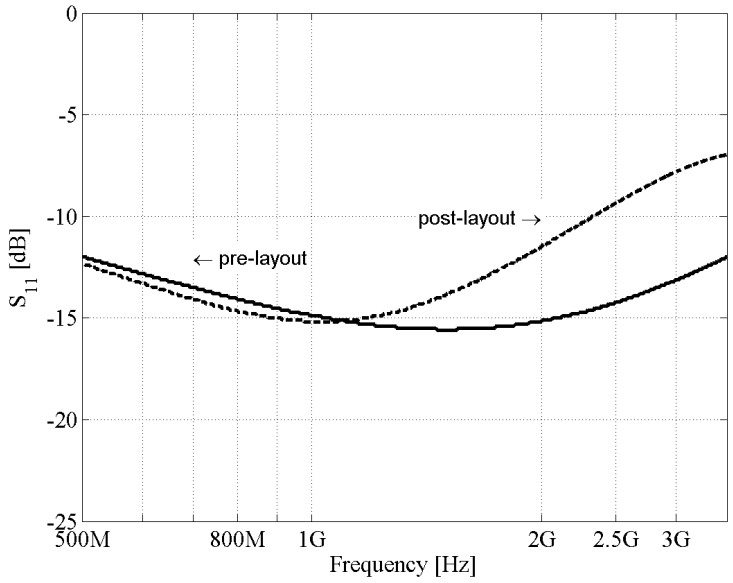

Figure 7.17: S_{11} of the complete circuit (LNA and buffer): pre and post-layout simulations.

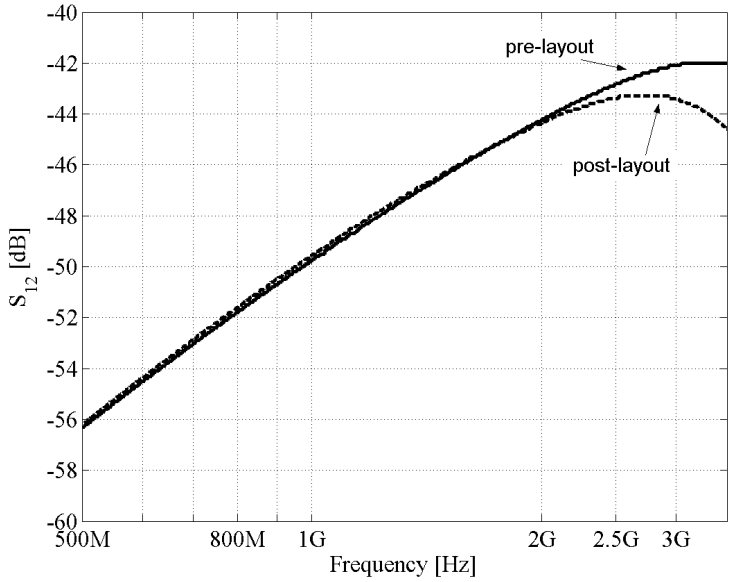

Figure 7.18: S_{12} of the complete circuit (LNA and buffer): pre and post-layout simulations.

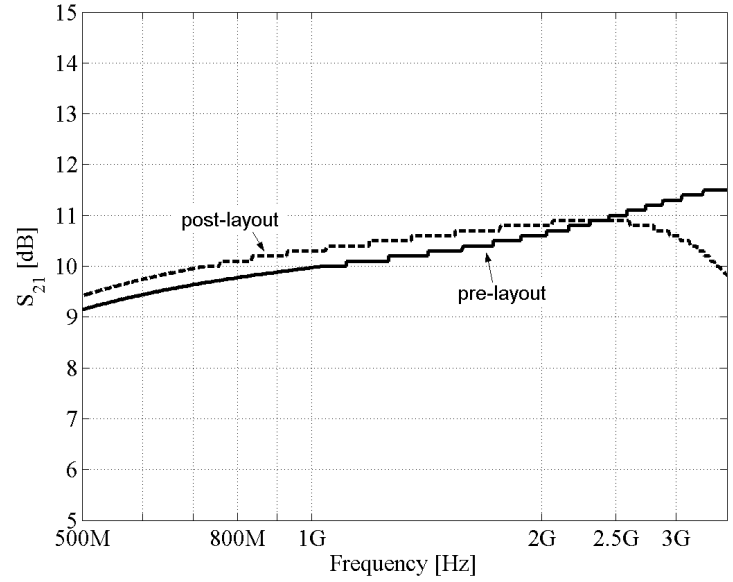

Figure 7.19: S_{21} of the complete circuit (LNA and buffer): pre and post-layout simulations.

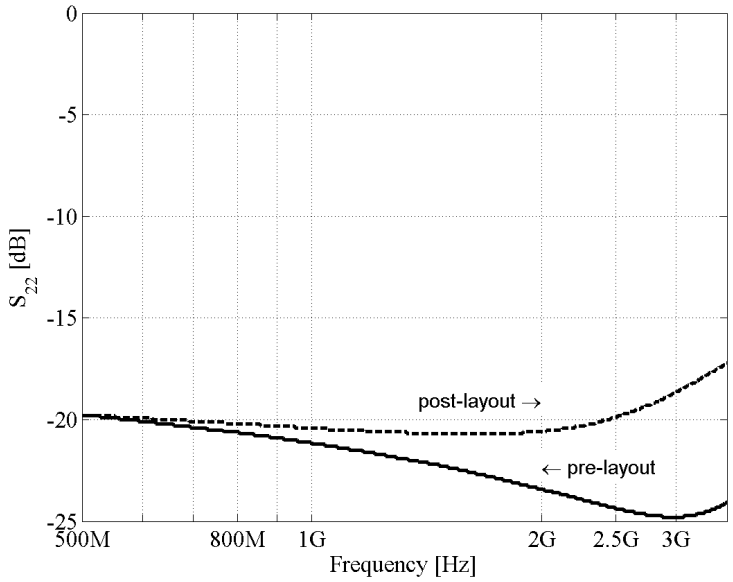

Figure 7.20: S_{22} of the complete circuit (DLF LNA and buffer): pre and post-layout simulations.

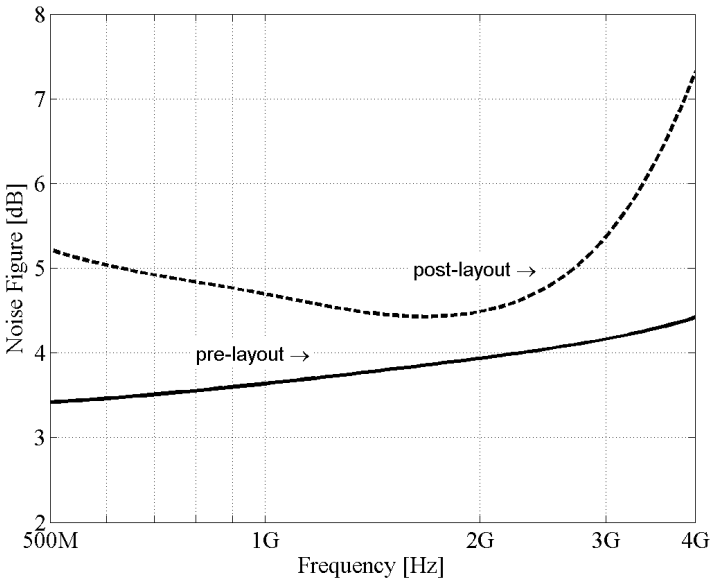

Figure 7.21: Noise figure of the complete circuit (DLF LNA and buffer): pre and post-layout simulations.

7.4 Test Board Design and Wire Bonding

To perform the DLF LNA test, a printed circuit board of FR-4[2] (PCB) laminate with a thickness of 0.8 mm was used with two metal (copper) layers. The input and output lines should have 50 Ω characteristic impedance, which leads to a width of 1.27 mm for these lines [127]. In figure 7.22 the board layout is represented in natural size.

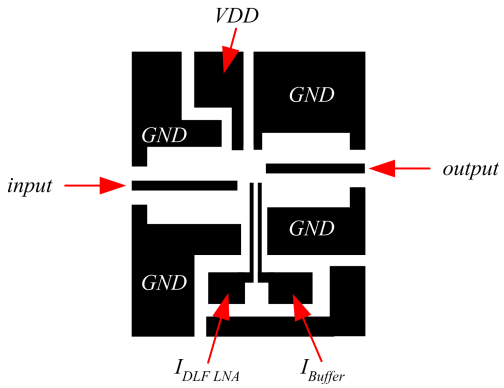

Figure 7.22: Board 1 layout - natural size.

In figure 7.23 the circuit with its access points (pads) is represented, and in figure 7.24 the DLF LNA circuit is represented connected to the test setup and voltage supply. Variable resistances are used to obtain the reference currents for biasing. R_{DLF} controls the current in the DLF LNA and R_{BUFFER} controls the current in the buffer. All bonding wire inductances are represented.

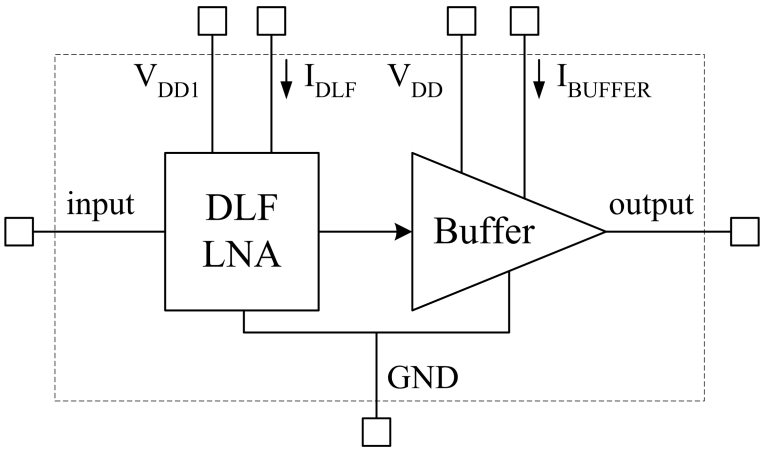

Figure 7.23: Test circuit with pads.

[2]The "FR" means Flame Retardant (to UL94V-0), and Type "4" indicates woven glass reinforced epoxy resin [126].

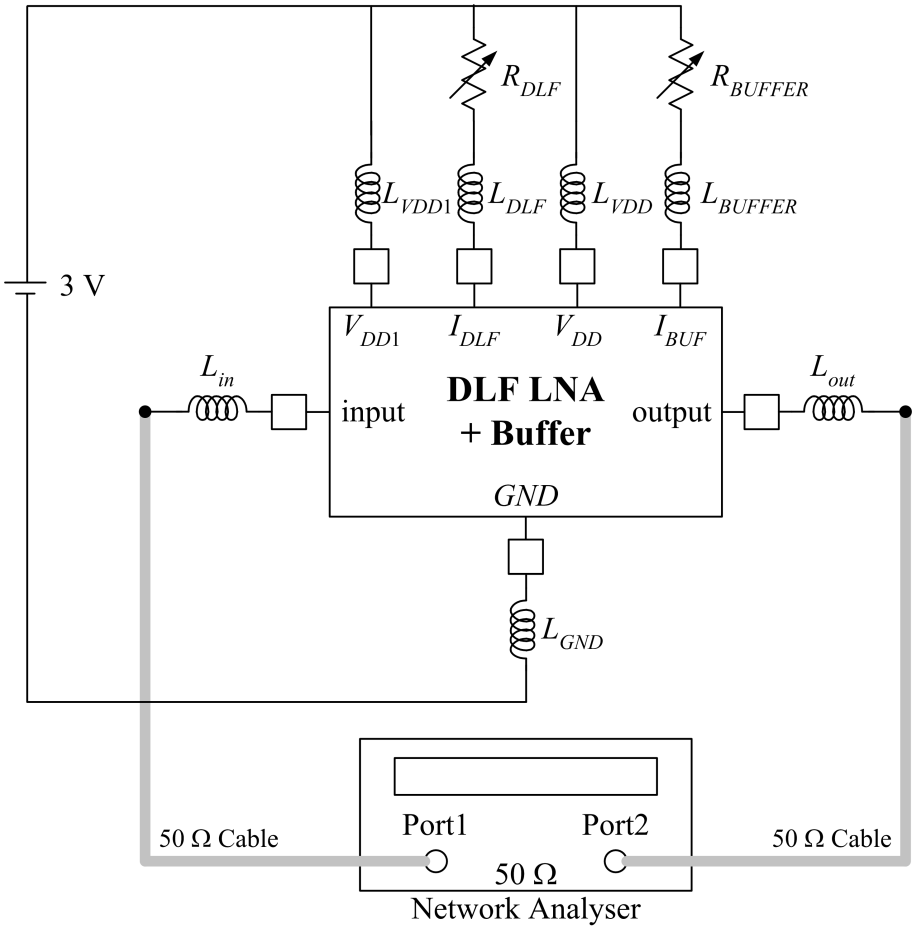

Figure 7.24: Test setup.

The two variable resistors in the schematic of figure 7.24 are adjusted to the following values:

- $R_{\mathrm{DLF}} = 70\ \Omega$
- $R_{\mathrm{BUFFER}} = 3500\ \Omega$

which produce biasing currents of approximately 10 mA in the DLF LNA and 0.5 mA in the buffer.

The connection of the circuit die to the board is done by bonding wires, which have series inductance and resistance with values given in [128]. A gold bond wire was used with approximately 18 μm diameter (approximately 0.8 mil). Figure 7.25 shows the photo of the test board. In table 7.4 the list of laboratory equipment used is presented.

Table 7.4: List of laboratory equipment.

Material:
WILTRON Vector Network Analyzer (NA), model 360B
HP Noise Figure Meter, model 8970B
HP Noise Source, model 346A
10 dB attenuator
DC blocking coupler

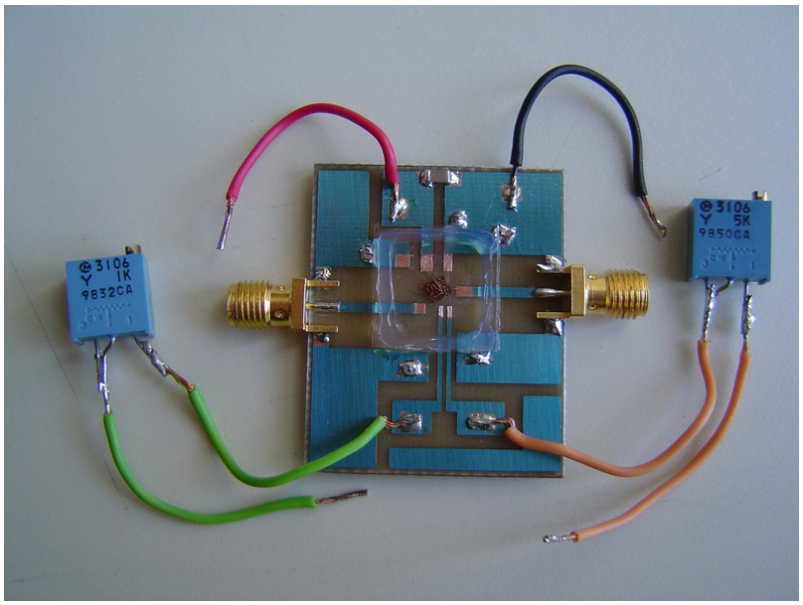

Figure 7.25: Test board with die.

In [129] the calibration process of the Vector Network Analyzer and the test procedure used are presented.

7.5 Experimental Results

In this section, the main experimental results are presented and discussed. First, the transformer experimental results are presented, and then, the LNA experimental results are given.

7.5.1 Transformer

An isolated transformer was included in the test chip and was tested individually by AMS. In figures 7.26 to 7.29 the (de-embedded) experimental and simulated S-parameters of the transformer are compared. In the simulated results, the model of figure 2.19 was used with the values listed in figure 7.15. There is a good agreement between the (de-embedded) experimental and the simulation results, meaning that the transformer parameters obtained using the electromagnetic simulator ASITIC are trustworthy. The patterned ground shield does not affect significantly the transformer performance.

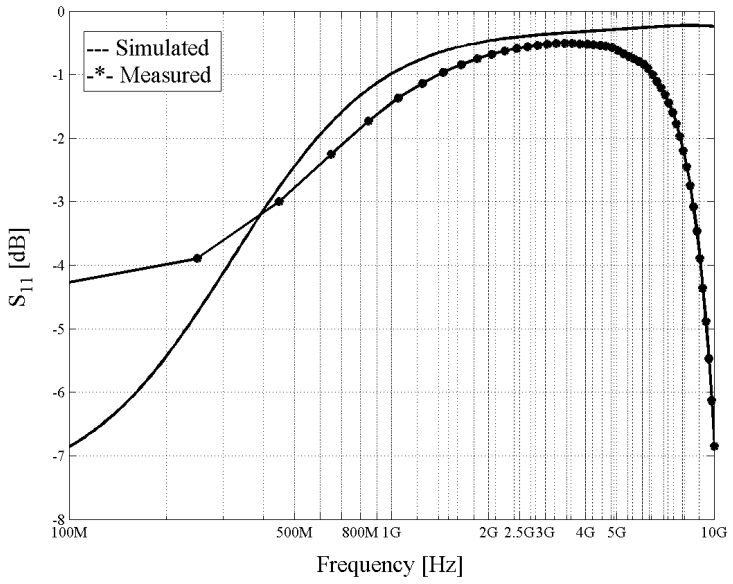

Figure 7.26: S_{11} of the transformer - experimental and simulated results.

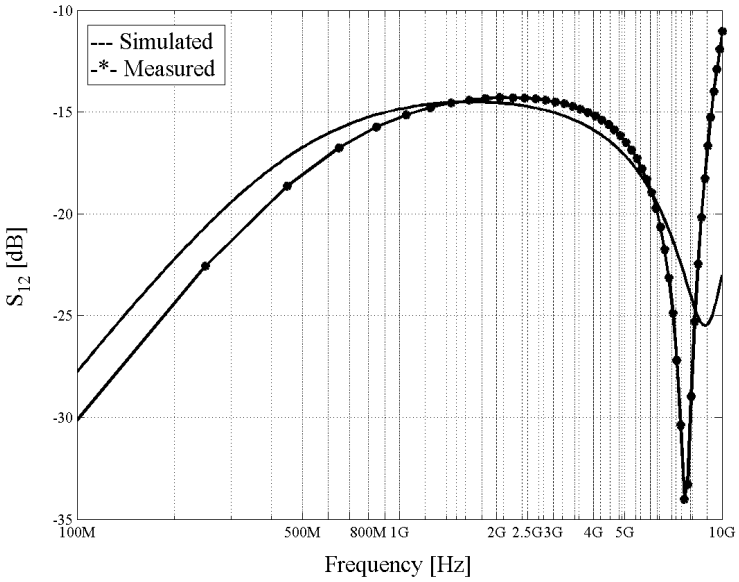

Figure 7.27: S_{12} of the transformer - experimental and simulated results.

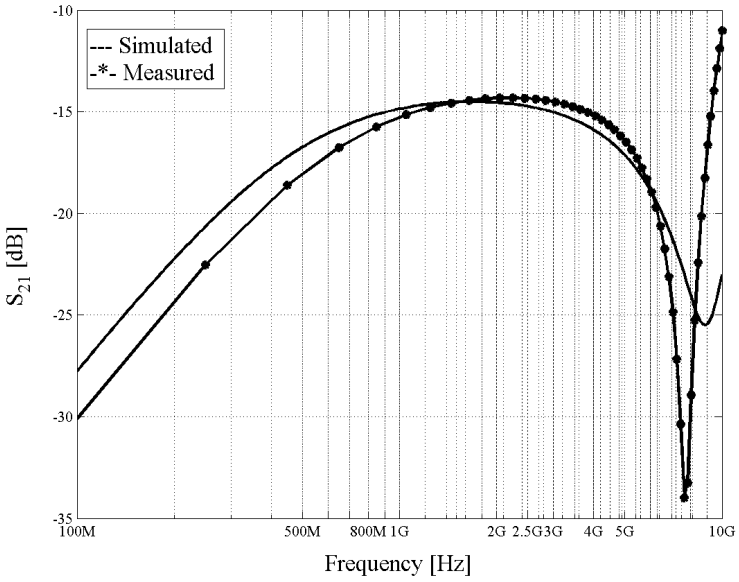

Figure 7.28: S_{21} of the transformer - experimental and simulated results.

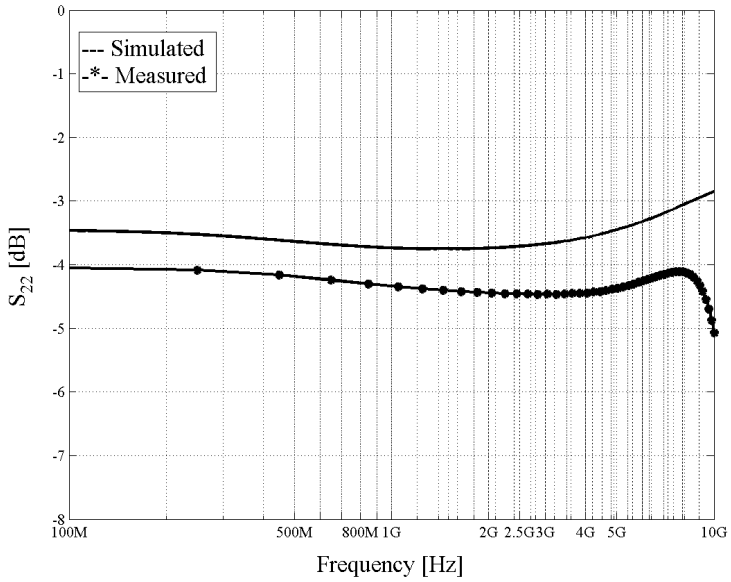

Figure 7.29: S_{22} of the transformer - experimental and simulated results.

7.5.2 LNA

Before testing the circuit, the maximum input power allowed at the LNA input was determined. The buffer has a current of 500 μA for an output impedance of 50 Ω. This allows a maximum voltage swing of 500 μA $\times$ 50 Ω = 25 mV. Considering a voltage gain of around 10, the maximum input peak-to-peak voltage is approximately 2.5 mV (or -39 dBm). The network analyzer power was then adjusted to -40 dBm. The DLF LNA is biased with a DC current of 10 mA.

Using the bias currents determined above, the circuit presents resonances in the S_{21} parameter. If the buffer bias current is varied to a higher value (approximately 40 mA), it is verified that the resonance disappears. One consequence of this increase was the degradation of the S_{22} parameter. Note that only the bias currents can be varied to debug the circuit.

To evaluate these results, a simulation of the test setup using the estimated of the bonding inductances was performed. The estimated bonding inductances are listed in table 7.5, and the bias currents and voltages measured at the test setup are listed in table 7.6. The experimental and simulated results considering the bonding inductances are represented in figures 7.30 to 7.33.

Table 7.5: Estimate of the bond wire inductances.

Inductance	Value	Inductance	Value
L_{GND}	1 nH	L_{VDD1}	1 nH
L_{VDD}	1 nH	L_{DLF}	3 nH
L_{BUF}	3 nH	L_{out}	3 nH
L_{in}	3 nH		

Table 7.6: DC voltages and currents.

Currents			
Current	Value	Current	Value
I_{BUF}	38.60 mA	I_{DLF}	5.02 mA
Voltages			
Voltage	Value	Voltage	Value
V_{BUF}	2.02 V	V_{DLF}	1.58 V
V_{in}	0.85 V	V_{out}	1.85 V

The measured S_{12} and S_{21} are in a good agreement with the simulation results. The measured and simulated results for S_{11} and S_{22} vary roughly in the same way with frequency, but there are significant differences of value. This is a consequence of the high sensitivity of these two S-parameters when the LNA input and output circuit impedances approach the 50 Ω characteristic impedance, since

$$S_{11} = 10 \log \left| \frac{Z_i - Z_0}{Z_i + Z_0} \right| \tag{7.5}$$

and

$$S_{22} = 10 \log \left| \frac{Z_L - Z_0}{Z_L + Z_0} \right| \tag{7.6}$$

where Z_i is the LNA input impedance, Z_L is the buffer output impedance and Z_0 is the test equipment impedance. If Z_i (or Z_L) and Z_0 are almost equal, S_{11} (or S_{22}) tend to $-\infty$.

In figure 7.34 the measured noise figure is represented and compared with the simulated results of the test setup considering the bonding inductances. Again, the strong influence of the bonding inductances on the noise figure is apparent.

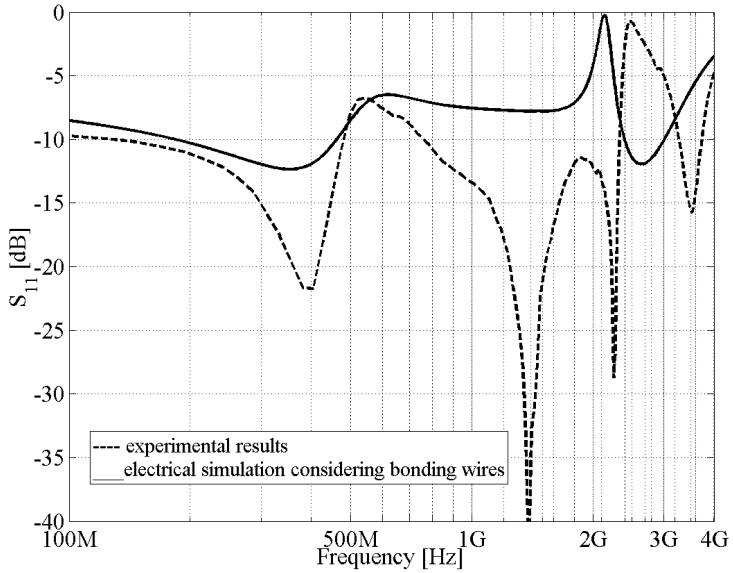

Figure 7.30: Measured S_{11} and simulation considering bonding inductances.

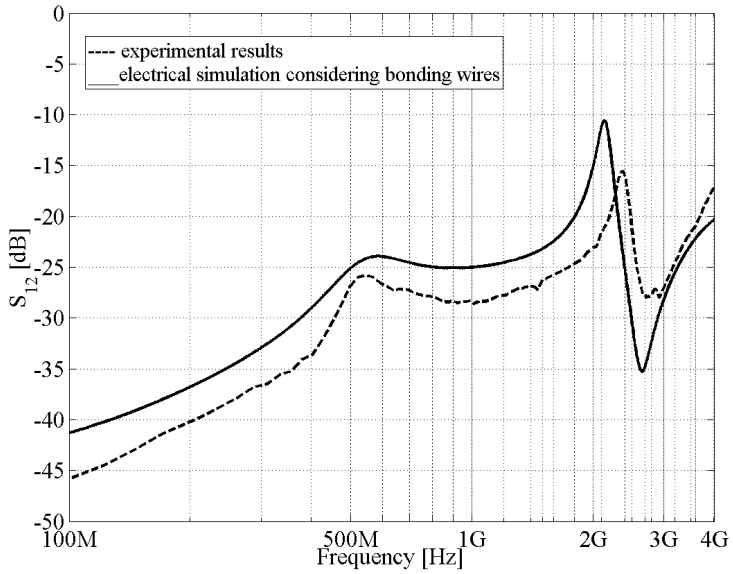

Figure 7.31: Measured S_{12} and simulation considering bonding inductances.

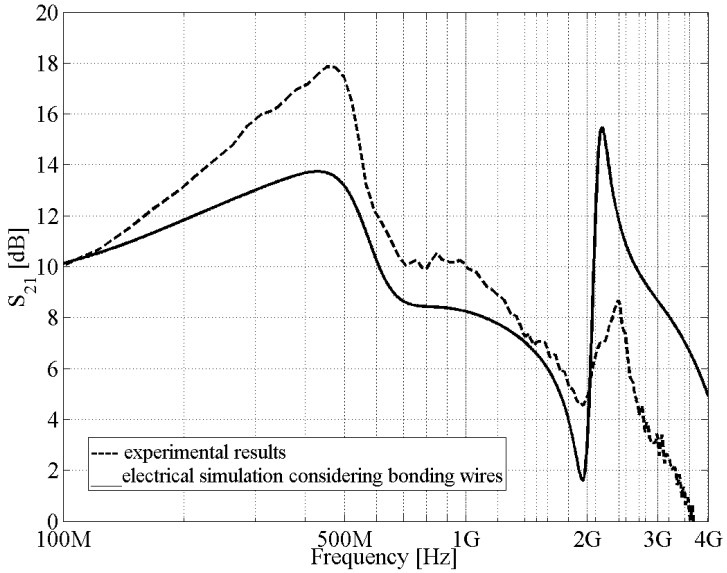

Figure 7.32: Measured S_{21} and simulation considering bonding inductances.

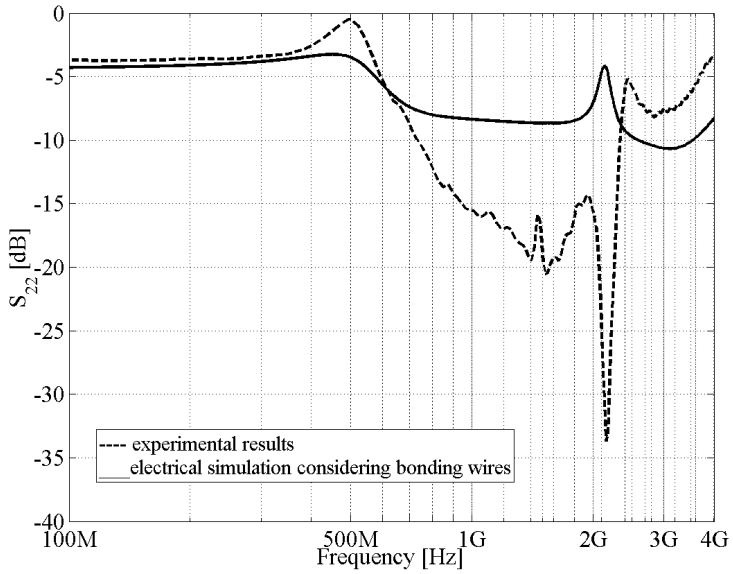

Figure 7.33: Measured S_{22} and simulation considering bonding inductances.

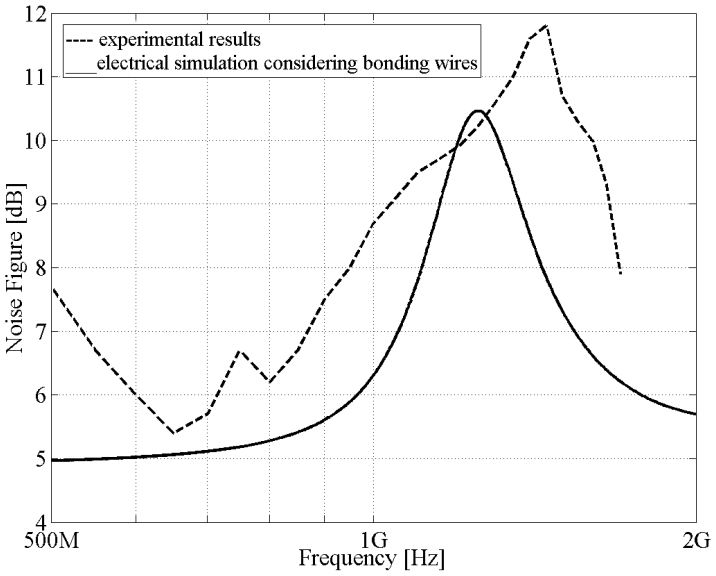

Figure 7.34: Measured noise figure and simulation considering bonding inductances.

7.5.3 Discussion and improvements for a second prototype

Due to the difference between the expected DLF LNA performance and that measured, it is desirable to design a second prototype of the circuit.

The test results show a strong influence of the bonding inductances, mainly of the voltage supply (verified by simulation). To reduce the bonding inductance several pads can be used for the voltage supply; in addition, a large capacitance can be placed in parallel with the voltage supply.

In figure 7.35 the layout of the second prototype is represented. Each terminal of the voltage supply has 10 pads, and a large capacitance (1.4 nF) is used to further minimize the bond wires effect.

In figures 7.36 to 7.40 the simulated S-parameters and the noise figure are represented, considering two different situations. In one situation (solid lines), the bonding inductances L_{GND} and L_{VDD} have 1 nH, which is the inductance value considered in the test setup used for the first prototype. In the other situation (dashed lines), the bonding inductances L_{GND} and L_{VDD} have 0.2 nH, which corresponds to 10 bonding wires in parallel, each one having an inductance of 2 nH (this is a pessimistic situation, because it assumes that each bonding has a length of

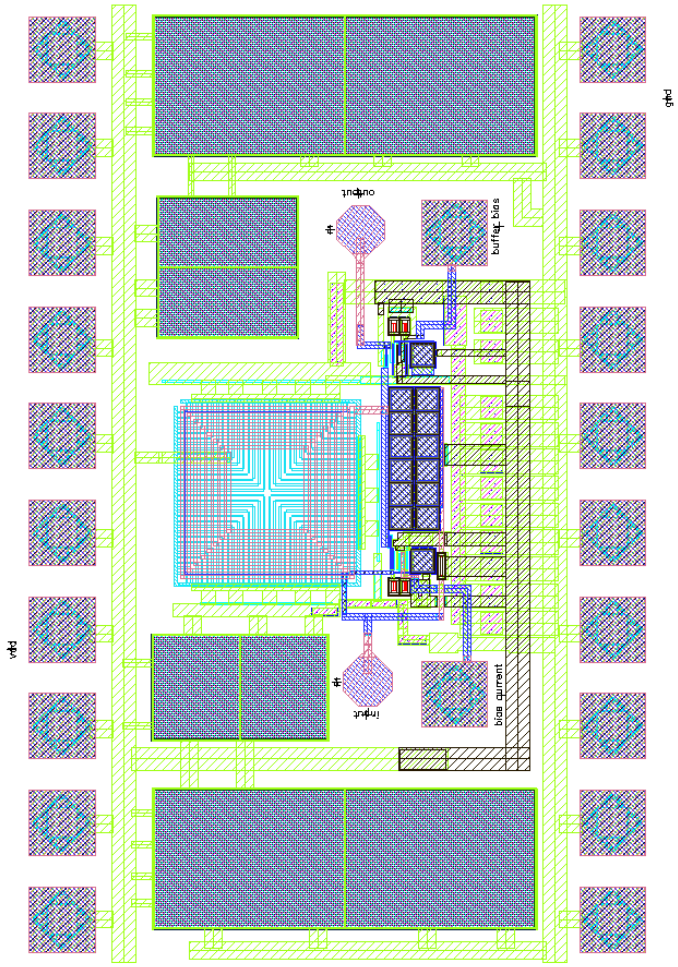

Figure 7.35: Layout of the second circuit prototype.

2 mm). It is visible that the effects of the bonding inductances are reduced in both curves of figures, the reduction being more significant when inductances L_{GND} and L_{VDD} are lower. If the bonding wire inductances are neglected, the S-parameters and noise figure are very similar to those in figures 7.17 to 7.21, obtained by simulation of the first prototype without the bonding inductances.

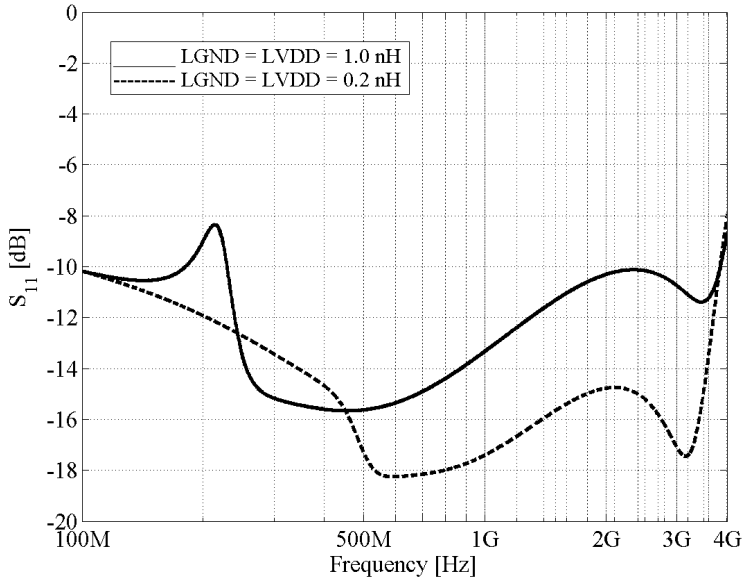

Figure 7.36: S_{11} considering $L_{GND} = L_{VDD} = 1$ nH (solid line) and $L_{GND} = L_{VDD} = 0.2$ nH (dashed line).

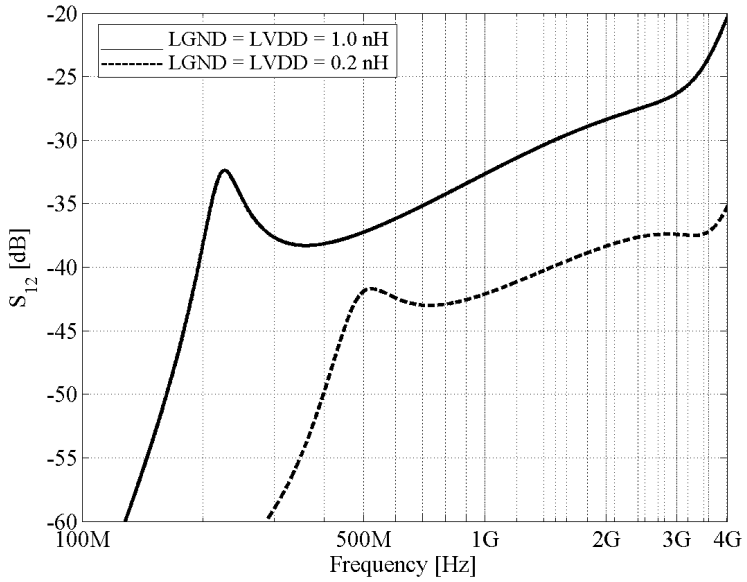

Figure 7.37: S_{12} considering $L_{GND} = L_{VDD} = 1$ nH (solid line) and $L_{GND} = L_{VDD} = 0.2$ nH (dashed line).

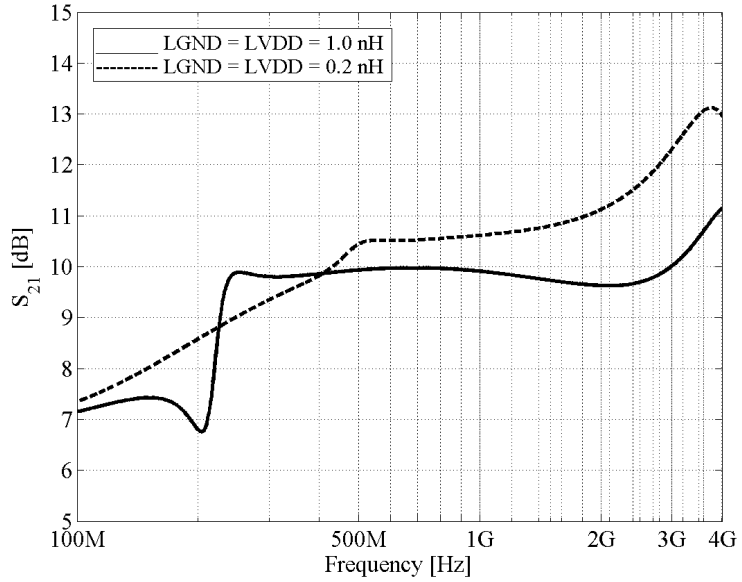

Figure 7.38: S_{21} considering $L_{GND} = L_{VDD} = 1$ nH (solid line) and $L_{GND} = L_{VDD} = 0.2$ nH (dashed line).

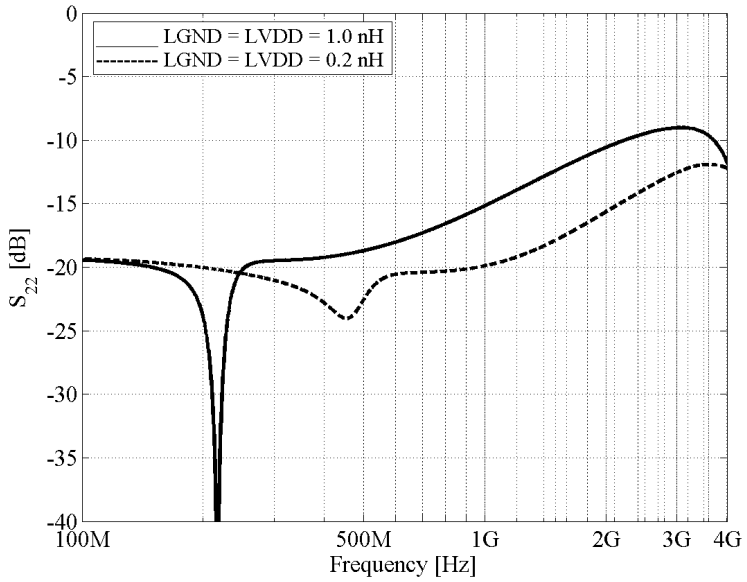

Figure 7.39: S_{22} considering $L_{GND} = L_{VDD} = 1$ nH (solid line) and $L_{GND} = L_{VDD} = 0.2$ nH (dashed line).

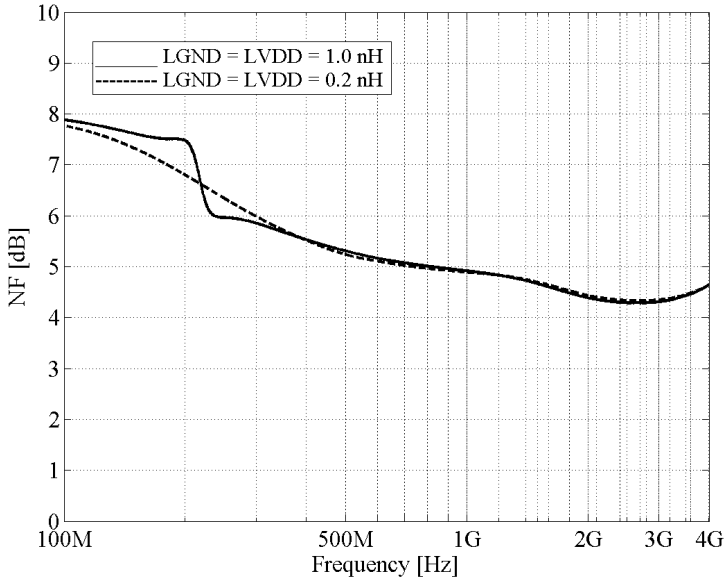

Figure 7.40: Noise figure considering $L_{GND} = L_{VDD} = 1$ nH (solid line) and $L_{GND} = L_{VDD} = 0.2$ nH (dashed line).

7.6 Conclusions

In this chapter, a prototype was designed and tested of the DLF LNA studied in chapter 6. The dimensioning of the different elements of the LNA and biasing circuits was explained.

The use of a single stage amplifying block is shown to be a good solution for the implementation of the DLF LNA. It was found that low output swing of the buffer limits the LNA input power.

The agreement between the simulated and measured results for the transformer confirms that the electromagnetic simulator ASITIC was a good choice for the design of the transformer.

The LNA test results are not in close agreement with the simulation results without bonding inductances, but the agreement is good when bonding inductances are considered in the simulations.

A second prototype was designed, in which the LNA circuit is identical to that in the first prototype, but the number of pads is increased with parallel wire bonding, to minimize the bonding inductances. A large capacitance was also placed in parallel with the voltage supply. The simulations show that this is an effective solution to minimize the negative effects of the bonding inductances.

Experimental results for the second prototype cannot be included in the thesis, since there was no time available for fabrication and testing.

Chapter 8

Conclusions and Future Work

8.1 Conclusions

At the beginning of wireless communication, most receivers were narrowband. However, the demand for more flexible receivers has led to the development of multi-band and wideband receivers. In this thesis, multi-band and wideband low noise amplifiers (LNAs) were studied.

The first multi-band LNA studied is based on a cascode stage with inductive degeneration and has wideband input impedance matching that embraces the bands to be amplified. At the output there are different resonant branches with their cascode transistors, each one tuned to a different band. The output branches can be active simultaneously, or some can be switched off by controlling the gate voltage of the cascode transistors. A noise analysis of this LNA shows that it keeps the noise performance of the basic cascode LNA. It is also shown that it is possible to vary the voltage gain in one band without affecting significantly the other band.

The proposed multi-band LNA has a circuit similar to the previous one, but has two resonant output branches that are magnetically coupled. The output is taken at one of the branches being present two bands simultaneously; this is known as a concurrent multi-band LNA. By varying the gate bias voltage of one of the cascode transistors, while keeping the other constant, it is possible to vary the relative voltage gain in the two bands. The range of variation depends on the width ratio of the cascode transistors. It is shown that the noise study of the first multi-band LNA is also applicable to this concurrent LNA.

The suitability of double loop feedback (DLF) to the realization of wideband LNAs was investigated in chapter 3. It was concluded that to obtain input impedance matching independent of the output load, both feedback networks must sample the same output variable (voltage or current) and compare different variables (voltage and current) at the input. Using one transformer and one resistance to realize the two feedback loops, four different LNA topologies are obtained: two of them sampling the output current and two sampling the output voltage. All four topologies were studied in terms of input impedance, gain, and noise figure.

One of the DLF LNAs with output voltage sampling at the output was studied in more detail. The LNA performance was evaluated considering a non-ideal transformer and an ideal amplifying block (nullor). It was concluded that the transformer parasitic elements limit the LNA band of operation, but it is still possible

to realize a wideband LNA. In a second part of the study, the transformer model is limited to two magnetically coupled inductors to simplify the analysis, and the amplifying block model includes its most important non-idealities. It is shown that a cascode stage should be used to minimize the effect of the drain-base capacitance of the input transistor. Equations for the minimum acceptable transconductance of this stage were developed. It was shown, using electrical simulations, that it is possible to realize a wideband DLF LNA with a reasonable power consumption.

A prototype of the above DLF LNA was designed. The transformer was designed using an electromagnetic simulator (ASITIC). Testing of the integrated transformer proved that the electromagnetic simulator is reliable. The experimental results of the DLF LNA were different from those obtained by simulation ignoring the bonding inductances; however, a good agreement was obtained with simulation results taking into account the bonding inductances, meaning that the circuit under test is very sensible to them.

In parallel with the work reported in this thesis, a method for the impedance evaluation of circular inductors was developed, but this was not included here, since it is somewhat outside the scope of the thesis.

8.2 Future Work

In the continuation of the research performed, the following further work could be done.

The concurrent multi-band LNA proposed in this thesis should be prototyped to evaluate its functionality. Two prototypes should be realized, with opposite magnetic coupling orientation. The design should follow the rules described in chapter 7 to overcome testing problems.

The DLF LNA prototype should be revised, preferably with the same technology, taking into account the bonding inductances.

The DLF LNA type 4, described in chapter 3.1, should be studied considering the transformer non-idealities to evaluate its performance limits. This study has already been done for the remaining topologies [24, 27].

The circuit presented in figure 4.3 can also be used to obtain dual mixing by making v_{BIAS1} and v_{BIAS2} the voltages of two local oscillators with different frequencies f_{L1} and f_{L2}, as represented in figure 8.1.

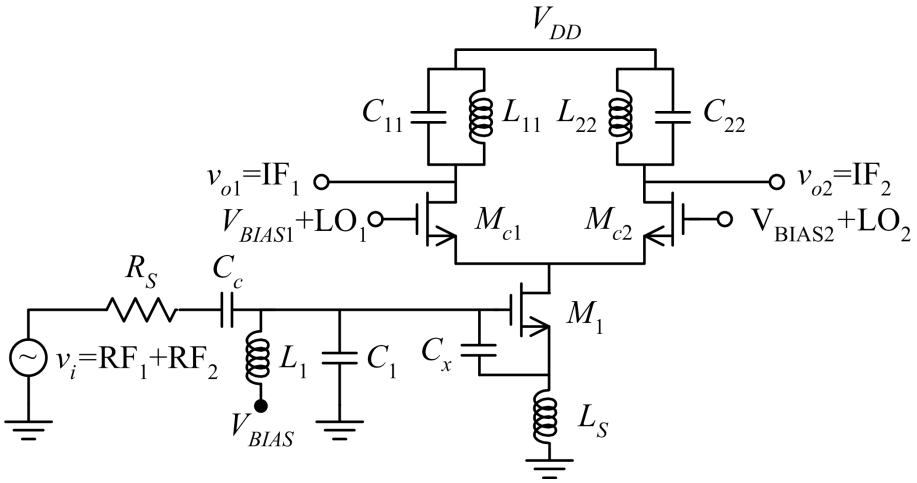

Figure 8.1: Proposed dual-band LNA - Mixer.

In this mode of operation the circuit of figure 8.1 can be viewed as a 2-quadrant variable transconductance multiplier, composed of a differential pair (M_{c1}, M_{c2}) and a controlled current source M_1; transistors M_{c1} and M_{c2} must remain in the active zone of operation.

If the input signal v_i has two frequency bands centered at f_{i1} and f_{i2}, the currents of M_{c1} and M_{c2} will contain 8 modulation products centered at frequencies $f_{L1} \pm f_{i1}$, $f_{L1} \pm f_{i2}$, $f_{L2} \pm f_{i1}$, $f_{L2} \pm f_{i2}$. Two of these can be selected to appear at the outputs (v_{o1} and v_{o2}) by tuning the output branches to the desired frequencies. This provides a great design flexibility, since the two frequencies are chosen from a set of eight. This circuit seems to have a potential that should be further explored.

Appendix A

2-Port Matrices

In table A.1, several 2-port matrix descriptions are presented. The voltages and currents are in accordance with figure A.1 [43].

Table A.1: 2-port matrix descriptions.

Reference	Matrix description	Name
Y	$\begin{bmatrix} i_1 \\ i_2 \end{bmatrix} = \begin{pmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{pmatrix} \begin{bmatrix} v_1 \\ v_2 \end{bmatrix}$	Admittance Matrix
Z	$\begin{bmatrix} v_1 \\ v_2 \end{bmatrix} = \begin{pmatrix} z_{11} & z_{12} \\ z_{21} & z_{22} \end{pmatrix} \begin{bmatrix} i_1 \\ i_2 \end{bmatrix}$	Impedance Matrix
H	$\begin{bmatrix} v_1 \\ i_2 \end{bmatrix} = \begin{pmatrix} h_{11} & h_{12} \\ h_{21} & h_{22} \end{pmatrix} \begin{bmatrix} i_1 \\ v_2 \end{bmatrix}$	Hybrid Matrix
H'	$\begin{bmatrix} i_1 \\ v_2 \end{bmatrix} = \begin{pmatrix} h'_{11} & h'_{12} \\ h'_{21} & h'_{22} \end{pmatrix} \begin{bmatrix} v_1 \\ i_2 \end{bmatrix}$	Dual Hybrid Matrix
T	$\begin{bmatrix} v_1 \\ i_1 \end{bmatrix} = \begin{pmatrix} t_{11} & t_{12} \\ t_{21} & t_{22} \end{pmatrix} \begin{bmatrix} v_2 \\ -i_2 \end{bmatrix}$	Chain Matrix

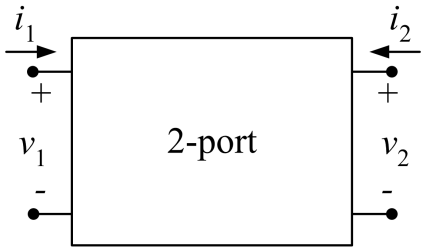

Figure A.1: 2-port block.

Appendix B

Poles and Zeros of the DLF LNA considering Transformer Parasitic Capacitances and Resistances

Consider figure B.1 of the of the double loop feedback low noise amplifier (DLF LNA) that considers the transformer including the series resistances R_{wi} and inter-winding capacitances C_{wi}.

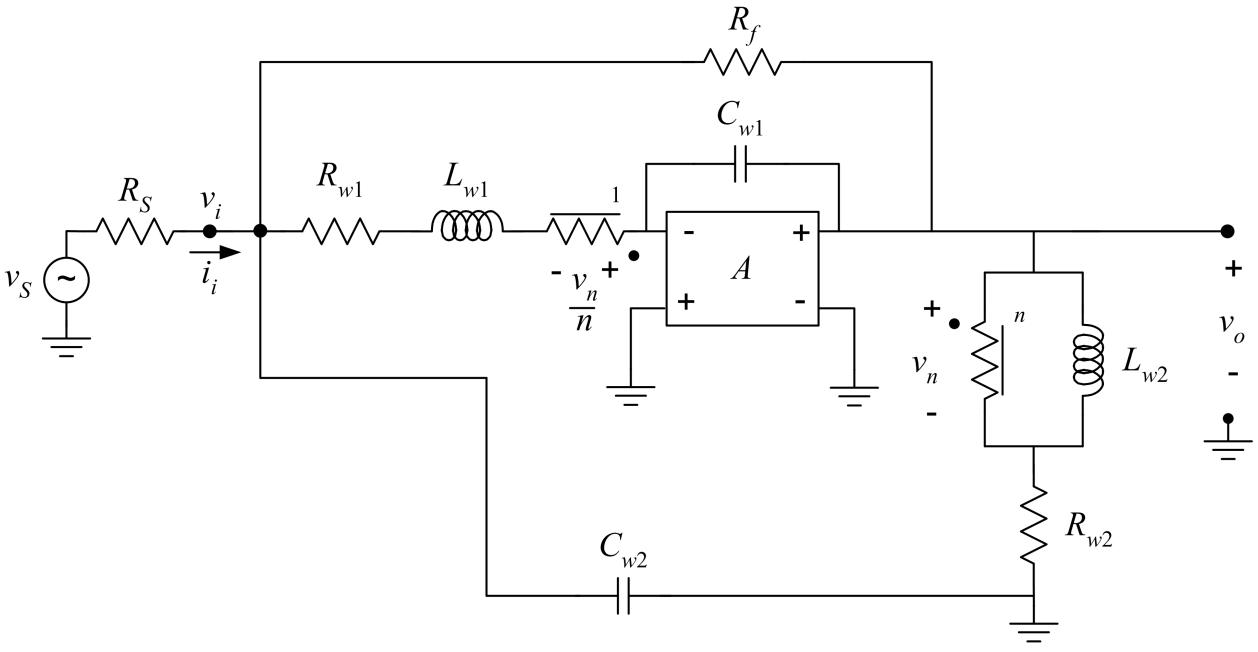

Figure B.1: DLF LNA with transformer model including winding inductances L_{wi}, series resistances R_{wi} and inter-winding capacitances C_{wi}.

B.1 Input Impedance Analysis

The first step to determine $Z_{in} = v_i/i_i$ consists on determining v_o/v_n:

$$v_o = v_n + \left(\frac{v_n}{sL_{w2}} + \frac{sC_{w1}}{n}v_o\right)R_{w2} \Leftrightarrow v_o = \frac{n(sL_{w2}+R_{w2})}{sL_{w2}(n+sC_{w1}R_{w2})}v_n \tag{B.1}$$

(B.1) is used to determine v_o/v_i,

$$\begin{aligned} v_i &= -\frac{v_n}{n} - (sL_{w1}+R_{w1})sC_{w1}v_o \Leftrightarrow \\ \Leftrightarrow v_o &= -\frac{n^2(sL_{w2}+R_{w2})}{sL_{w2}(n+sC_{w1}R_{w2}) + n^2(sL_{w2}+R_{w2})(sL_{w1}+R_{w1})sC_{w1}}v_i \end{aligned} \tag{B.2}$$

Finally, i_i is determined

$$i_i = sC_{w2}v_i + \frac{v_i - v_o}{R_f} - sC_{w1}v_o \tag{B.3}$$

The input impedance Z_{in} is determined using (B.2) and (B.3):

$$\begin{aligned} Z_{in} = \frac{v_i}{i_i} = \\ = \frac{R_f[sL_{w2}(1+n^{-1}sC_{w1}R_{w2}) + (sL_{w2}+R_{w2})(sL_{w1}+R_{w1})sC_{w1}]}{(1+R_fsC_{w2})[sL_{w2}(1+n^{-1}sC_{w1}R_{w2}) + n(sL_{w2}+R_{w2})(sL_{w1}+R_{w1})sC_{w1}] + n(1+R_fsC_{w1})(sL_{w2}+R_{w2})} \end{aligned} \tag{B.4}$$

To determine the poles and zeros of Z_{in}, it is assumed that different frequency ranges exist. At lower frequencies, it is assumed that the influence of C_{w1} and C_{w2} is not significant; i.e. $C_{w1} = C_{w2} = 0$, becoming Z_{in}

$$Z_{in}(s) = \frac{v_i}{i_i}(s) = \frac{R_fsL_{w2}}{(n+1)sL_{w2}+nR_{w2}} = \frac{R_fL_{w2}}{nR_{w2}}\frac{s}{1+\dfrac{s}{\omega_{p1,Zin}}} \tag{B.5}$$

(B.5) has one zero at the origin and one pole at

$$\omega_{p1,Zin} = \frac{nR_{w2}}{(n+1)L_{w2}} \tag{B.6}$$

At high frequencies the simplification assumed is $sL_{w2} \gg R_{w2}$

$$\begin{aligned} Z_{in} = \frac{v_i}{i_i} = \\ \frac{R_f[1+n^{-1}sC_{w1}R_{w2} + (sL_{w1}+R_{w1})sC_{w1}]}{(1+R_fsC_{w2})[1+n^{-1}sC_{w1}R_{w2} + n(sL_{w1}+R_{w1})sC_{w1}] + n(1+R_fsC_{w1})} \end{aligned} \tag{B.7}$$

C_{w1} and C_{w2} model the distributed capacitance between transformer windings 1 and

2. At the transformer model they are considered lumped and connected between the winding terminals. The total capacitance is usually distributed equally through C_{w1} and C_{w2} meaning that these capacitances can be assumed as having the same value. Considering $C_{w2} = C_{w1}$, (B.7) simplifies to

$$Z_{in} = \frac{v_i}{i_i} = \frac{R_f}{n+1}\frac{[1 + n^{-1}sC_{w1}R_{w2} + (sL_{w1} + R_{w1})sC_{w1}]}{(1 + R_f sC_{w1})[1 + n^{-1}sC_{w1}R_{w2} + n(sL_{w1} + R_{w1})sC_{w1}]} \tag{B.8}$$

(B.8), one single pole is directly determined and is equal to:

$$p_{2,Zin} = -\frac{1}{R_f C_{w1}} \tag{B.9}$$

The remaining poles are determined from the equality

$$1 + n^{-1}sC_{w1}R_{w2} + n(sL_{w1} + R_{w1})sC_{w1} = 0 \Leftrightarrow \tag{B.10}$$

$$\Leftrightarrow s^2 n^2 L_{w1}C_{w1} + sC_{w1}(n^2 R_{w1} + R_{w2}) + n = 0 \tag{B.11}$$

Now, assuming that $n^2 R_{w1} \gg R_{w2}$ and that a second order polynomial can be written in the following form,

$$s^2 + \frac{\omega_0}{Q}s + \omega_0^2 = 0 \tag{B.12}$$

where ω_0 is the pole frequency and Q is the quality factor. With this in mind, $\omega_{p3,Zin}$ and $Q_{p3,Zin}$ are determined:

$$\omega_{p3,Zin}^2 \approx \frac{1}{nL_{w1}C_{w1}} \tag{B.13}$$

$$Q_{p3,Zin} \approx \frac{1}{R_{w1}}\frac{1}{\sqrt{n}}\sqrt{\frac{L_{w1}}{C_{w1}}} \tag{B.14}$$

Concerning the zero of (B.8) it is determined by next equality:

$$1 + n^{-1}sC_{w1}R_{w2} + (sL_{w1} + R_{w1})sC_{w1} = 0 \Leftrightarrow \tag{B.15}$$

$$\Leftrightarrow s^2 nL_{w1}C_{w1} + sC_{w1}(nR_{w1} + R_{w2}) + n = 0 \tag{B.16}$$

Considering (B.12), $\omega_{z2,Zin}$ and $Q_{z2,Zin}$ are determined:

$$\omega_{z2,Zin}^2 \approx \frac{1}{L_{w1}C_{w1}} \tag{B.17}$$

$$Q_{z2,Zin} \approx \frac{n}{nR_{w1}+R_{w2}}\sqrt{\frac{L_{w1}}{C_{w1}}} \tag{B.18}$$

B.2 Voltage Gain Analysis

To determine the voltage gain v_o/v_S, it is considered the next equality:

$$i_i = \frac{v_S - v_i}{R_S} \tag{B.19}$$

(B.19) and (B.3) are used to obtain next equality:

$$\begin{aligned} &\frac{v_S - v_i}{R_S} = sC_{w2}v_i + \frac{v_i - v_o}{R_f} - sC_{w1}v_o \Leftrightarrow \\ &\Leftrightarrow \left(\frac{1}{R_f} + sC_{w1}\right)v_o - \left(\frac{1}{R_S} + \frac{1}{R_f} + sC_{w2}\right)v_i = -\frac{1}{R_S}v_S \end{aligned} \tag{B.20}$$

$A_v = v_o/v_S$ is determined by using (B.2) in (B.20). The representation of A_v does not give any inside over the circuit besides being a too large expression. Thus, A_v will be determine considering several frequency ranges. At lower frequencies, it is assumed that the interstage capacitances do not have effect on the voltage gain; i.e., $C_{w1} = C_{w2} = 0$. It is also assumed that $R_f = R_S(n+1)$ (input impedance matching condition). Under these conditions, A_v becomes:

$$A_v(s) = \frac{v_o}{v_S}(s) = -\frac{n(n+1)(sL_{w2}+R_{w2})}{2(n+1)sL_{w2}+nR_{w2}} \tag{B.21}$$

(B.21) has one single zero and one single pole located at

$$\omega_{p1,Av} = -\frac{1}{2}\frac{n}{n+1}\frac{R_{w2}}{L_{w2}} \tag{B.22}$$

$$\omega_{z1,Av} = -\frac{R_{w2}}{L_{w2}} \tag{B.23}$$

After $p_{1,Av}$ and $z_{1,Av}$, sL_{w2} becomes dominant over R_{w2}. Assuming again the input

matching condition $R_f = R_S(n+1)$, A_v becomes

$$A_v = \frac{v_o}{v_s} = \tag{B.24}$$

$$= -\frac{n^2(n+1)}{(2n^2C_{w1}L_{w1} + n^3C_{w1}L_{w1})s^2 + (n^2C_{w1}R_S + n^3C_{w1}R_S + 2C_{w1}R_{w2} + nC_{w1}R_{w2})s + 2n^2 + 2n}$$

(B.24) does not have zeros. To determine the pole consider next approximations:

- $n^3C_{w1}L_{w1} \gg 2n^2C_{w1}L_{w1}$;
- $n^3C_{w1}R_S \gg n^2C_{w1}R_S + 2C_{w1}R_{w2} + nC_{w1}R_{w2}$;
- $n^2 \gg n$

The above approximations allow (B.24) to be simplified further to

$$A_v = \frac{v_o}{v_s} = -\frac{(n+1)}{nC_{w1}L_{w1}s^2 + nC_{w1}R_Ss + 2} \tag{B.25}$$

Considering (B.12), (B.28) has a pair of complex poles at

$$\omega_{p2,Av}^2 \approx \frac{1}{nL_{w1}C_{w1}} \tag{B.26}$$

and having a quality factor of

$$Q_{p2,Av} \approx \frac{1}{R_S}\sqrt{\frac{2}{n}}\sqrt{\frac{L_{w1}}{C_{w1}}} \tag{B.27}$$

At frequencies above $\omega_{p2,Av}$ next approximations can be made over equality (B.20):

- $sL_{w1} \gg R_{w1}$;
- $sL_{w2} \gg R_{w2}$;
- $sC_{w1}R_{w2} \gg n$;
- $sC_{w1} \gg 1/R_f$;
- $sC_{w2} \gg 1/R_f$;

A_v becomes

$$A_v = \frac{v_o}{v_s} = -\frac{n}{nC_{w1}^2L_{w1}R_Ss^3 + ((n+1)R_S + nL_{w1}s)C_{w1}s + 1} \tag{B.28}$$

Considering $nL_{w1}s \gg (n+1)R_S$ and 1 negligible in comparison with the other denominator terms, (B.28) simplifies further to

$$A_v = \frac{v_o}{v_s} = -\frac{1}{C_{w1}^2 L_{w1} R_S s^3 + L_{w1} C_{w1} s^2} \tag{B.29}$$

(B.29) has a pole at

$$p_{3,Av} \approx -\frac{1}{R_S C_{w1}} \tag{B.30}$$

Appendix C

Source Transformations

In this appendix, some source transformation rules suitable for noise analysis are presented [23, 41, 47].

The Blakesley transformation or noise voltage source shifting is represented in figure C.1. The polarity of the new voltage sources must be respected as represented, to ensure the network equations are not changed.

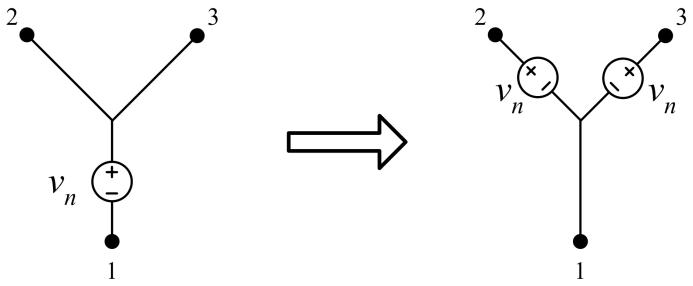

Figure C.1: Voltage source shifting (Blakesley transformation).

A current source can be split into two current sources having the same value, and being connected to one of the terminals of the original current source - figure C.2. Their polarity must be as indicated.

The voltage source v_n in series with the resistance R has a Norton equivalent that is a current source $i_n = v_n/R$ in parallel with resistance R as represented in figure C.3, and vice-versa.

In a 2-port, it is possible to transfer a source connected to one of the ports to the other port. Consider the 2-port of figure C.4.a) characterized by a chain matrix **T**

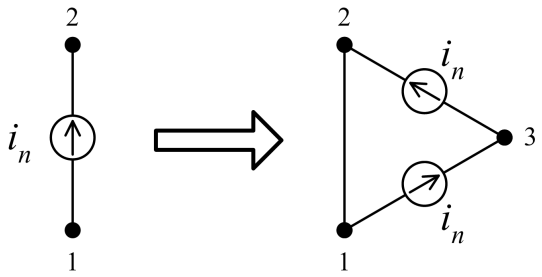

Figure C.2: Splitting of a current source.

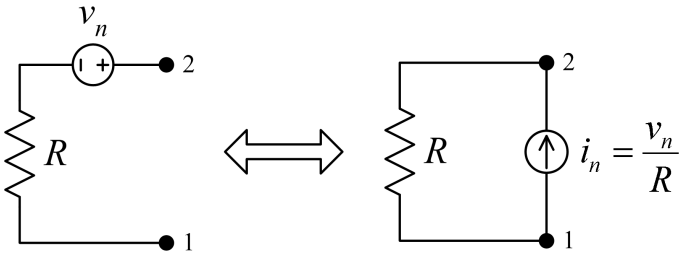

Figure C.3: Norton-Thevenin sources equivalence.

and having a voltage source and a current source at output. The resulting sources at the input have the values represented in figure C.4.b). If the 2-port is a nullor, all terms of the chain matrix are zero, and this transfer is not applied - the input sources are zero.

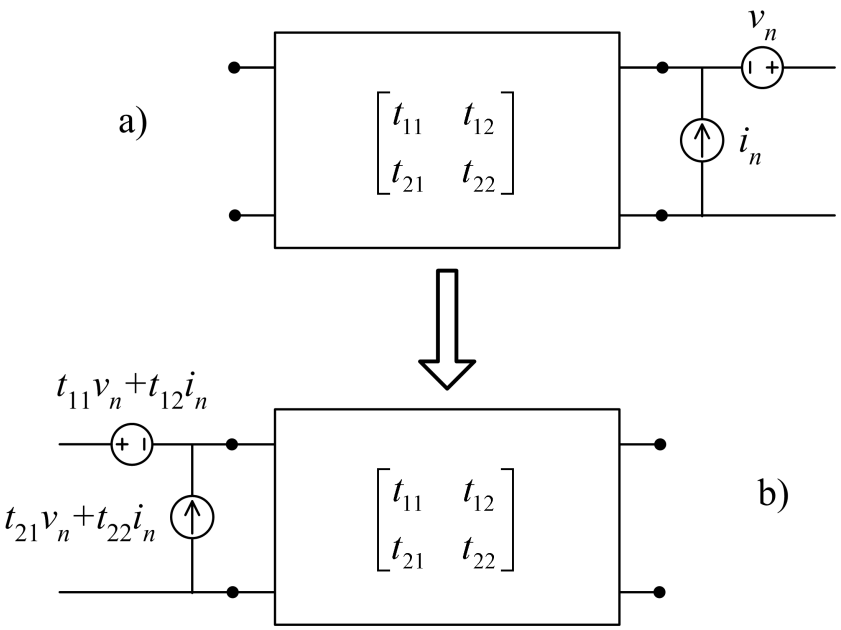

Figure C.4: 2-port transformation of noise sources.

Appendix D

DLF LNA Input Noise Sources

In this appendix, the equivalent noise sources referred to the input of the DLF LNA noise sources are determined. They use the source transformations presented in appendix C.

D.1 Demonstration of (6.12)

In figure D.1, the different noise sources considered in the determination of (6.12) are represented. In this circuit, the amplifying block is considered an ideal voltage amplifying block with infinite voltage gain and input impedance and a zero output impedance. The amplifying block is noiseless.

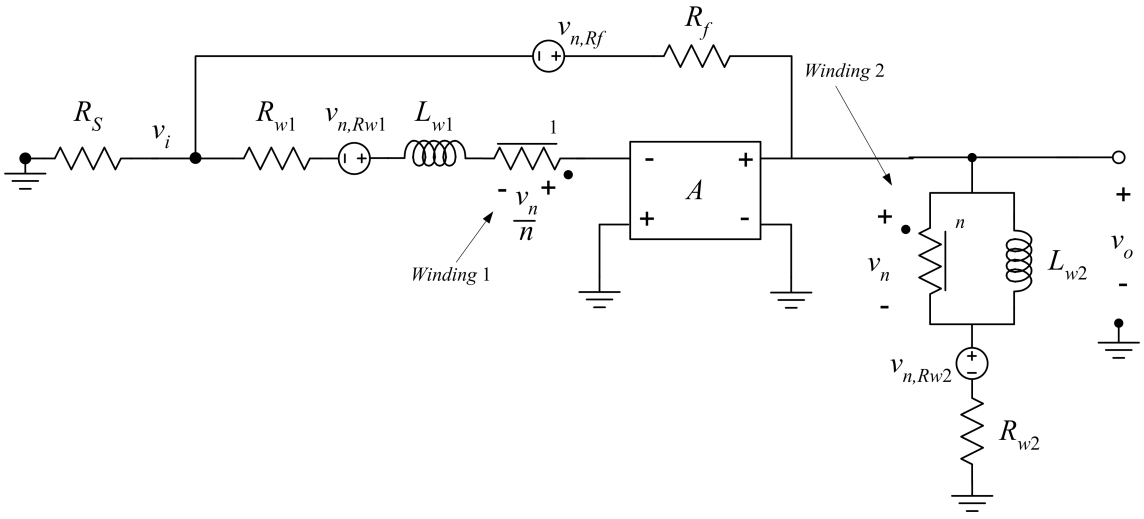

Figure D.1: DLF LNA noise sources.

In figure D.2 the noise voltage source $v_{n,Rw2}$ due to R_{w2} is transformed towards the

DLF LNA input.

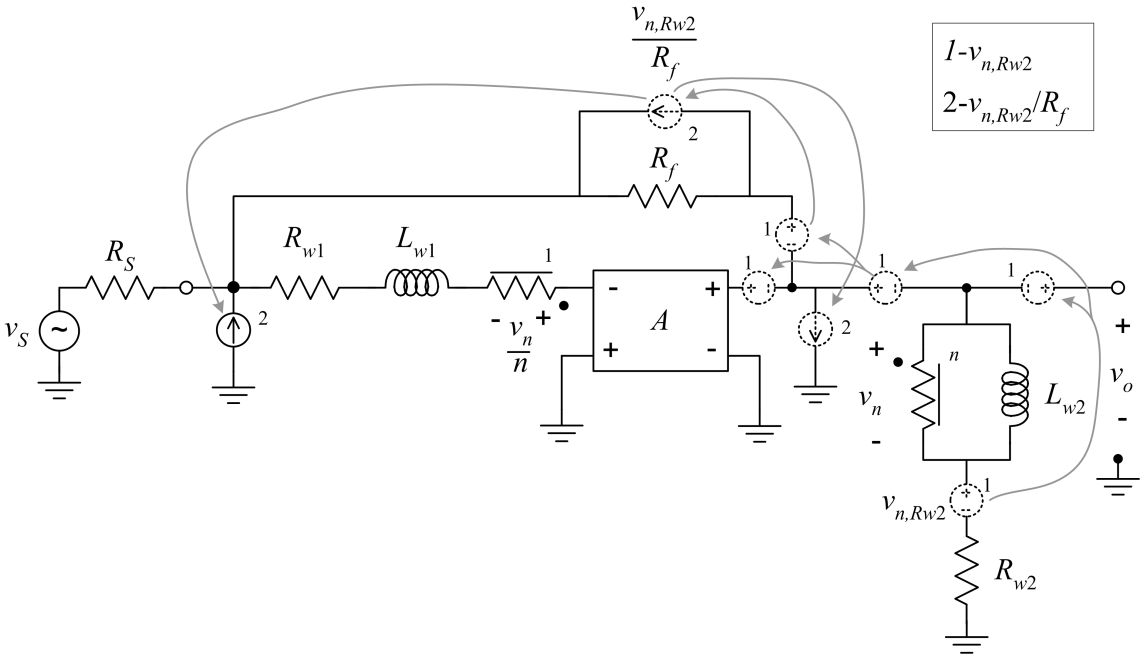

Figure D.2: Transformation of the noise voltage source $v_{n,Rw2}$.

In step 1, the voltage source is moved towards the DLF LNA output and split into three sources, one in series with the output, one in series with the amplifying block output and one in series with R_f. The first two are canceled because they are in parallel with the zero output impedance of the ideal amplifying block, while the remaining is converted to a current source $v_{n,Rw2}/R_f$ at R_f, by the Norton equivalence - step 2. This current source is split into one current source in parallel with the source resistance R_S and one current source in parallel with the zero output impedance of the amplifying block. The equivalent voltage noise source $v_{n,i,Rw2}$ due to R_{w2} is then

$$v_{n,i,Rw2} = \frac{R_S}{R_f} v_{n,Rw2} \tag{D.1}$$

In figure D.3 the voltage noise source $v_{n,Rf}$ due to R_f is moved towards input. It is firstly transformed to a current source by the Norton equivalence and then split into two current sources, one connected in parallel with the source resistance R_S and one connected to the amplifying block output. The second is canceled due to the ideality of the amplifying block (the output impedance is zero).

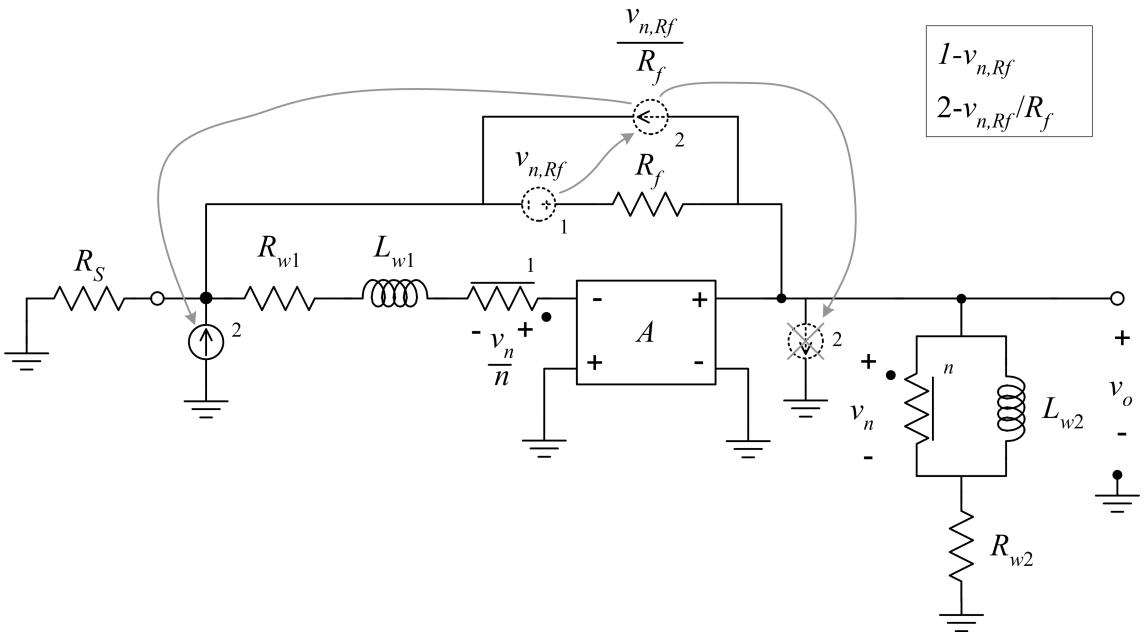

Figure D.3: Transformation of the noise voltage source $v_{n,Rf}$.

The equivalent voltage noise source $v_{n,i,Rf}$ due to R_f is

$$v_{n,i,Rf} = \frac{R_S}{R_f} v_{n,Rf} \tag{D.2}$$

In figure D.4 the voltage noise source $v_{n,Rw1}$ due to R_w1 is moved towards input. The initial noise voltage source is split into two voltage sources, one connected in series with the source resistance R_S and one in series with the R_f. The second is transformed to the input like that in the last example.

The equivalent voltage noise source $v_{n,i,Rw1}$ due to R_w1 is

$$v_{n,i,Rw1} = \left(1 + \frac{R_S}{R_f}\right) v_{n,Rw1} \tag{D.3}$$

The total input noise voltage is the sum of (D.1) to (D.3), resulting:

$$\begin{aligned} v_{n,i} &= v_{n,i,Rw1} + v_{n,i,Rw2} + v_{n,i,Rf} = \\ &= \frac{R_S}{R_f}(v_{n,Rw1} + v_{n,Rw2} + v_{n,Rf}) + v_{n,Rw1} \end{aligned} \tag{D.4}$$

Assuming $R_f = (n+1)R_S$, and using the Wiener-Khintchine theorem (2.29), the

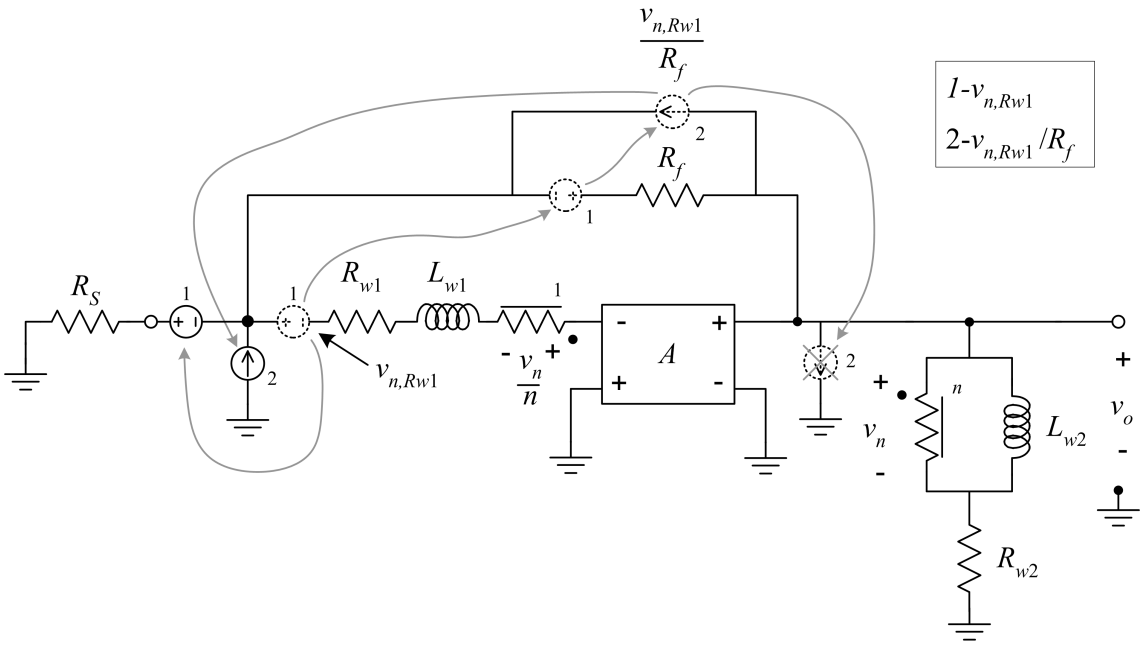

Figure D.4: Transformation of the noise voltage source $v_{n,Rw1}$.

DLF LNA equivalent input spectral noise density becomes:

$$N_i = 4k_BT[R_f + R_{w2} + R_{w1}]\left(\frac{1}{n+1}\right)^2 + 4k_BTR_{w1} \tag{D.5}$$

D.2 Demonstration of (6.44)

In figure D.5, the different noise sources considered in the determination of (6.12) are represented. In this circuit, the amplifying block is considered an ideal voltage amplifying block with infinite voltage gain and input impedance and a zero output impedance. The amplifying block has two noise sources at its input: $v_{n,A}$ and $i_{n,A}$.

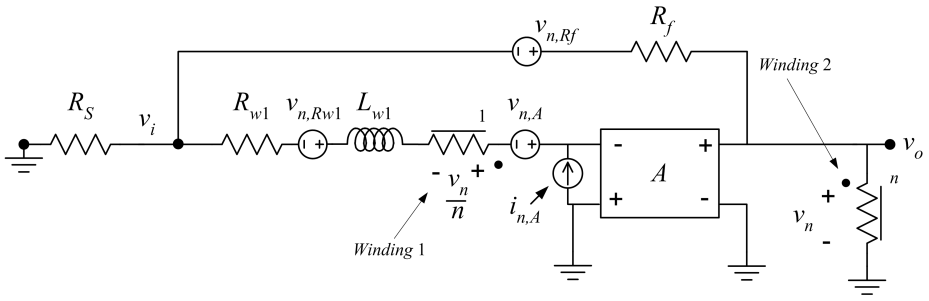

Figure D.5: DLF LNA noise sources.

The equivalent noise voltage and current sources due to $v_{n,A}$ are similar to that

determined to $v_{n,Rw1}$:

$$v'_{n,i,A} = v_{n,A} \tag{D.6}$$

$$i'_{n,i,A} = \frac{1}{R_f} v_{n,A} \tag{D.7}$$

The equivalent noise current source due to $v_{n,Rf}$ is equal to that determined in section D.1 and is

$$i_{n,i,Rf} = \frac{1}{R_f} v_{n,Rf} \tag{D.8}$$

Finally, in figure D.6 are represented the source transformations to determine the equivalent noise sources referred to the input and due to $i_{n,A}$.

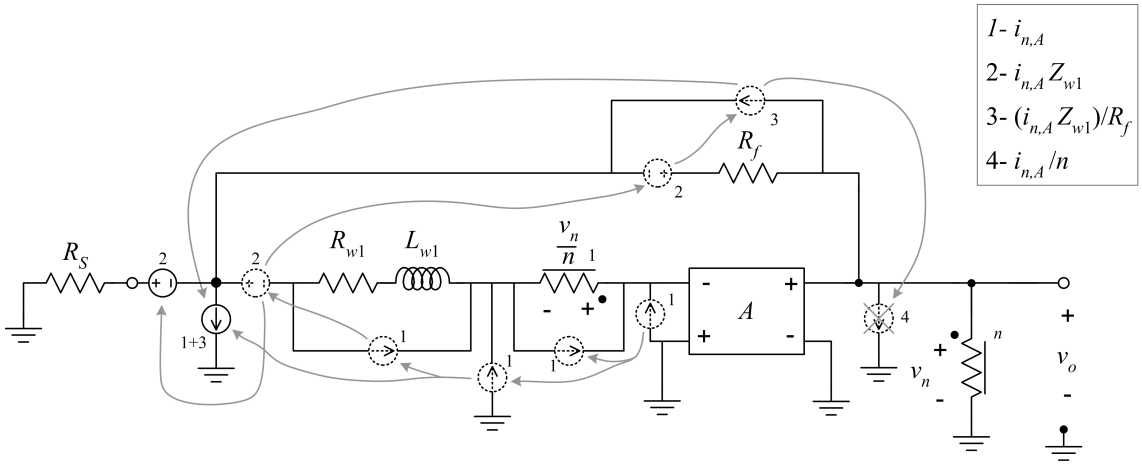

Figure D.6: Transformation of the noise voltage source $v_{n,Rw1}$.

The current source $i_{n,A}$ is firstly split into two current sources, one in parallel with winding 1 and the other connected between the winding and L_{w1}. The current source in parallel with winding 1 is translated to the output via the transformer current gain; and there, the current source is killed by the zero output impedance of the amplifying block. The second current source is again split into one current source in parallel with the series of L_{w1} and R_{w1} and one current source in parallel with the source resistance R_S. The current source ... is converted to a voltage source $i_{n,A}Z_{w1}$ and from now on, its treatment is similar to that of $v_{n,Rw1}$. The equivalent

noise voltage and current sources due to $i_{n,A}$ are:

$$v''_{n,i,A} = Z_{w1} i_{n,A} \tag{D.9}$$

$$i''_{n,i,A} = \left(1 + \frac{Z_{w1}}{R_f}\right) i_{n,Amp} \tag{D.10}$$

Z_{w1} is the impedance due to the series of L_{w1} and R_{w1}.
The equivalent input noise voltage is:

$$\begin{aligned} v'_{n,i} = v_{n,i} + i_{n,i} R_S = \frac{1}{R_f}(R_f + R_S)(v_{n,A} + v_{n,R_{w1}}) + \\ + \left(\frac{Z_{w1}}{R_f}(R_f + R_S) + R_S\right) i_{n,A} + \frac{R_S}{R_f} v_{n,R_f} \end{aligned} \tag{D.11}$$

where $v_{n,i}$ and $i_{n,i}$ are

$$v_{n,i} = v'_{n,i,A} + v''_{n,i,A} \tag{D.12}$$

$$v_{n,i} = i'_{n,i,A} + i''_{n,i,A} + i_{n,i,R_f} \tag{D.13}$$

Appendix E

Technology File for ASITIC Program

The technology file used in the ASITIC program to design the inductors used along the work is listed below. Figure E serves to a better understanding of the technology file.

Technology File:

```
<chip>
        chipx = 512    ; dimensions of the chip in x direction in microns
        chipy = 512    ; dimensions of the chip in y direction
        fftx = 1024     ; x-fft size (must be a power of 2)
        ffty = 1024     ; y-fft size
        TechFile = tech_sige.tek   ; the name of this file
        TechPath = /home/mam/ ; the pathname of the data files
        freq = .1

<layer> 0     ; Bulk Substrate

        rho = 19                ; Resistivity:  ohm-cm
        t   = 700               ; Thickness:  microns
        eps = 11.9              ; Permitivity:  relative

<layer> 1     ; Oxide Layer

        rho = 1e10              ; ohm-cm
        t = 10                   ; microns
```

```
        eps = 4                 ; relative

<metal> 0     ; metal layer 1

        layer = 1
        rsh = 70
        t = 0.665
        d =  0.927
        name = m1
        color = red


<metal> 1     ; metal 2

        layer = 1
        rsh =   70
        t   = 0.640
        d = 2.592
        name = m2
        color = blue


<metal> 2     ; metal 3

        layer = 1
        rsh =   70
        t   = 0.640
        d = 4.232
        name = m3
        color = green


<metal> 3     ; metal 4

        layer = 1
        rsh =   10
        t   = 2.800
```

```
d = 5.872
name = m4
color = yellow
```

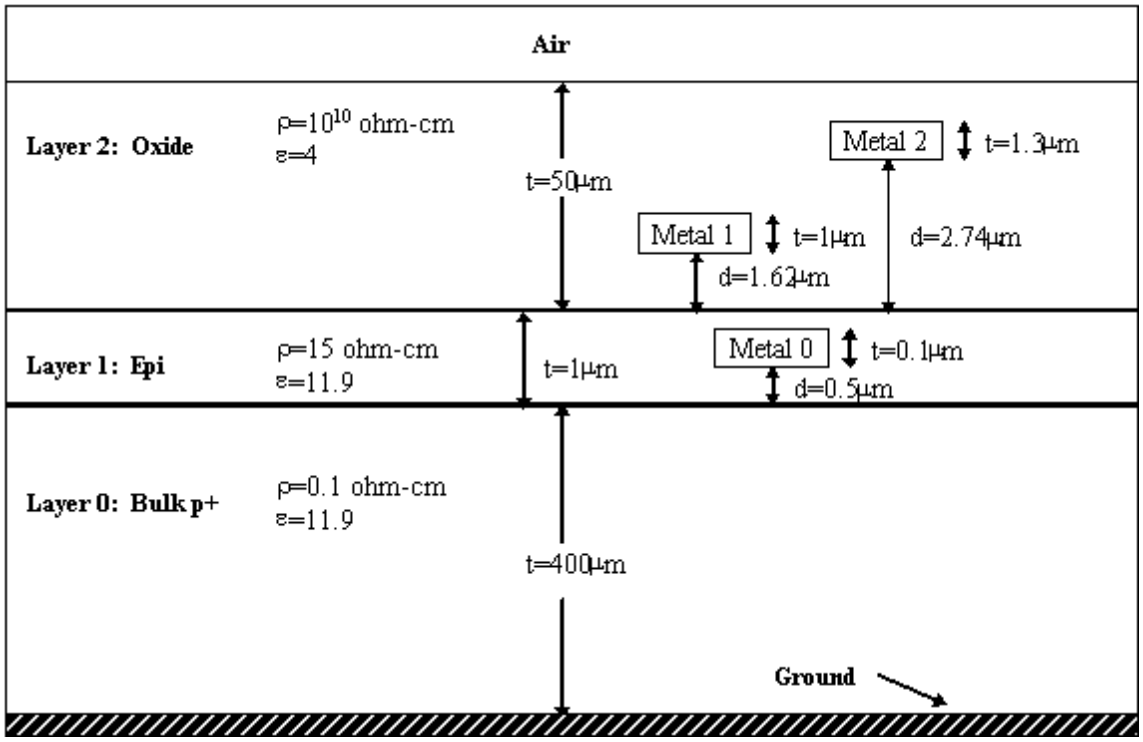

Figure E.1: Figure containing the different layers of a technology process.

Appendix F

Impedance Evaluation of Integrated Circular Spiral Inductors

The work presented in this appendix was realized in collaboration with professors Vitor Maló Machado and Luís Bica de Oliveira, during the course of *Simulation Tools for Electromagnetics*, and resulted in a publication [30]. It is presented in appendix because it is more related with element analysis, while the thesis is more dedicated to circuit analysis; however, it gives a good inside on problems related with inductance determination.

F.1 Introduction

An inductor is a "circuit element which is a conductor wrapped into a coil to create a magnetic field" [130]. "The voltage across an inductor is directly proportional to the rate of change of the current through it divided by the rate of change of time (difference current/difference time = $\frac{di}{dt}$). The proportionality constant which makes this true is L, the inductance of the inductor component. It is denoted by L and its units are the Henry (H). Therefore, the voltage v across an inductor is given by

$$v = L\frac{di}{dt} \tag{F.1}$$

"[130].

The aim of this work is the determination of the inductance of a spiral integrated inductor. To obtain inductance value L of equation (F.1) it is necessary to describe

the electromagnetic fields, define the material conditions, the boundaries, etc... The electromagnetic field is described by *Maxwell Equations*. Their local form are showed below:

$$\nabla \times H = J + \frac{\partial D}{\partial t} \tag{F.2}$$

$$\nabla \times E = -\frac{\partial B}{\partial t} \tag{F.3}$$

$$\nabla \cdot D = \rho \tag{F.4}$$

$$\nabla \cdot B = 0 \tag{F.5}$$

B is the magnetic field, E is the electric field, H is the magnetic field strength, D is the electric displacement and ρ is the charge density. Equation (F.2) with the omission of the electric displacement density from the second term, $\frac{dD}{dt}$ represents the local form of the *Ampere* equation: a current density J that generates a magnetic field H, i.e. $\nabla \times H = J$. This formulation is only valid in quasi-static situations, i.e. when the size of the physical elements is much smaller than the minimum wave length of interest. The inclusion of the second term was one great *Maxwell* contribution which allowed the study of electromagnetic waves. Equation (F.3) is the local form of the *Faraday* induction law. A temporal variation of the magnetic field generates an electric field. Equation (F.4) represents the local form of the *Gauss* law for electricity. It means that the electric flux out of any closed surface is proportional to the total charge enclosed within the surface. Equation (F.5) is the local form of *Gauss* law for magnetism and means that the net magnetic flux out of any closed surface is zero. This amounts to a statement about the sources of magnetic field: it is not possible to store magnetic charges.

The electric field E can be deduced from two other fields, the vector potential A and the electric potential ϕ by means of the next relation.

$$E = -\frac{\partial A}{\partial t} - \nabla\phi \tag{F.6}$$

Inside a linear conductor, the current density J can be related with the electric field E by

$$J = \sigma E \tag{F.7}$$

σ represents the conductor conductivity. Applying equation (F.6) into equation (F.9) it is possible to relate the two fields introduced with J as

$$J = -\sigma \frac{\partial A}{\partial t} - \sigma \nabla \phi \tag{F.8}$$

F.2 Description of the problem

In this work an algorithm to determine the inductance of an integrated circular spiral inductor is developed. A top view of the inductor is presented in figure F.1. The inductance will be determined by the moment method. This method consists basically in dividing each ring in several finite elements and then determining the magnetic flux caused by each element over the others. The final result is a square matrix with the contribution of one element over all the others. In figure F.2 is shown a vertical projection of the inductor. As a first approach, the inductance will be determined by approximating the spiral inductor to metal concentric rings as in figure F.3.

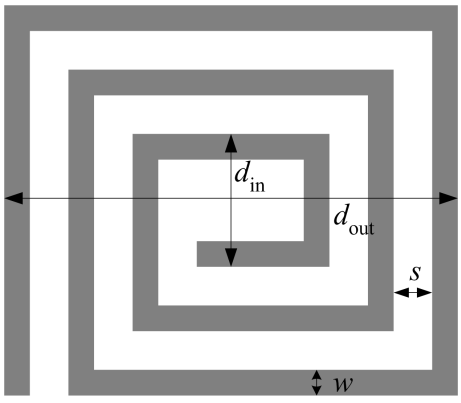

Figure F.1: Spiral square inductor.

In each turn of the inductor, the vector current density is

$$\vec{J} = J\vec{u}_{\varphi} \tag{F.9}$$

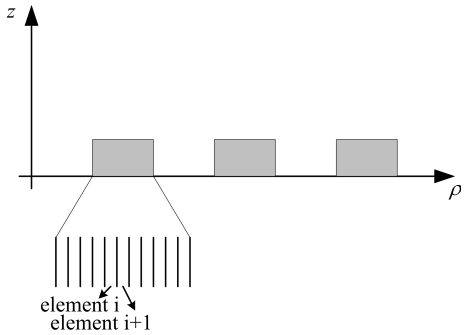

Figure F.2: Vertical plane projection of the concentric inductor.

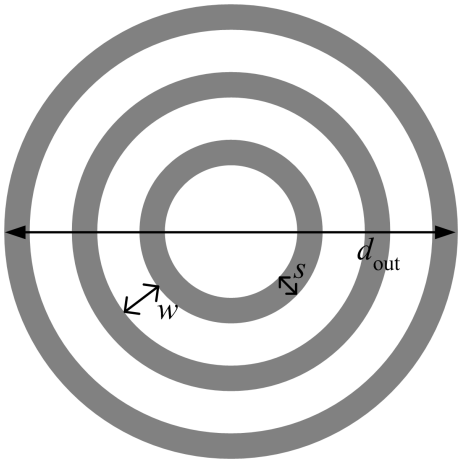

Figure F.3: Concentric ring inductor.

and the vector potential is

$$\vec{A} = A\vec{u}_{\varphi} \tag{F.10}$$

With a constant frequency stimulation, vector J is equal to

$$J = -j\omega\sigma A + J_s \tag{F.11}$$

ω is equal to $2\pi f$, where f is the frequency. σ is the conductivity of the metal and Js is a current inside the conductor due to the source.

From equations (F.8) and (F.11), using the fact that the current has zero divergence inside the conductor and that $\nabla A = 0$, the electrical potential satisfies Laplace's equation inside conductor: $\nabla^2\phi = 0$. With this approximation, it is neglected the inductor capacitance. Therefore, this work is only suitable for determining inductance L and resistance R.

To determine the magnetic flux Ψ related caused by all the elements it is necessary to use a specific Green function to solve the flux integral. The Green function G for concentric wires is

$$Green = \mu G = \frac{1}{2\pi}\int_0^{\pi} \frac{\rho' \cos\varphi}{\sqrt{\rho'^2 + \rho^2 - 2\rho'\rho\cos\varphi + (Z - Z_0)^2}} d\varphi \tag{F.12}$$

The $(Z - Z_0)^2$ component of the Green function above might be neglected in order to simplify the calculation.

The potential vector A is related with the current density J by

$$A = \int_S J\mu G dS \tag{F.13}$$

The magnetic flux Ψ is related with the potential vector A by equation

$$\Psi = 2\pi\rho A \tag{F.14}$$

Gathering equations (F.13) and (F.14) the magnetic flux Ψ relates with the current density J by

$$\Psi = \int_S J\mu(2\pi\rho G) dS \tag{F.15}$$

Relating equations (F.11), (F.14) and (F.15) it is obtained an equation where the only unknown variables are the magnetic flux Ψ and J_s

$$\Psi + j\omega\mu\sigma \int_S \Psi \frac{2\pi\rho G}{2\pi\rho} dS - \int_S J_s 2\pi\rho\mu G dS = 0 \tag{F.16}$$

The expression (F.16) is a complete description of our configuration, where all inductor rings are included.

$$\sum_n -j\omega\mu\sigma \int_{\Delta S_n} \frac{\Psi}{2\pi\rho}\frac{1}{\mu} dS + \sum_n \int_{\Delta S_n} J_s dS = I \tag{F.17}$$

The next step is to divide the global equation (F.16) in smaller equations. In order to do that there are defined N equations that represent the N inductor rings, equation (F.17). Each inductor ring is also divided into smaller elements. These elements determine the accuracy of the calculation: few elements leads to less accuracy, while many elements increase the calculation time. In all those rings it is considered a constant current with value I.

Equation (F.17) can not be computed because Ψ is continuous and unknown. In order to determine it, Ψ is considered constant inside each element, there they assume the value Ψ_n. This approximation is another source of errors.

$$\sum_n -j\left(\frac{\sqrt{2}}{\delta}\right)^2 \frac{\Psi_n}{2\pi\mu}\int_{\Delta S_n}\frac{1}{\rho}dS + \sum_n \frac{K_s}{2\pi}\int_{\Delta S_n}\frac{1}{\rho}dS = I \tag{F.18}$$

Equation (F.18) allows the determination of the flux in a matrix form. To avoid, or reduce, numerical errors during the resolution of Gauss methods, the different sub-matrixes are normalized. Next equations are used for normalization.

$$\rho_{norm} = \frac{\rho}{\alpha}, \alpha = 10^{-6} \tag{F.19}$$

$$\Psi_{norm} = \frac{\Psi}{2\Pi\alpha\mu_0 I} \tag{F.20}$$

$$K_{snorm} = \frac{\alpha K_s}{2\Pi i} \tag{F.21}$$

$$p_{norm} = p\alpha, p = \sqrt{\omega\mu\sigma} \tag{F.22}$$

The matrix form is shown in equation (F.23). Variables are Ψ_n of each element and K_s, both in the normalized form.

$$\left[\begin{array}{c|c} L & H \\ \hline Q & S \end{array}\right]\left(\begin{array}{c} \Psi_{norm} \\ \hline K_{snorm} \end{array}\right) = \left(\begin{array}{c} 0 \\ \hline 1 \end{array}\right) \tag{F.23}$$

where the sub-matrix elements are:

$$L_{i,j} = jp_{norm}^2 \int_{\Delta S_{jn}} g(\rho = \rho_i, \rho' = \rho_j)dS, i \neq j \tag{F.24}$$

$$L_{i,i} = 1 + jp_{norm}^2 \int_{\Delta S_{in}} g(\rho = \rho_i, \rho')dS \tag{F.25}$$

$$H_{i,k} = -\sum_{m_k} \int_{\Delta S_{m_k n}} g(\rho = \rho_i, \rho')dS \tag{F.26}$$

$$Q_{k,j} = -jp_{norm}^2 \int_{\Delta S_{jn}} \frac{1}{\rho_{norm}} dS, if j \in ring_k \tag{F.27}$$

$$Q_{k,j} = 0, if j \notin ring_k \tag{F.28}$$

$$S_{k,k} = \int_{S_{kn}} \frac{1}{\rho_{norm}} dS \tag{F.29}$$

After solving equation (F.23), inductance and resistance are determined respectively with next expressions:

$$L = \frac{1}{2} \sum_n \left(\frac{1}{2} Re(K_s^* \Psi_n) \frac{1}{2\Pi} \int_{S_n} \frac{1}{\rho_n} dS \right) \tag{F.30}$$

$$R = \frac{1}{2} \sum_n \left(\frac{1}{2\Pi} \frac{1}{2\sigma} (-j\omega\sigma\Psi_n + K_s)^2 \int_{S_n} \frac{1}{\rho_n} dS \right) \tag{F.31}$$

F.3 Results

To evaluate the algorithm exposed above some known results are used. From [131], results listed in table F.1 have been used as reference. Results obtained with the presented algorithm are shown on figures F.4 to F.9. Inductance graphics, figures F.4, F.6 and F.8 show a constant value for low frequencies and then a sharp decrease. Quality factor graphics, figures F.5, F.7 and F.9 have a peak at medium frequencies. These behaviors are in accordance with the results of the work used as reference, however they have numerical errors.

Table F.1: Geometrical parameters (N - number of turns, D - diameter, w - width, s - section), inductance at maximum quality factor, L, and maximum quality factor, Q, of three inductors in medium-resistivity factor.

Inductor	N	$D[\mu\text{m}]$	$w[\mu\text{m}]$	$s[\mu\text{m}]$	$L[\text{nH}]$	Q
A	4	240	13.7	10.27	1.93	6.26
B	4	280	11.38	3	5.17	5.90
C	6	320	11.25	3	10.69	4.83

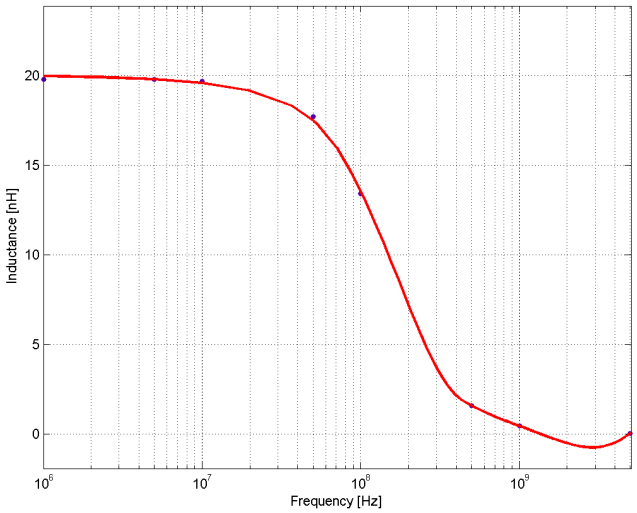

Figure F.4: Inductance A vs frequency.

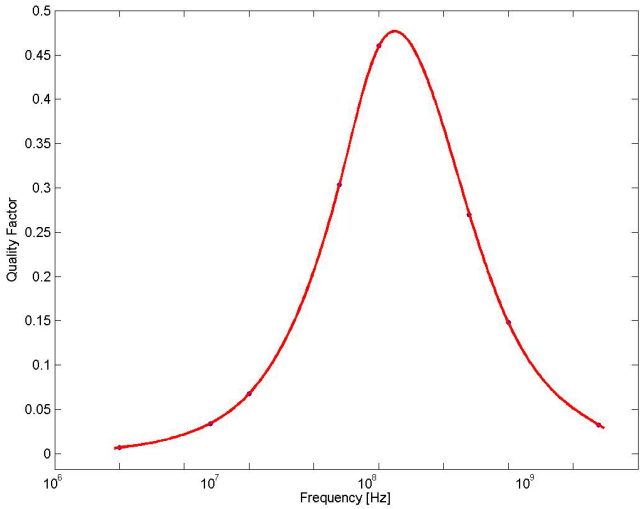

Figure F.5: Quality factor of inductor A.

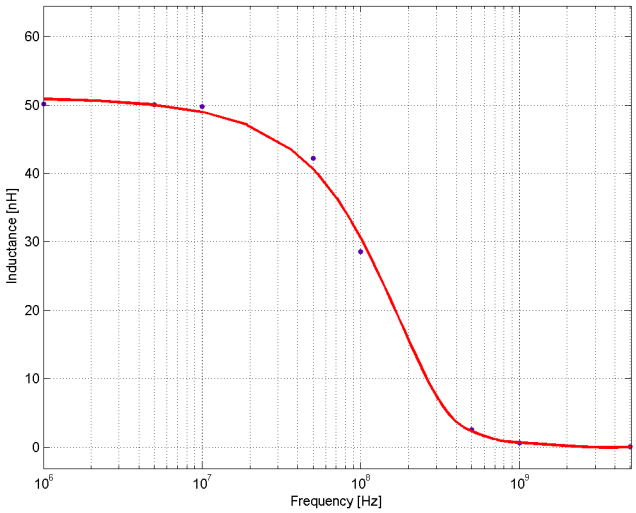

Figure F.6: Inductance B vs frequency.

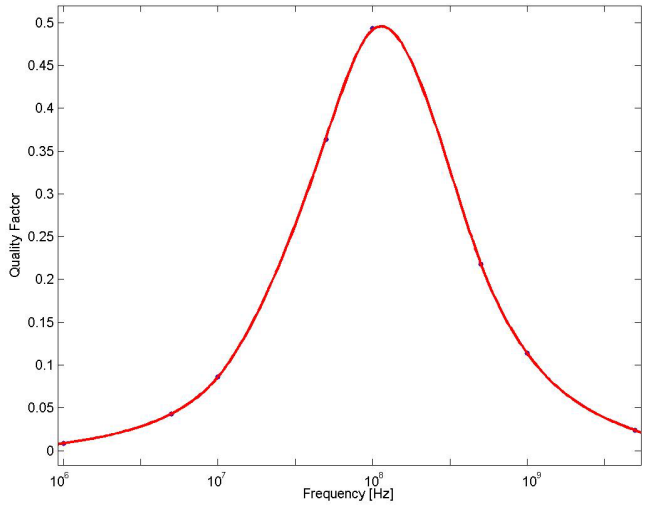

Figure F.7: Quality factor of inductor B.

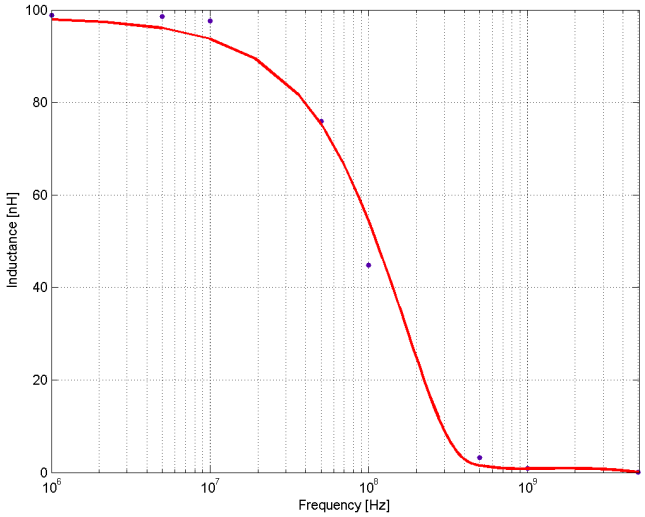

Figure F.8: Inductance C vs frequency.

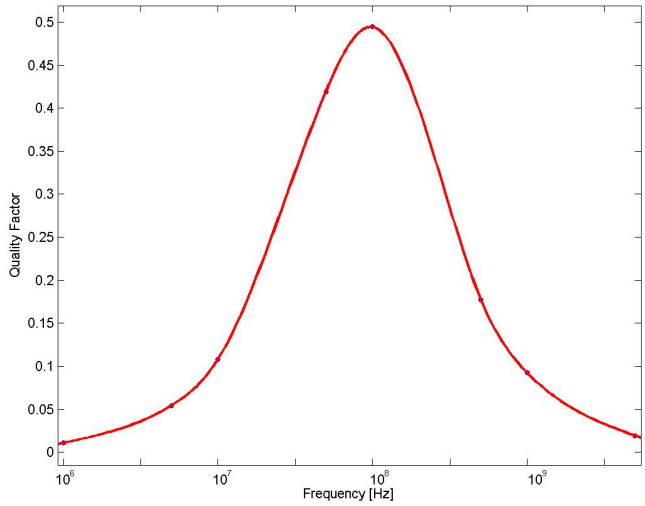

Figure F.9: Quality factor of inductor C.

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