Experimental analysis of CMOS short-channel gate enclosed transistors

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***Abstract*— The outstanding benefits of standard deep submicron CMOS technologies for the design of radiation tolerant devices can be further exploited by means of the use of special layout styles, such as the gate-enclosed transistors. This work constitutes a study of the impact of technology downscaling on the performance of this type of devices, particularly the threshold voltage roll-off due to short-channel effects and the drain-induced barrier lowering. Theoretical predictions have been validated with experimental data in a commercial 0.18μm CMOS process.**

I. Introduction

Irradiation measurements on CMOS devices show a significant decrease of the radiation induced oxide trapped charge for oxides thinner than 10nm, thus minimizing the effect of threshold voltage variation. The reason for this is that as the oxide thickness decreases, and in addition to thermal annealing, tunnelling becomes possible and more effective at neutralizing radiation-induced charge. In fact, in 0.25μm and smaller technologies, radiation induced threshold voltage variation becomes negligible even at very high doses.

Deep submicron processes are therefore attractive for the design of ASIC's for experiments which involve pions, protons and other charged hadrons and neutrons [1], [2], [3]. However, using standard transistors and due to positive charge trapping that accumulates in the oxide bordering the transistor channel, ionizing radiation may induce an inversion layer at the bird's beak or at the shallow trench corner resulting in undesirable effects, among them an increase in the threshold voltage variation. It has been shown that this can be remedied by using enclosed-layout transistors (ELT) characterized by an special layout style having an inner diffusion (drain or source) surrounded by the transistor gate and outer diffusion (source or drain, respectively) [4], [5]. Radiation hardness of ELT devices has been experimentally confirmed by measurements in 0.25μm, 0.18μm and 0.13μm standard CMOS technologies, showing no significant change in threshold voltage up to an absorbed dose of 71kGy(SiO_2), [6], [7].

The first studies on ELT devices focused on the extraction of the effective W/L aspect ratio as a function of physical and geometrical parameters [8], [9]. The first attempt to develop an electrical model for ELTs based on variations of the SPICE and BSIM models for standard transistors was proposed in [10]. Later, a numerical solution in the velocity saturation region was proposed based on a discretized 1-D representation of the voltage along the channel [3]. Important second-order effects such as depletion region non-uniformity, carrier velocity saturation and channel length modulation were also considered in later works [11]. In [12] we proposed an expression for the calculation of the threshold voltage variation due to short-channel effects (SCE) on ELT based on a simplified model of the physics involved, using simulation data to validate the model. In this work, we will show experimental data corresponding to a test chip with ELTs of several topologies fabricated in a commercial 0.18μm CMOS standard process. This data will be used to empirically confirm the model of the threshold voltage variation due to SCE on ELT as well as to study other second-order phenomena such as the drain-induced barrier lowering (DIBL) effect and small-signal parameters.

The paper is organized as follows. In Section II we will briefly summarize the ELT analytical model formulation deriving expressions for the transconductance and drain conductance. Then, in Section III we will take into account short-channel and DIBL effects on the threshold voltage variation. Finally, we will compare our model with experimental results from a 0.18μm chip in Section IV and present the main conclusions of the work.

II. Model formulation

Fig. 1, shows the layout of a square-shaped ELT where s is the contact size, c the contact to gate distance, $a_{p,i}$ the apothem of the inner diffusion, L the channel length, E the extension of the outer diffusion over the gate, W_1, W_2 and W_3 represent the sides of the regular polygons defining the inner diffusion, gate and outer diffusion, respectively, and $\alpha = \pi/n$, where n is the number of sides of the structure.

In a previous work we derived the following expression for the $I-V$ curves of an ELT transistor in the linear region of operation, [13],

$$I_D = \left[\frac{W}{L}\right]_{\text{eff}} \mu_e C_{ox} \left((V_{GS}-V_{TH0})V_{DS} - \frac{V_{DS}^2}{2}\right) - \left[\frac{W}{L}\right]_{\text{eff}} \frac{4\,\mu_e\,C_{ox}\,V_W\,\phi_F}{3} \left(\left(1+\frac{V_{DS}}{2\phi_F}\right)^{3/2} - \left(1+\frac{3V_{DS}}{4\phi_F}\right)\right) \quad (1)$$

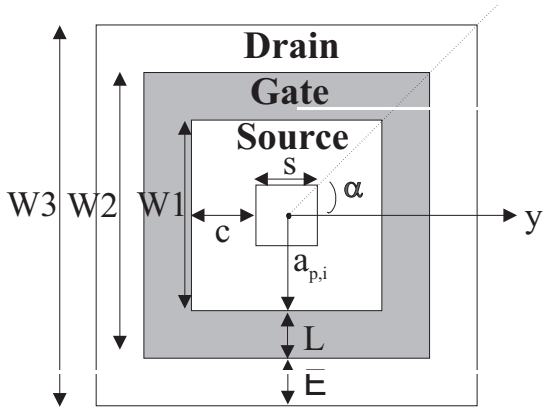

Fig. 1. Schematic layout of an ELT device with $n = 4$

where μ_e is the effective mobility taken as the carrier's average mobility in the inversion layer, C_{ox} the total oxide capacitance per unit area, $V_W = q\,N_A\,x_{dep}/C_{ox}$ being q the electron charge and N_A the doping concentration, ϕ_F the Fermi potential, V_{GS} and V_{DS} are the gate and drain to source voltages, V_{TH0} is the long-channel threshold voltage $V_{TH0} = V_{FB} + 2\,\phi_F + \gamma\sqrt{2\,\phi_F + V_{SB}}$, where V_{FB} is the flat-band potential, γ the body-effect coefficient, V_{SB} the source-to-bulk potential and

$$\left[\frac{W}{L}\right]_{\text{eff}} = 2n\frac{\tan(\pi/n)}{\ln(1 + L/a_{p,i})} \tag{2}$$

is the effective W/L ratio of polygonal ELT, [9].

A. Transconductance

To obtain a meaningful expression of the transconductance, g_m, we express the mobility as, $\mu_e = \mu_0/\left(1 + \left(\frac{V_{GS}-V_{TH0}}{V_{gx}}\right)^2\right)$, where μ_0 is low field mobility term and $V_{gx} = \frac{\epsilon_{Si}}{\eta\,C_{ox}}\sqrt{\frac{K_{sr}}{\mu_0}}$, η is taken as 1/2 and K_{sr} is a constant related with the surface roughness, [14]. Differentiating (1) with respect to V_{GS} we obtain,

$$g_m = \mu_0\,C_{ox}\left[\frac{W}{L}\right]_{\text{eff}} V_{gx}^2\left\{\frac{V_{DS}}{V_{gx}^2 + {V'_{GS}}^2} - \frac{2\,V'_{GS}\,V_{DS}}{\left(V_{gx}^2 + {V'_{GS}}^2\right)^2}\cdot\right.$$
$$\left.\left(V'_{GS} - \frac{V_{DS}}{2} + V_W - \frac{4V_W\,\phi_F}{3\,V_{DS}}\left(\left(1 + \frac{V_{DS}}{2\phi_F}\right)^{3/2} - 1\right)\right)\right\} \tag{3}$$

where we used $V'_{GS} = V_{GS} - V_{TH0}$.

B. Drain conductance

Analogously, differentiating (1) with respect to V_{DS} we obtain the following expression for the drain conductance of an ELT device, g_d,

$$g_d = \mu\,C_{ox}\left[\frac{W}{L}\right]_{\text{eff}}\left(V'_{GS} - V_{DS} - V_W\left(\sqrt{1 + \frac{V_{DS}}{2\,\phi_F}} - 1\right)\right) \tag{4}$$

III. Impact of short-channel effects on ELT devices

Assuming a null bulk-source voltage, $V_{BS} = 0$, and neglecting the non-uniform lateral doping effect, (5) shows the various factors that affect the threshold voltage, V_T, based on the Berkeley Short Channel BSIM4 model, which models the MOS transistor operation in deep submicron technologies,

$$V_T = V_{TH0} + \Delta V_{T,SCE} + \Delta V_{T,DIBL} \tag{5}$$

where $\Delta V_{T,SCE}$ is the short channel effect on V_T and $\Delta V_{T,DIBL}$ is the DIBL effect, [15]. A simple model of the DIBL effect assumes a linear relationship with V_{DS} proportional to the DIBL coefficient, α, [15],

$$\Delta V_{T,DIBL} = \alpha\,V_{DS} \tag{6}$$

With respect to the threshold voltage roll-off due to SCE, $\Delta\,V_{T,SCE}$, it is explained from a qualitative point of view by the fact that a significant amount of the charge on the depletion region is compensated by the charge on the drain and source junctions. Thus, less charge under the gate is needed to achieve inversion and the threshold voltage decreases [15]. Based on this argumentation, we have derived an estimation of the threshold voltage variation due to SCE in ELT transistors that we summarize here for the sake of clarity, [12]. A first-order approximation can be obtained as,

$$\Delta V_{T,SCE} = -\frac{1}{C_{ox}}(Q_{BS} - Q_{BL}) = \frac{Q_{BL}}{C_{ox}}\left(1 - \frac{Q_{BS}}{Q_{BL}}\right) \tag{7}$$

where Q_{BL} and Q_{BS} are the charge densities in the depletion region for long and short channel devices, respectively [16]. Under the assumption of V_{DS} small or zero the depletion region thickness under the gate can be supposed to be constant and equal to x_{dep}. The charge density, on the other hand, can be calculated as, $Q = -qN_A\frac{\Omega_G}{A_G}$, where Ω_G is the volume of the depletion region and A_G the area of the gate. Through elemental geometrical considerations in Fig. 1 we can write, for a long-channel device, $A_{G,LC} = n\,L\,\tan(\pi/n)\,(2a_{p,i} + L)$ and $\Omega_{G,LC} = A_G\,x_{dep}$. Hence, $Q_{BL} = -q\,N_A\,x_{dep}$.

For short-channel ELT, the situation is summarized in Fig. 2 taking as example an ELT device with $n = 4$. The outer and inner diffusions penetrate into the volume under the gate reducing the depletion region. The penetration is supposed to be uniform in all directions and equal to d. Thus, the effective volume under the gate, $\Omega_{G,SC}$ can be calculated as, $\Omega_{G,SC} = \Omega_O - \Omega_I$, where Ω_O is the total volume under the n-sided polygonal shape of side W_2 minus the penetration of the outer diffusion under the gate and Ω_I is the volume under the n-sided polygonal shape of side W_1 plus the penetration of the inner diffusion under the gate (see Fig. 2). We write $\Omega_O = \frac{x_{dep}}{3}\left[A_{upper\_base} + A_{lower\_base} + \sqrt{A_{upper\_base}\,A_{lower\_base}}\right]$ with $A_{upper\_base} = n\,\tan(\pi/n)(a_{p,i} + L)^2$ and $A_{lower\_base} = n\,\tan(\pi/n)(a_{p,i} + L - d)^2$. Analogously, $\Omega_I = n\,\tan(\pi/n)\frac{x_{dep}}{3}\left[3\,a_{p,i}^2 + d^2 + 3\,d\,a_{p,i}\right]$. Thus, the charge density in the depletion region for the short-channel ELT, Q_{BS}, is given by, $Q_{BS} = -q\,N_A\,x_{dep}\left(\frac{L-d}{L}\right)$.

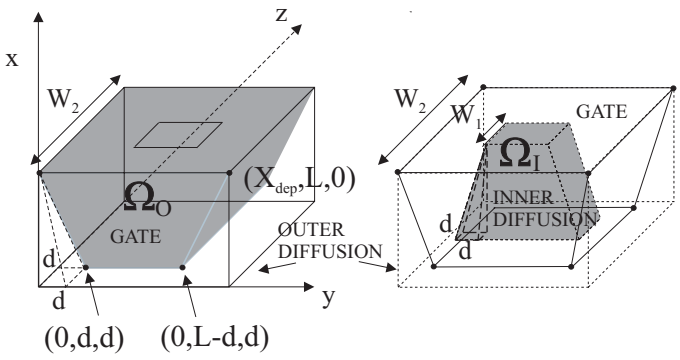

Fig. 2. Lateral penetration under the gate of the outer and inner diffusion regions.

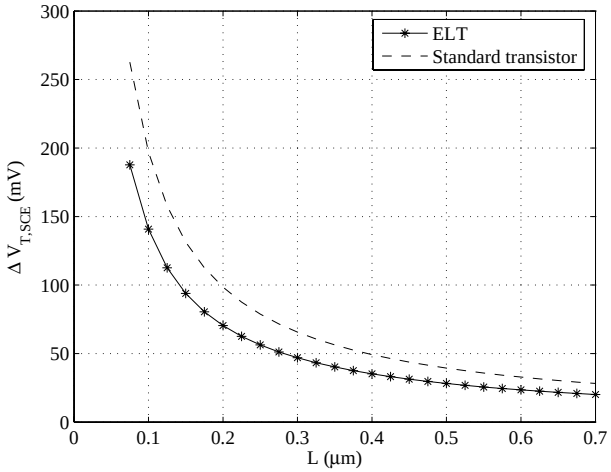

Fig. 3. Modeled $\Delta V_{T,SCE}$ for ELT and standard transistors.

Expressing d as $d = \frac{x_j}{3}\left(\sqrt{1+\frac{6x_{dep}}{x_j}}-1\right)$, where x_j is the junction depth, and substituting in (7) we obtain,

$$\Delta V_{T,SCE}|_{ELT} = \frac{-q\,N_A\,x_{dep}}{C_{ox}}\left(\frac{x_j}{3L}\left(\sqrt{1+\frac{6\,x_{dep}}{x_j}}-1\right)\right) \quad (8)$$

Fig. 3 shows the comparison between (8) and an analogous expression for standard transistors obtained through a similar geometrical analysis for typical values from the MOS BSIM3v3 Hspice model. As seen, our model predicts that ELTs will be less affected by V_T roll-off due to SCE than standard transistors. This is attributed to the fact that the penetration of the inner and outer diffusions have opposite signs and are symmetrical with respect to the center of the device leading to compensation effects. In Section IV the theoretical approach presented here will be compared with measured data using the Shift&Ratio method for the extraction of $\Delta V_{T,SCE}$ from experimental data.

IV. Comparison with experimental data

We fabricated a test chip in a CMOS 0.18μm standard process with ELT devices of different geometries. Fig. 4 shows

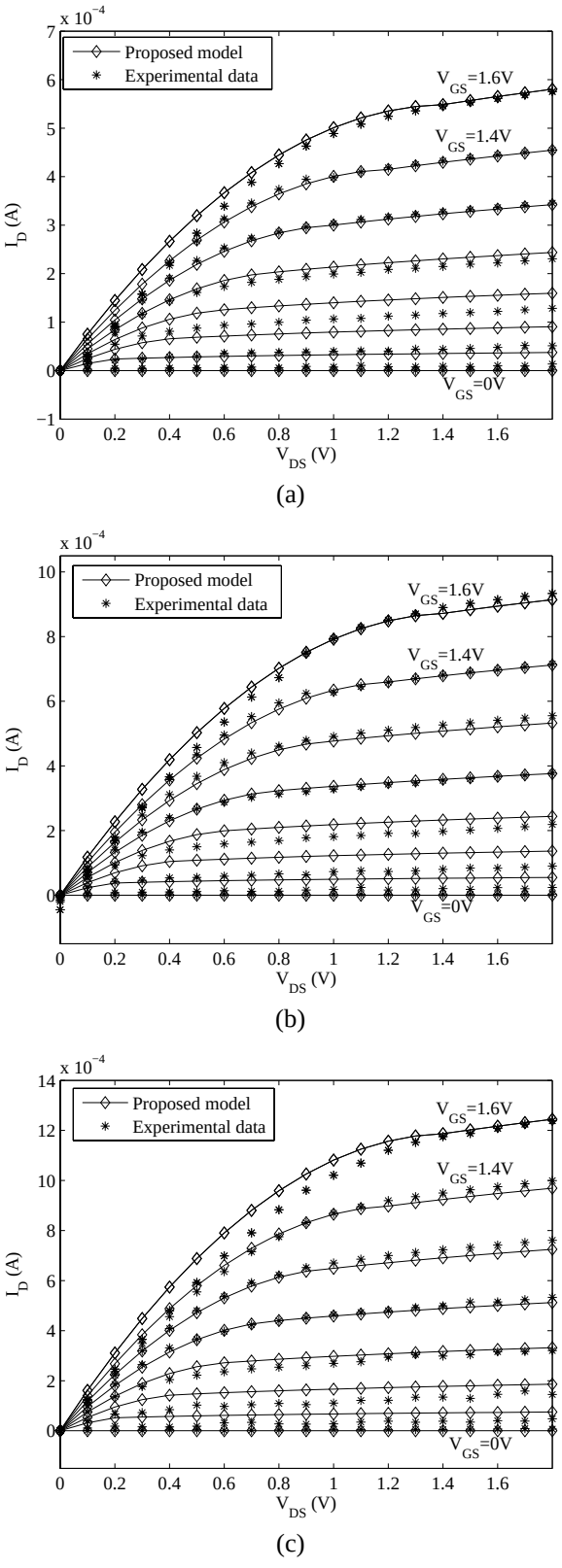

Fig. 4. Comparison of the $I-V$ curves of an ELT device with n=4 and $L = 0.2\mu m$ given by the proposed model with experimental data from a CMOS 0.18μm process with (a) $[W/L]_{\text{eff}} = 15$, (b) $[W/L]_{\text{eff}} = 20$ and (b) $[W/L]_{\text{eff}} = 30$.

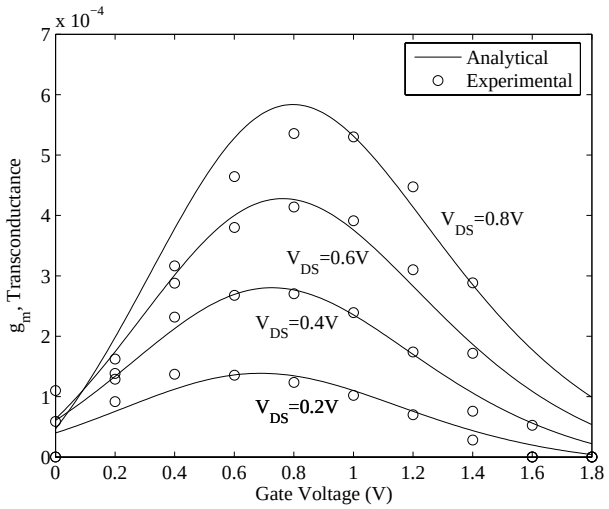

Fig. 5. Comparison of the variation of experimental and theoretical transconductance, g_m, with gate bias for different drain voltages.

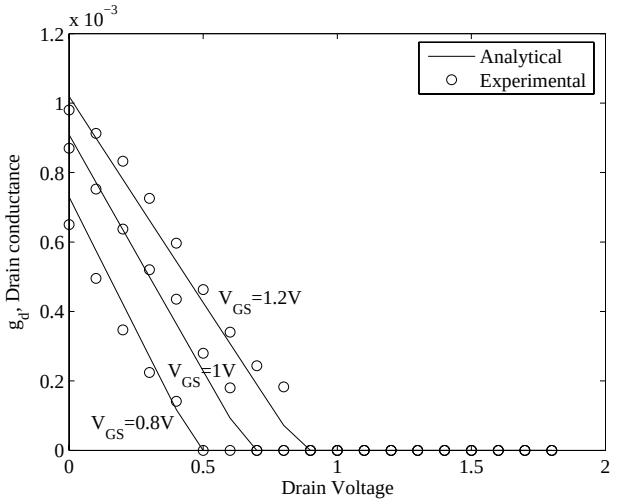

Fig. 6. Comparison of the variation of experimental and theoretical drain conductance, g_d, with drain bias for different gate voltages.

fits of the analytical ELT model presented here to experimental data from short-channel square devices (n=4) with $L = 0.2\mu$m and different $[W/L]_{\text{eff}}$ ratios. In all cases the drain was taken as the inner diffusion. The current in the saturation region has been approximated by the channel length modulation model (CLM) [17]. We used, $I_{DS} = I_{DSAT}/\left(1 - \frac{y_{ld}}{L_{eq}}\right)$, where y_{ld} is the channel length modulation parameter which was estimated making use of simulation results from Sentaurus TCAD and $L_{eq} = L(1 + V_{DSAT}/L\,E_{sat})$. The value of E_{sat} was also obtained from device simulation. As seen in the figures, the model shows close agreement with the experimental data.

With respect to the small-signal parameters, graphs of the transconductance and drain conductance as given by the analytical models in (3) and (4) are shown in Figs. 5 and 6 with a comparison to the experimental values for selected gate and drain voltages for an ELT device with n =4 and $[W/L]_{\text{eff}} = 20$. The small-signal parameters good agreement between experimental and analytical results validates the model.

On the other hand, experimental data corresponding to two different types of ELT devices, with both square and octogonal shapes respectively, and standard-layout transistors for different W/L ratios have been used to study the DIBL effect on the threshold voltage for different drain bias. These results are shown in Fig. 7. As can be seen in the figure, the threshold voltage variation due to DIBL follows a similar pattern regardless of the layout style considered and the dimensions of the device. In all cases, increasing V_{DS} results in an increased $\Delta V_{T,DIBL}$ following a linear relationship as suggested by (6).

Regarding the impact of short-channel effects on the threshold voltage of ELT devices and in order to validate the analytical model proposed in Section III, we measured a set of both long and short channel devices with $L = 10\mu$m and $L = 0.2\mu$m respectively. In all cases, different W/L ratios for

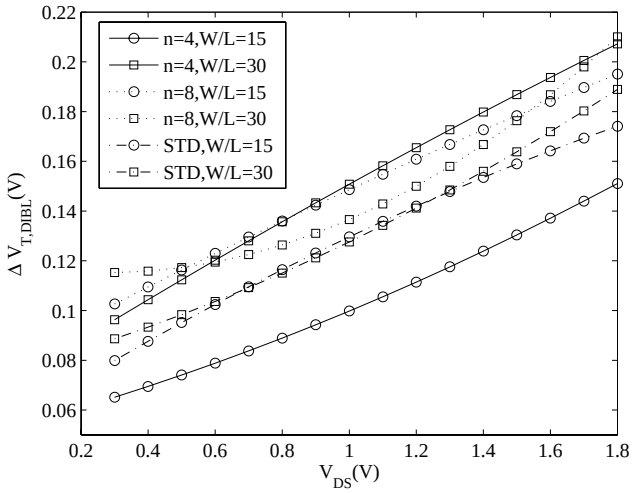

Fig. 7. Experimental threshold voltage variation due to DIBL for different drain bias.

each value of L were considered. A modified shift and ratio method was used to extract the threshold voltage variation due to SCE from experimental data [18]. Applying this procedure to all the transistor types considered in this analysis we obtain the result in Fig. 8. As seen, both types of ELT devices show smaller threshold voltage roll-off at small or moderate W/L ratios, which constitute the scope of applicability of our analysis, as predicted by the theoretical model proposed in this paper (see Fig. 3). However, increasing the W/L ratio while keeping the channel length constant results in similar threshold voltage roll-off values. The reason for this behavior is attributed to the fact that increasing W/L for a constant L increases the asymmetry of the inner and outer diffusions.

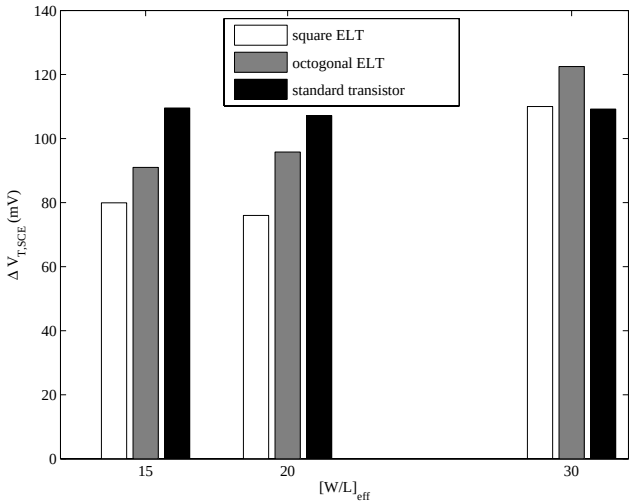

Fig. 8. Experimental threshold voltage variation due to SCE for the different types of transistors considered in the analysis.

V. Conclusions

We have shown an analysis of the impact of technology downscaling on the performance of radiation tolerant ELT devices. Both theoretical predictions and experimental results in a standard 0.18μm process show a smaller threshold voltage roll-off for ELT devices than for their conventional layout counterpart for small or moderate W/L ratios. DIBL effects, however, follow a similar pattern regardless of the layout style or the dimensions of the device.

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