An Analysis and Design Technique to Reduce SET Sensitivity in Combinational Integrated Circuits

Cristiano Lazzari[1,2,3,*], Thiago Assis[1], Fernanda Lima Kastensmidt[1], Gilson Wirth [1], Ricardo Reis[1], Lorena Anghel[3]

[1]*PGMICRO/PPGC - UFRGS*
Porto Alegre, Brazil

[2]*ALGOS - INESC-ID*
Lisbon, Portugal

[3]*TIMA - INPG*
Grenoble - France

E-mails:{clazz,thiago.assis,fglima,wirth,reis}@inf.ufrgs.br, lorena.anghel@imag.fr

Abstract

The proposed technique improves the dependability of circuits under energetic particles by resizing transistors in the most critical paths. First, the SET vulnerability of a mapped circuit is analyzed by identifying the most sensitive nodes when logic and electrical masking is considered. Once the most critical nodes are selected, the transistor sizing algorithm can resize the pull-up and pull-down transistors separately, which allows symmetric and asymmetric transistor resizing. The asymmetric resizing offers more efficient results in terms of area, performance and power consumption.

1. Introduction

In deep submicron technologies, decreasing feature sizes and lower voltage levels cause an increase in the soft error rate (SER) in integrated circuits. When a particle strikes a sensitive region of a semiconductor device with a particular energy, the resulting electron-hole pair generation may change the logical state of the circuit node.

When this temporary current disturbance occurs in a combinational logic circuit, the effect is known as single event transient (SET). SETs may lead a system to an unexpected response whether it propagates to a memory element or a primary output (PO) of a circuit. If a particle directly hits a memory element, the logic value stored may be changed causing the erroneous functioning of the circuit. This changing state in memory elements is known as single event upsets (SEU).

Historically, memories have been concerned for single event upsets. Efficient solutions to memory protection are presented in [1, 2, 3]. However, since the transition time of the logic gates is getting shorter and clock frequencies are significantly increasing in nanometric technologies, errors in combinational logic parts are increasing and error rates will reach the same levels as in memories in the near future.

A recent work predicts SERs in combinational logic circuits comparable to memory elements by 2011 [4]. For this reason, the design of combinational logic tolerant to transient faults is mandatory.

This paper proposes a new transistor sizing method for soft errors protection in combination logic circuits. The main characteristic of the proposed methodology is the ability to find the smallest accepted transistor widths to attenuate SETs in the nodes of a combinational circuit.

Another important point is that pull-up and pull-down transistors are independently sized, minimizing the area overhead and the power consumption. In other words, we apply asymmetric transistor sizing to attenuate SETs with minimized area overhead. Works presented in the literature are based in symmetric models to size pull-up and pull-down blocks.

2. The Transistor Sizing Strategy

The transistor sizing strategy proposed in this paper consists of finding the smallest transistor widths of each circuit gate for SET attenuation.

We consider logical and electrical masking in our sizing strategy. The *logical masking* occurs when a SET provoked by a particle is not propagated to a primary output (PO) due to the logic of the circuit. In other words, the pulse is masked as function of the vector applied in the primary inputs (PI) of the circuit. Controllability and observability techniques are used to define the logical masking of a node.

Controllability in combinational logic circuits denotes the ability to a state be set in a node. Observability is a mea-

*Supported by CNPq and CAPES Brazilian Agencies

sure for how well a state in a internal node can be known at the primary outputs (PO).

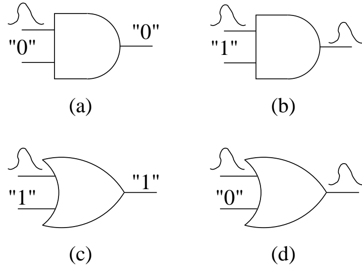

Figure 1. The logical masking.

Figure 1 illustrates the logical masking in a gate. A pulse in one of the gate inputs is propagated through the gate only if a non-controlling value is applied at the other input. Figure 1(a) shows the logical masking in the AND gate as function of the controlling logic value "0" at the input. Otherwise, the logical masking does not happen if a non-controlling value is applied (Figure 1(b)).

In the OR gate, the same situation is considered, where the pulse propagates through the gate only if the non-controlling value is applied at the other input. Figure 1(c) shows the logical masking as function of a controlling value and Figure 1(d) shows the case where there is no logical masking.

Electrical masking can be defined as the electrical attenuation of a pulse in a node by the gates in a path to the point that the SET does not affect the results of the circuit.

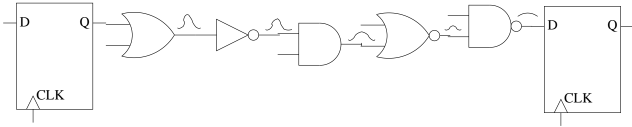

Figure 2. The electrical masking.

Figure 2 shows an example of SET degradation. This degradation is the base to the electrical masking, where the pulse is degraded as function of the electric characteristics of the gates in the path. The pulse can be captured by the memory element if it is not enough degraded. More details about electrical masking and SET propagation are given in Section 3.1.

We consider the logical and electrical masking as the sensitivity of a circuit. The logical masking represents the probability of a transient pulse be masked by the logic function of the circuit, an the electrical masking describe if a transient pulse in a node is not propagated to the POs. Thus, the sensitivity of a circuit is given by

$$S_{circuit} = \sum_{n=1}^{N} (1 - L_n) \cdot (1 - E_n) \tag{1}$$

where L_n is the logical masking and E_n is the electrical masking. The logical masking L_n is a probability value. Larger logical masking means smaller probability of a transient pulse be detected in the circuit outputs. The electrical masking E_n is a binary value where "1" indicates that the transient pulse is totally attenuated and "0" indicates that the transient can be seen in the outputs. Thus, E_n = "1" means sensitivity zero at the node n.

Algorithm 1 The transistor sizing for SET attenuation.

Require: Set of gates G, Set of Nets N, Set of outputs O, Maximum sensitivity M, Max critical charge Q_c, Desired circuit sensitivity $S_{desired}$

Ensure: Set of gates with sized transistors G_{new}

1: $G_{new} \Leftarrow \emptyset$
2: **for all** $n \in N$ **do**
3: $L_n \Leftarrow$ calculateLogicalMasking(n);
4: $E_n \Leftarrow$ calculateElectricalMasking(n, Q_c);
5: $S_n \Leftarrow (1 - L_n) \cdot (1 - E_n)$
6: **end for**
7: $V \Leftarrow O$ {Nets to visit, starting from the outputs.}
8: **while** $V \neq \emptyset$ **do**
9: **for all** $n \in V$ **do**
10: $g \Leftarrow$ getFaninGateConnectedToNet(n);
11: **if** $S_n > M$ **then**
12: $\tau_n \Leftarrow$ getMaximumSET(n, g);
13: $g_{new} \Leftarrow$ sizeTransistors(s, g, τ_n);
14: $G_{new} \Leftarrow G \bigcup \{g_{new}\} \setminus \{g\}$
15: **end if**
16: $I \Leftarrow$ getGateInputs(g);
17: $V \Leftarrow V \bigcup I \setminus \{n\}$
18: **end for**
19: **end while**

The proposed transistor sizing strategy is presented in Algorithm 1. First lines (2-6) define the cicuit sensitivity as shown in (1).

The transistor sizing strategy starts at line 8, where every node n of the circuit is visited in order to find the minimum transistor width to each gate g connected to this node. It is important to note that only nodes with the sensitivity larger than the maximum defined sensitivity M are evaluated (line 11).

Function `getMaximumSET( n, g )` (line 12) finds the maximum pulse duration τ_n in the node n that is suppressed before the primary outputs. The transistor sizing algorithm to a gate g is function of this SET duration τ_n.

Function `sizeTransistors( s, g, τn )` (line 13) continuously increase the transistors width until the SET in the node n be smaller than τ_n. When this situation is reached, we consider the transistors of the gate g are sized as expected to the charge Q_c.

Other lines of the strategy shown in Algorithm 1 give

some idea about the navigation in the nets. The algorithm evaluates every node of the combinational logic, from the primary outputs (PO) to the primary inputs (PI). This is done because the delay of the gates is changed after sizing. When transistors of a gate are sized, the delay usually becomes smaller and a transient pulse propagates with smaller degradation.

Erroneous interpretation concerning the SET propagation must happen if the transient pulse is evaluated before the sizing of the gates in the path to the POs. Thus, when the SET is evaluated in a node n, we guarantee that every gate in the path between this node n and the POs, were already sized.

3. Modeling Single Event Transients

The sensitivity model used in our transistor sizing strategy was proposed in [5]. The model is based on two electrical device parameters. The effective loading capacitance C lumped onto the output node of a gate g and the effective resistance R of the "ON" transistors of this gate.

The model derivation has a strong relation with the electrical devices behavior and allows the evaluation of the critical charge Q_c needed to induce a SET in a node, and the transient pulse duration, as well.

The charge deposition mechanism of a SET is modeled by the double exponential function proposed in [6]. The SET behavior is modeled as the follows.

$$I(t) = I_0(e^{-t/\tau_\alpha} - e^{-t/\tau_\beta}) \tag{2}$$

where I_0 is defined as $Q_c/(\tau_\alpha - \tau_\beta)$, τ_α is collection time constant of the junction, and τ_β is ion-track establishment time constant. Q_c is the charge of a particle while τ_α and τ_β are constants that depend on several process-related factors. In this work, τ_α and τ_β were defined as 1.06×10^{-9} and 5×10^{-11}, respectively [7].

Important characteristics about the transient pulse can be obtained by (2). Models presented in [5] are derivations of the double exponential to obtain the peak time t_{peak} and the voltage peak V_{peak}.

$$t_{peak} = \frac{ln\left(\frac{\tau_\alpha}{RC}\right)\tau_\alpha RC}{\tau_\alpha - RC} \tag{3}$$

$$V_{peak} = \frac{I_0\tau_\alpha R}{\tau_\alpha - RC}\left(\left(\frac{\tau_\alpha}{RC}\right)^{\frac{RC}{RC-\tau_\alpha}} - \left(\frac{\tau_\alpha}{RC}\right)^{\frac{\tau_\alpha}{RC-\tau_\alpha}}\right) \tag{4}$$

where R is the effective resistance of the pull-up path (if PMOS transistors are "ON") or the effective resistance of the pull-down path (if NMOS transistors are "ON") and C is the effective capacitance loading lumped onto the output node.

The critical charge Q_c can be derived by (4) once the V_{peak} of a transient pulse is known. Thus, the critical charge Q_c is given by

$$Q_c = \frac{V_{peak}(\tau_\alpha - RC)}{R\left(\left(\frac{\tau_\alpha}{RC}\right)^{\frac{RC}{RC-\tau_\alpha}} - \left(\frac{\tau_\alpha}{RC}\right)^{\frac{\tau_\alpha}{RC-\tau_\alpha}}\right)} \tag{5}$$

The voltage at the struck node shows a double exponential behavior in which the transient voltage V_{peak} is reached at time t_{peak}. The voltage starts to decrease exponentially after t_{peak}.

$$\tau_n = t_{peak} - RCln\left(\frac{\frac{1}{2}VDD}{V_{peak}}\right) - \tau_\alpha ln\left(\frac{\frac{1}{2}VDD}{V_{peak}}\right) \tag{6}$$

The transient pulse duration τ_n is shown in (6), where the second term corresponds to the analytical solution if RC time is much greater than τ_α and the last term corresponds to the analytical solution if τ_α time is much greater than RC.

3.1. Single Event Transient Propagation

The analysis of the transient pulse propagation shows that pulse degradation is directly influenced by the propagation delay τ_g. In other words, larger τ_g leads to greater degradation of the transient pulse.

We consider the SET was electrically masked whether a pulse is complete degraded before the primary outputs.

Wirth *et al* proposed a pulse degradation model based on curve fitting [8]. The model considers a k parameter equals to the minimum ratio τ_n/τ_g needed to propagate a SET to the next stage in a circuit path. This model is the basis to the sizing algorithm because of its propagation properties. These properties can be useful also to obtain the maximum acceptable transient pulse duration in a node.

4. Results

Table 1 shows the results obtained by the proposed transistor sizing strategy. Results include a comparison between a symmetric and asymmetric sizing methodologies using a $180nm$ technology process [9]. The transient pulse propagation parameter k was defined by hspice simulations as 0.8 for this technology. The transistor sizing was done aiming at reducing the sensitivity to 50% sensitivity and 0%.

A study presented in [10] shows that the charge of very few particles is higher than $0.3pC$ at ground level. We use this value in our experiments by considering as the worst case deposited charge.

The first important point shown by these results is the small overhead presented by the proposed methodology.

Table 1. The proposed transistor sizing to single event transient attenuation. Results show the area, timing and average power overhead for symmetric and asymmetric sizing techniques for particles with charge $Q = 0.3pC$.

Combinational Circuit	Number of Gates	Sensitivity $S_{circuit}$	Symmetric Sizing			Asymmetric Sizing		
			Area (%)	Power (%)	Timing (%)	Area (%)	Power (%)	Timing (%)
C432	227	50%	47.4	63.8	0.0	35.5	50.7	2.0
		0%	69.8	105	1.2	50	59.7	0.0
C880	365	50%	88.0	72.4	0.0	69.2	51.6	0.0
		0%	115.3	88.7	12.3	86.9	59.1	13.2
C1355	464	50%	62.4	38.6	16.0	50.6	29.5	15.8
		0%	80.0	61.6	24.8	58.6	37.2	17.1
C1908	423	50%	47.0	35.5	12.0	37.0	29.0	8.8
		0%	69.2	20.89	13.0	49.2	17.4	10.16
Average overhead		50%	61.2	52.7	7.0	48.0	40.2	6.65
		0%	83.5	69.0	12.82	61.1	43.3	10.11

The worst case was a 87% area overhead for complete protection against particles with charge $Q = 0.3pC$. Results show an average 83% area overhead for the symmetric sizing and 61% for the asymmetric sizing. Power consumption presents 70% average overhead for the symmetric sizing against 43% for the asymmetric. Results shown small timing penalties of 10% for the circuit with 0% sensitivity.

The asymmetric transistor sizing resulted in smaller area, power consumption and timing in comparison with the symmetric sizing. Despite the penalties when designing radiation hardened circuits, results shown the asymmetric sizing efficiency.

5. Conclusions

This paper presents a new transistor sizing algorithm aiming at protecting combinational logic circuit to single event transients. The transistor sizing strategy is based on logical and electrical masking in order to independently size pull-up and pull-down transistors.

The technique consists on sizing only transistors directly related to the SET attenuation. Besides, the model takes into account propagation characteristics in which the degradation of the transient pulse is considered.

Results show small area, timing and power consumption overhead in comparison with a symmetrical methodology. The reduced timing penalties presented by the sizing methodology allows the development of high frequency circuits.

References

[1] T. Calin, M. Nicolaidis, and R. Velazco. Upset hardened memory design for submicron cmos technology. *IEEE Transactions on Nuclear Science*, 43:2874–2878, December 1996.

[2] L. Rockett. An seu hardened cmos data latch design. *IEEE Transaction on Nuclear Science*, NS-35(6):1682–1687, Dec 1988.

[3] S. Whitaker, J. Canaris, and K. Liu. Seu hardened memory cells for a ccsds reed solomon encoder. *IEEE Transaction on Nuclear Science*, NS-36(6):1471–1477, December 1991.

[4] P. Shivakumar, M. Kistler, S. W. Keckler, D. Burger, and L. Alvisi. Modeling the effect of technology trends on the soft error rate of combinational logic. In *DSN '02: Proceedings of the 2002 International Conference on Dependable Systems and Networks*, pages 389–398, Washington, DC, USA, 2002. IEEE Computer Society.

[5] G. Wirth, M. Vieira, and F. L. Kastensmidt. Accurate and computer efficient modelling of single event transients in cmos circuits. *IET Circuits, Devices & Systems*, 1:137–142, April 2007.

[6] G. Messenger. Collection of charge on junction nodes from ion tracks. In *Proceedings of the IEEE Transactions on Nuclear Science*, pages 2024–2031, 1982.

[7] A. Dharchoudhury, S. M. Kang, H. Cha, and J. H. Patel. Fast timing simulation of transient faults in digital circuits. In *ICCAD '94: Proceedings of the 1994 IEEE/ACM international conference on Computer-aided design*, pages 719–722, Los Alamitos, CA, USA, 1994. IEEE Computer Society Press.

[8] G. Wirth, M. Vieira, E. H. Neto, and F. L. Kastensmidt. Modelling the sensivity of cmos circuits to radiation induced single event transients. *Microelectonics Reliability*, 47(3), March 2007.

[9] ASU. Predictive technology model. nanoscale integration and modeling (nimo) group. Available in http://www.eas.asu.edu/∼ptm/, 2007.

[10] Q. Zhou and K. Mohanram. Gate sizing to radiation harden combinational logic. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 25:155– 166, Jan 2006.