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# A Case Study on Phase-Locked Loop Automatic Layout Generation and Transient Fault Injection Analysis

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**Abstract** This paper reports a case study on the automatic layout generation and transient fault injection analysis of a Phase-Locked Loop (PLL). A script methodology was used to generate the layout based on transistor level specifications. Experiences were performed in the PLL in order to evaluate the sensibility against transient faults. The circuit was generated using the STMicroelectronics HCMOS8D process (0.18 $\mu$m). Results reveal the PLL sensitive points allowing the study and development of techniques to protect this circuit against transient faults.

**Keywords** Phase-locked loop · Automatic layout generation · Transient fault injection

## 1 Introduction

The development of radiation-hard Phase-Locked Loops (PLLs) has been presented in many research works. These structures are used in radiation environments, such as nuclear reactors, nuclear weapons, large accelerators and clearly satellites or space shuttles where a large variety of high-energy particles can be found with energies from *keV* to *GeV* [5].

Previous research in radiation-hard PLLs are presented in Toifl and Moreira [9], Lyons et al. [4] and Pan et al. [7]. These works were performed at transistor or mask layout level. In all cases, automatic methods for structure generation were not used and hardening techniques were manually applied in the PLL. It means that PLL structures were analyzed and hardening techniques were manually inserted according the functionality of each block.

The goal of this work was to develop a technology independent layout generation methodology based on transistor level specifications and to analyze the PLL behavior under transient faults effects. Transient fault injection analysis allows to identify critical points of the PLL and to define methods to protect the PLL against this kind of faults. These results can be used in future works to automatically generate a radiation-hard PLL.

This paper is organized as follows. In Section 2 is described the PLL functionality. In Section 3 is reported the methodology used to generate the PLL layout and Section 4 presented details about the layout generation. The PLL validation is shown in Section 5. Transient fault injection experiences are shown in Section 6 and Section 7.

## 2 PLL Functionality

Phase-Locked Loop (PLL) is basically a closed loop frequency control system, whose functionality is based

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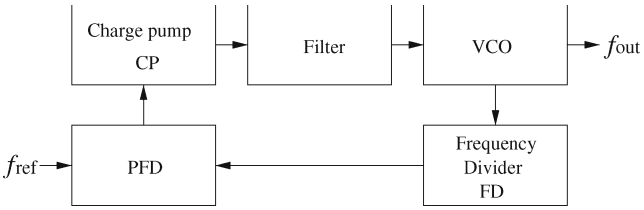



**Fig. 1** PLL block diagram

on the sensitive detection of the phase difference between its input and the signal coming from the voltage-controlled oscillator (VCO) module. PLLs are commonly used as frequency multipliers. Many digital signal processors (DSPs) and high performance microcontrollers use PLLs as its internal clock generation circuits [7].

The PLL block diagram is shown in Fig. 1. It is composed by five blocks where each block has a well defined function in the PLL operation. It consists in a phase-frequency detector (PFD), a charge-pump (CP), a filter, a VCO and a frequency divider (FD).

The function of the PFD is to detect phase and frequency differences between the reference clock $f_{ref}$ and the signal coming from the frequency divider (FD). The CP injects a current into the filter according to signals coming from the PFD. Based on the value of these signals, the charge pump injects or extract current into and from the loop filter. The filter is located between the CP and the VCO and it is used to ensure the performance control and to attenuate undesirable characteristics of the PFD signals. The VCO is basically a ring oscillator aiming at generating an output frequency based on the voltage applied to its input. The goal of the FD in the PLL is to divide the VCO frequency $f_{out}$. The PLL loop will ensure that the FD output frequency is identical to the $f_{ref}$.

The output frequency of a PLL is given by

$$f_{out} = N \times f_{ref} \tag{1}$$

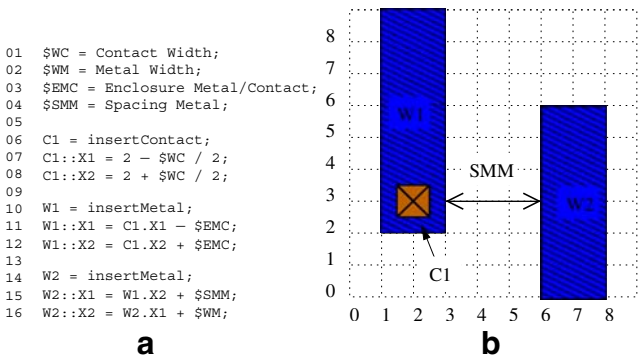



**Fig. 2** Example of the script-based methodology. **a** Short description. **b** Layout

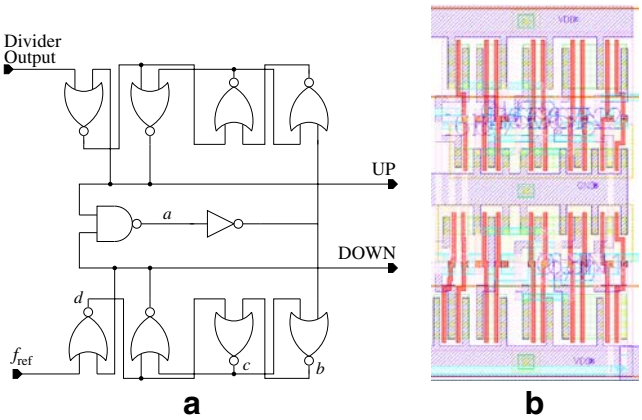



**Fig. 3** Phase-frequency detector (PFD). **a** PFD gate level schematic. **b** PFD layout

where $N$ is the division factor of the frequency divider and $f_{ref}$ is the input reference frequency.

## 3 The Script-Based Layout Generation Methodology

The layout generation method used in this work is a script-based methodology, in which layout elements (layout polygons) are generated according to predefined functions. These functions are basically used to generate transistors, wires, body ties and other elementary structures. Thus, a set of functions are available in which allows the designer to write the script.

Figure 2 illustrates the script-based methodology. In this figure, variables `$WC`, `$WM`, `$EMC` and `$SMM` are the technology values from the contact width, metal width, metal enclosure on contacts and spacing between metal layers, respectively. Functions `insertContact` and `insertMetal` are used to insert rectangles in the layout.

Rectangles can be seen as the following structure,

```
struct rectangle {
  var X1, X2; // Horizontal coordinates
  var Y1, Y2; // Vertical coordinates
}
```

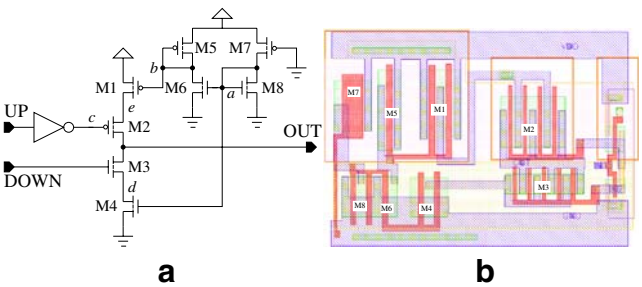



**Fig. 4** Charge-pump (CP). **a** Transistor level schematic. **b** Layout

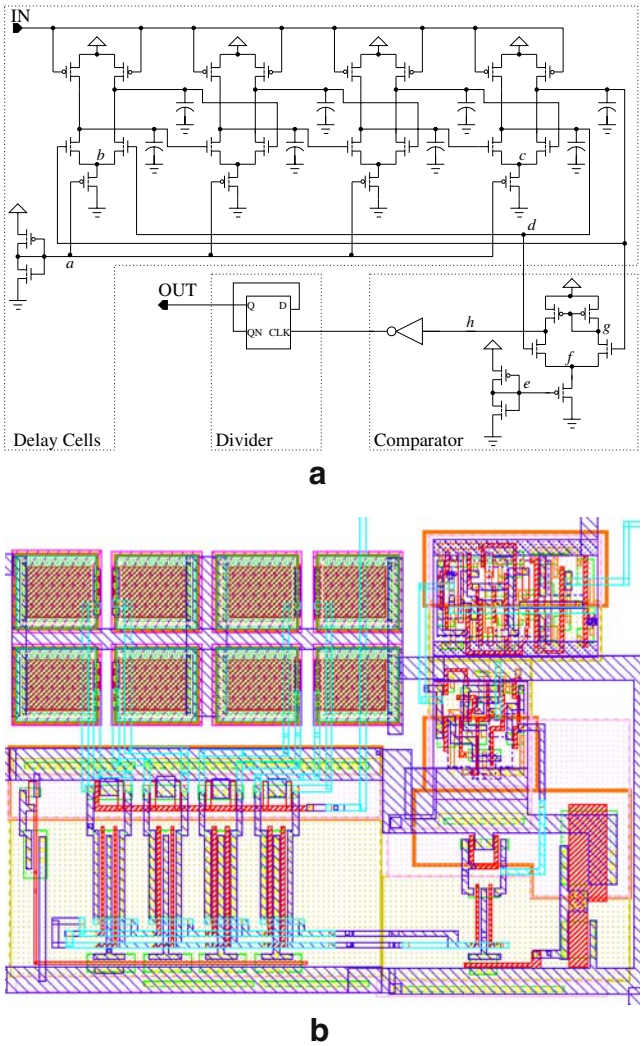



**Fig. 5** Voltage-Controlled Oscillator (VCO). **a** VCO schematic. **b** VCO layout

where `X1` and `X2` are horizontal coordinates and `Y1` and `Y2` are vertical coordinates, `[X1,Y1]` are the coordinates to the most left/bottom point and `[X2,Y2]` represents the most right/top point of the rectangle. For example, lines 07-08 in Fig. 2a define a rectangle that represents the contact $C1$, lines 11–12 and 15–16 are the coordinates of the metal wires $W1$ and $W2$. Only horizontal coordinates are represented in this example, but vertical coordinates and constraints are defined as well using the same idea. Any other function can be developed to help generating layout patterns according to the transistor level implementation of a proposed circuit.

## 4 PLL Layout Generation

The layout implementation was done based on the work proposed in Ammari [1]. The PLL was designed

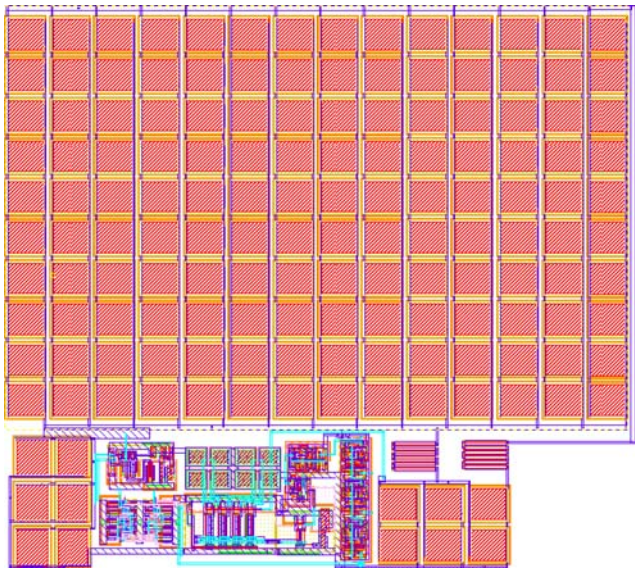


**Fig. 6** The whole PLL layout

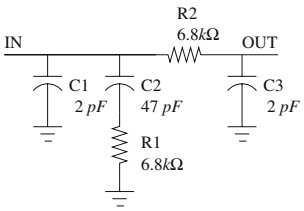
and validated at transistor level in the ST 0.18 $\mu$m (HCMOS8D) technology. The PLL $f_{out}$ is 200 MHz for a $f_{ref}$ of 25 MHz for the proposed PLL architecture. The validation includes LVS (layout versus schematic) and electric simulation.

The layout of every module was separately generated as follows:

1. The filter was implemented by using capacitors provided by the ST foundry,
2. Frequency Divider (FD) is composed by 3 D-flipflops. Flipflops from the standard cell library were used,
3. Phase-Frequency Detector (PFD) is a block composed by 10 digital gates (8 NORs, 1 NAND and 1 INV). Parrot Punch Tool [3] was used to generate the layout,
4. Charge-pump (CP) and Voltage-Controlled Oscillator (VCO) circuits being analog blocks were generated by using the script-based methodology presented in Section 3,
5. All the blocks were manually connected.

In the following we present the layout implementation of the different components of the PLL.

**Fig. 7** Filter schematic



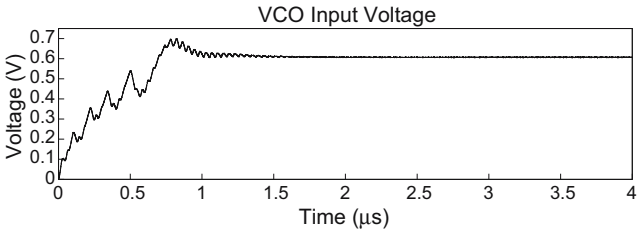



**Fig. 8** VCO input voltage

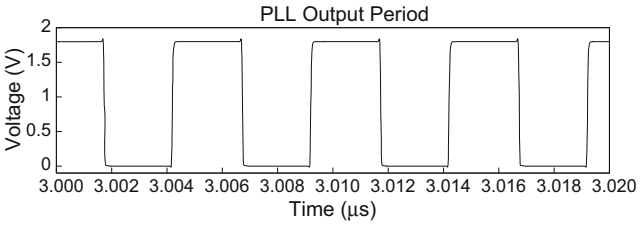



**Fig. 10** PLL Output Signal

The PFD structure is illustrated Fig. 3. This block is a pure digital element and it was generated by the Parrot Punch tool [3]. Parrot Punch was used for PFD generation due to the simplicity of this circuit. Parrot Punch is able to generate static logic CMOS layouts based on a transistor net-list. The PFD element contains only 10 gates and the used tool can deal very well with this complexity.

The charge pump (CP) is shown in Fig. 4. It consists of an 8-transistor structure aiming at feeding a voltage level to the VCO in order to control the PLL output frequency ( $f_{out}$). It is important to highlight that the loop filter should be able to attenuate undesirable characteristics of the signal that feeds the VCO in order to ensure the desired output frequency. This layout was generated using the script-based methodology (Section 3).

Based on the characteristics extracted from the transistor level schematic (Fig. 4), technology rules, transistor sizes and the number of fingers of each transistor, the layout script description was manually generated. The advantage of using a script based methodology as opposed to *manually* generated the layout is that layout modifications can be easily applied to the layout. In manually generated layouts, modifications in the transistors characteristics usually imply hard working to implement again the layout.

The VCO is used to generate a frequency signal as function of a voltage applied in its input. The schematic of the VCO is shown in Fig. 5 and it is divided in three parts: *Delays Cells*, *Comparator* and *Divider*. The delay cells and the comparator were generated using the script-based methodology. The divider was inserted in the VCO layout by using a standard cell D-flipflop of the ST 0.18 $\mu$m library.

The PLL layout is shown in Fig. 6. As can be easily seen, the filter takes the largest part of the layout area due to the large capacitors values need to implement the filter.

The filter is a third order filter as shown in Fig. 7. These capacitance and resistance values explain the important area occupied by the filter in the PLL, where more than 90% of the PLL total area is occupied by the filter.

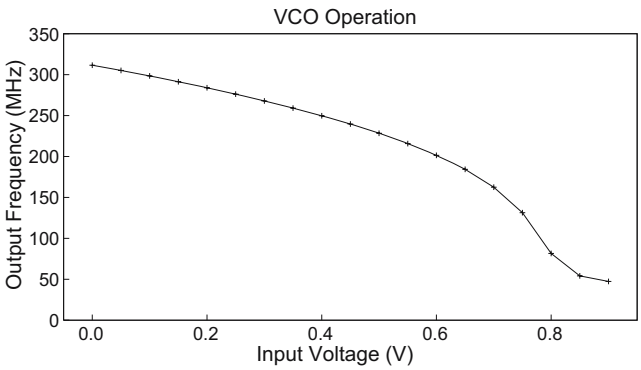



**Fig. 9** VCO characteristics

## 5 PLL Layout Simulation Results

The PLL layout and simulation were done in the Cadence Virtuoso and Cadence Spectre, respectively [2].

The VCO input voltage is shown in Fig. 8 where the behavior of the VCO input voltage is function of the execution time. The picture display the behavior of the VCO control voltage during lock acquisition (fist 2.5 $\mu$s) and phase tracking (beyond 2.5 $\mu$s).

The VCO characteristics are presented in Fig. 9. This figure represents the output frequency $f_{out}$ as function of the voltage applied in the VCO input. The curve shows the reduction of the frequency according to the

**Table 1** Fault injection points and transient fault sensitivity analysis in the PLL

| Block | # Total points | # Injection points | % failure | Schematic |
|---|---|---|---|---|
| PFD | 10 | 5 | 80 | Fig. 3 |
| CP | 5 | 5 | 60 | Fig. 4 |
| Filter | 3 | 3 | 100 | Fig. 7 |
| VCO | | | | |
| Delay Cells | 13 | 4 | 100 | Fig. 5 |
| Comparator | 5 | 4 | 50 | |
| Divider | 9 | 4 | 90 | |
| FD | 27 | 12 | 90 | N/A |
| Total | 72 | 37 | | |

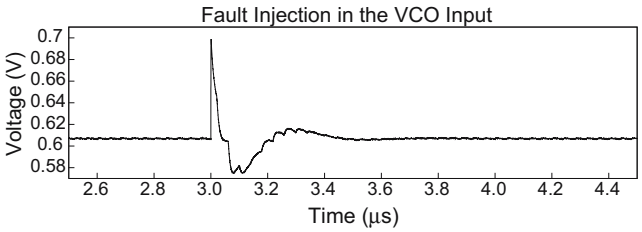



**Fig. 11** Fault injection in the VCO input

increasing of the input voltage. The range of VCO input signal is between 0 V and 0.9 V. Input voltages larger than 0.9 V lead to an constant output voltage equal to $V_{DD}$ and the output frequency is equal 0 (ZERO).

Figure 10 shows the output signal where a frequency $f_{out}$ of 200 MHz (5 ns of period) is obtained. This frequency is the same as the specifications presented in Ammari [1]. As shown in Fig. 9, an input voltage of ~0.600 V is enough to obtain the frequency required by this project.

## 6 The Transient Fault Injection Methodology

The device-level fault model presented in Messenger [6] is used to estimate the effects of single events in the developed cells. In this work, transient faults are modeled by the double exponential current representing the pulse disturbing the node.

$$I(t) = \frac{Q}{\tau_1 - \tau_2}\left(e^{-t/\tau_1} - e^{-t/\tau_2}\right) \quad (2)$$

In Eq. 2, $Q$ is the injected charge and may be positive or negative. $\tau_1$ is the collection time constant of the junction and $\tau_2$ is the time constant for initially establishing the ion track. $\tau_1$ and $\tau_2$ are constants and depend on several process-dependent factors.

In this work, the values for $\tau_1$ and $\tau_2$ were $2 \times 10^{-10}$ and $5 \times 10^{-11}$, respectively [8].

## 7 Fault Injection Results

As reported in Section 2, the PLL is divided in five blocks: *PFD*, *CP*, *filter*, *VCO* and *FD*. Fault injection points on these blocks were analyzed and they are classified as described in Table 1.

Due to the long simulation times and the huge number of injection points that need to be considered, points leading to similar erroneous behavior were discarded. For example, the first part of the VCO is composed by four delay cells (See Fig. 5), but fault injections were performed only in the first and the last delay cell. Thus, analyzing similarities between points

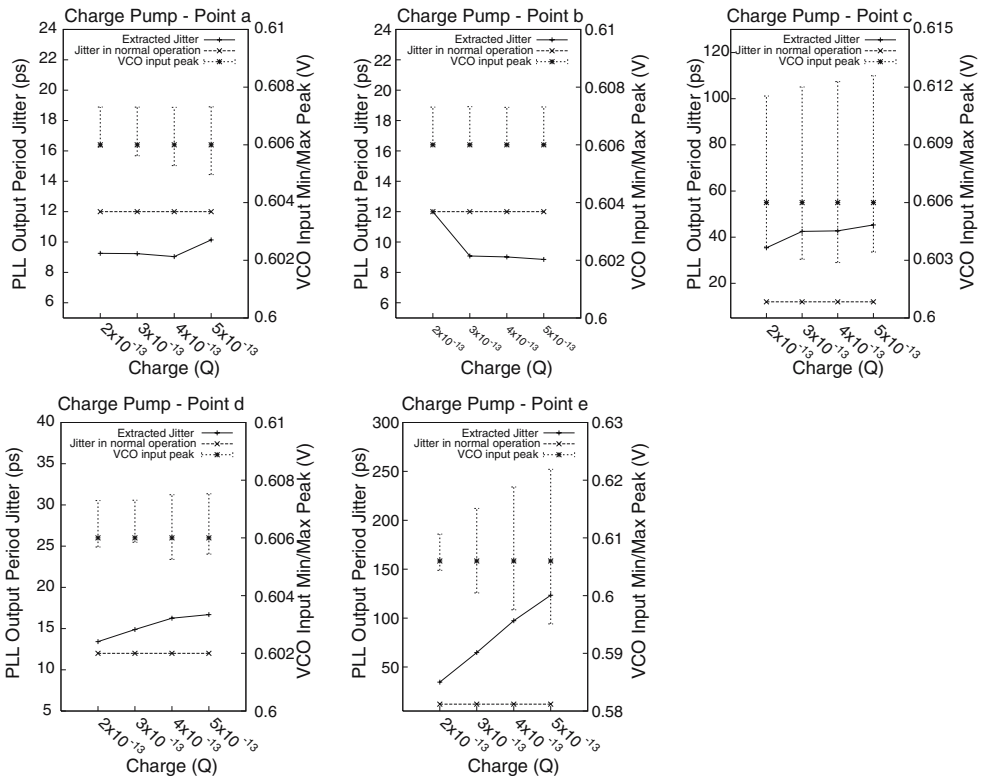



**Fig. 12** PLL jitter and VCO voltage peak due to transient fault injection in the charge pump (CP)

in the PLL, some points were identified and selected to perform the fault injection experiences.

In Table 1, sensitivity analysis is shown in which the number of points (#*Total Points*) represents every node in the PLL. All these nodes are candidates to fault injection. According similarities between the nodes, some of them were selected. # *Injection Points* shows the number of different points were selected to the fault injection.

The sensitivity of each block is shown in column % *Failure* where most part of the PLL elements presented high degree of failure. This failure rate were obtained by fault injection. The whole process were automated by scripts. The blocks with smallest sensibility were the VCO comparator and the Charge Pump.

Four values of the charge $Q$ were injected to each point for the layout: $0.2pC$, $0.3pC$, $0.4pC$ and $0.5pC$. Fault injections were performed during simulation time. Fault injection effects were analyzed according to the following criterion:

- Verification of the effects at the injection points;
- Analyze of changes in the VCO input voltage;
- Detection of differences in the PLL output frequency (Period Jitter).

The PLL operation is stable when no faults are injected, with a frequency range between 199.512 MHz and 200.378 MHz. It is considered that transient fault affects the PLL functionality when the frequency is out of this range. According the obtained clock period in normal condition, it is considered as an erroneous operation when the period jitter is larger than $12ps$ due to a fault injection. The jitter is used due to the possibility to measure small variances in the clock period.

In the transient fault injection experiences, the PLL period variation and the effect of the injection in the VCO input were analyzed. The jitter is discussed only when a small variation in the PLL period was detected.

In the following, transient fault injection in the main elements of the PLL is discussed.

In order to illustrate the effects of a transient fault, the Fig. 11 shows a fault injection in the VCO input. This figure presents the general behavior of the VCO input voltage in which there is a voltage peak of $0.7V$ when the fault is injected at $3\mu$s with a charge $Q = 0.5pC$. After that, the PLL attempts to stabilize the VCO input and the output frequency $f_{out}$, as consequence. It is considered that the PLL is stable $1\mu$s after the transient fault injection.

Figure 12 presents the transient fault injection in the five internal points of the charge pump (CP). These internal points are represented as *a*, *b*, *c*, *d*, and *e* in Fig. 4a. These values show three important results to each fault injection experience ($Q$=0.2$pC$, $Q$=0.3$pC$, $Q$=0.4$pC$ and $Q$=0.5$pC$) in every point. They are the biggest extracted jitter after the fault injection, the jitter value in normal operation mode (on the left side) and the voltage variation in the VCO input (on the right side).

Results show that transient faults in points *a* and *b* do not result in problems to the PLL functionality. The period jitter in these cases is always lower than the value in the normal operation (between $8ps$ and $12ps$), due to the small variation in the VCO input signal.

However, transient fault injection in points *c*, *d*, and *e* of the charge pump result in variations of the PLL output frequency. To every charge $Q$ used in the injections, the PLL output period jitter is higher than the acceptable value defined by the design specifications. In the point *e* with Q=0.5$pC$ for example, the resulting jitter arrives to $123ps$, being 10 times the jitter specified.

Figure 13 presents the effects of the transient fault injection in the three nodes of the filter and in the FD output. On the left side of the graphics is represented minimum and maximum values to the PLL output period ($1/f_{out}$) after the fault injection and on the right side is shown the voltage variation of the VCO input.

Based on these results, we can see that the PLL output period is outside of the range in all cases. The

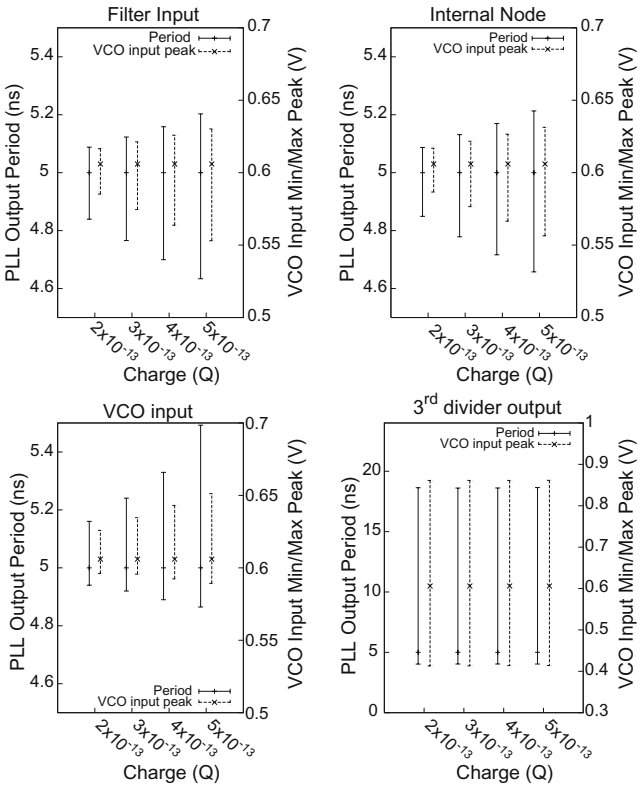



**Fig. 13** PLL period and VCO voltage peak due to transient fault injection in the filter and frequency divider (FD)

VCO input voltage is stable in ∼0.606 V, but results show peak voltages of 0.5 V larger than this value. Among the three points of the filter, the VCO input is the most sensitive to transient faults, due to its relation with the output frequency.

Transient fault experiences in the VCO are shown in Fig. 14. The injection points presented in this figure can be identified in Fig. 5a. These injection points correspond to main points in the three parts of the VCO (Delay cells, comparator and divider).

Four injection points were considered in the delay cells. It is assumed that the other points has similar impact with the chosen points. It is clear that transient faults has a negative effect in the case of the points a and b where the PLL period reaches to almost 6.5 ns and around 6 ns, respectively.

According the values resulting by the fault injection in points c and d, sometimes the effects of the transient faults cannot be clearly defined. The reason of these values is related to the fact that transient fault effects in the PLL output are not only dependents from the injection point and the injected charge $Q$, but the effects are also linked with a set of state conditions concerning the transistors connected with this point.

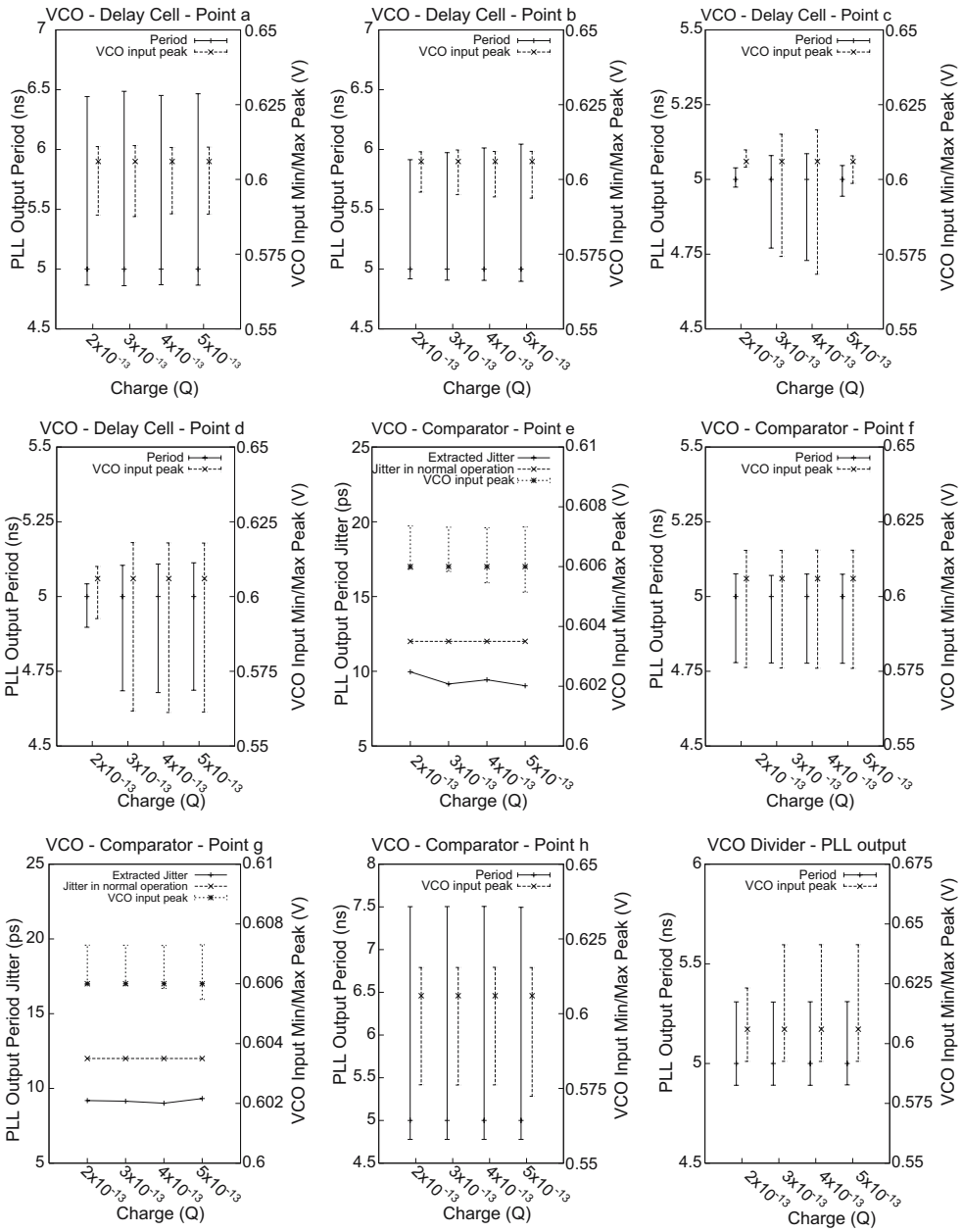



**Fig. 14** PLL period and VCO voltage peak due to transient fault injection in the voltage-controlled oscillator (VCO)

In the comparator, fault injections in points e and g do not cause any effect in the PLL normal operation. On the other hand, transient faults in the point f and specially the point h have negative effects in the PLL output frequency. The point h is very sensitive concerning transient faults because of its importance in the comparator. The inverter connected to point h is responsible to shape the output wave. Thus, when a transient fault hits this point, the distortion in the inverter input signal has a strong effect in the comparator output and in the PLL output, as consequence.

As seen in the last plot of the Fig. 14, transient fault injection in the PLL output are not so significant as the previously reported, but the results show that faults in this point can modify the PLL operation.

Figure 15 shows results of the transient fault injection in the PFD. Injection points are related to the points a, b, c and d in Fig. 3a. As the PFD is composed by two identical parts connected by an AND logic, only one of these parts was considered in the transient fault injection experience. Again, only the most significantly points are reported.

Fault injection experiences in the point a shows that the point can be sensitive to transients faults, but in particular conditions. In point b, the jitter in all injections is below the jitter acceptable by the design specifications.

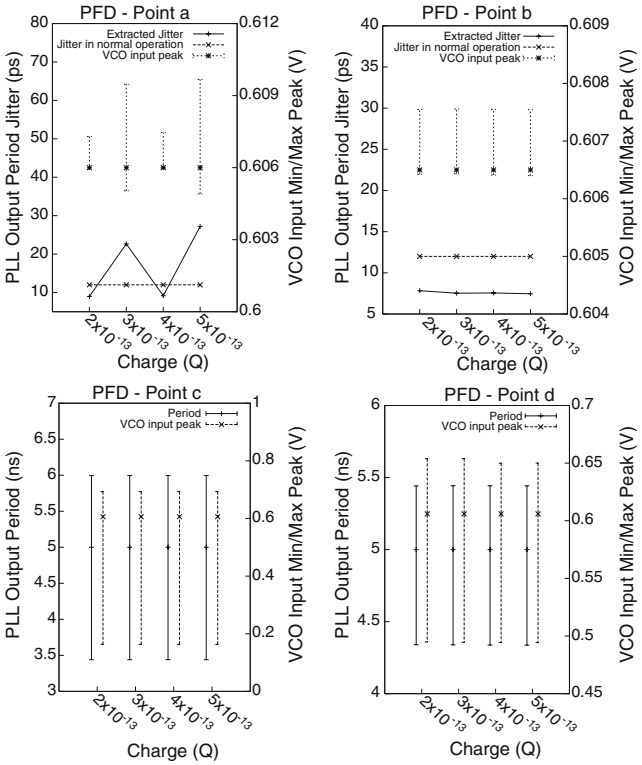



**Fig. 15** PLL period and VCO voltage peak due to transient fault injection in the PFD

Results extracted from the transient fault injections in points c and d shows the important sensibility of these points. Due to the fault injection, the PLL period staid between ∼4.3 ns and ∼5.5 ns in the point d and between ∼3.5 ns and ∼6 ns in the point c.

Obtained results about the sensitivity analysis in the PLL is shown in Table 1. Hardening techniques applied to digital blocks are widely discussed in literature. So, the PFD and divider blocks are not considered here. On the other hand, results shown high levels of functionality failure due to transient faults in the analog blocks of the PLL and this must be considered in the development of a radiation-hard PLL.

## 8 Transient Faults as Function of Device Size

An $\alpha$-particle injection results in a current at the faulty node. The current generates a voltage pulse whose magnitude depends on the transistors width, the capacitance at the node and the injected current. In this section, we discuss fault injection effects as function of device sizes. Results were obtained by an automated method where device structures are modified and simulated. We use the Cadence Ocean scripts to automate the simulation process.

Factors influencing the magnitude of the fault are the capacitance and the resistance of the transistor connected to a node. Thus, Increasing the transistor width we expect to improve the robustness of our PLL. Figure 16 shows the fault pulse width as function of the transistor width. Results show that transistors with 2 $\mu$m are robust against $\alpha$-particles with charge $Q = 0.2pC$, 4 $\mu$m for $Q = 0.3pC$, 9 $\mu$m for $Q = 0.4pC$ and width bigger than 10 $\mu$m for $Q = 0.5pC$. These results can be used in order to sizing up transistors and improve the robustness of the devices, mainly in digital

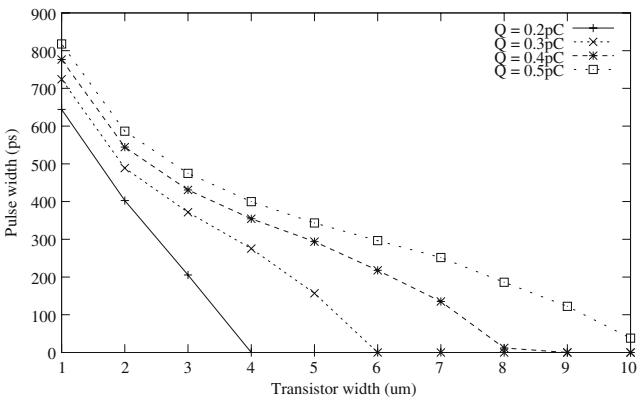



**Fig. 16** Fault width as function of the transistor width

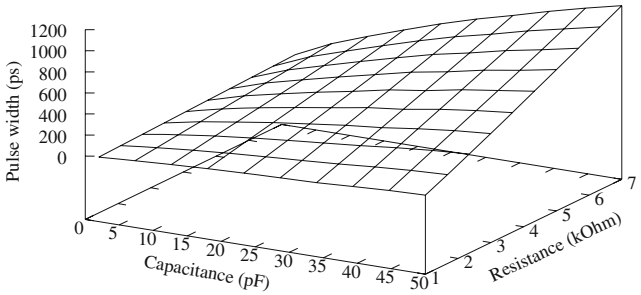



**Fig. 17** Pulse width as function of the capacitance and resistance in the filter

structures. According the target charge $Q$, we are able to size adequately the structures.

In analog structures, special attention must be taken due to the devices behavior. Analog structures are very sensitive to current and devices must be sized taken this sensitivity into account.

Figure 17 shows the fault pulse in the filter according variations on the capacitors and resistors. Figure 7 shows the schematic of the filter used in the PLL. In order to analyze the effects of the fault injection in the filter, we combined different capacitances to the capacitor C3 and resistances to the resistor R2 in the filter structure.

Results show that the fault pulse width present a linear behavior as function of the filter changes. This is important due to the possibility to test the filter configurations concerning the functionality but also the robustness against transient faults.

With these results we are able to find the best transistor sizing configuration according the target charge $Q$. In the same way, filter capacitors and resistors are sized and we can use the results to automatically generate the layout with our methodology.

## 9 Conclusion

This paper reports a case study on the automatic layout generation and transient fault injection analysis of a Phase-Locked Loop (PLL). A script methodology was used in association with a digital transistor placement & routing tool to generate the layout based on transistor level description and results shown that the methodology deals very well with the layout generation.

The main contribution of this work is the intensive fault injection experience in association with the semi-automatic layout generation. Results obtained from transient fault injection experiences allows to evaluate the PLL sensibility. The reported failure rate shows the importance of the development of radiation-hardened circuits. On going works include the research of automated methodology for finding the tradeoff between blocks sensibility and functionality, and automatic layout generation methods to radiation-hard PLL development.

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