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Threshold-Voltage Control Schemes through Substrate-Bias for Low-Power High-Speed CMOS LSI Design

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Abstract. Lowering supply voltage, V_{DD}, is the most effective means to reduce power dissipation of CMOS LSI design. In low V_{DD}, however, circuit delay increases and chip performance degrades. There are two means to maintain the chip performance: 1) to lower the threshold voltage, V_{th}, to recover circuit speed, or 2) to introduce parallel and/or pipeline architectures to make up for slow device speed. The first approach increases standby power dissipation due to low V_{th}, while the second approach degrades worst case circuit speed caused by V_{th} fluctuation in low V_{DD}. This paper presents two circuit techniques to solve these problems, in both of which V_{th} is controlled through substrate bias. A Standby Power Reduction (SPR) scheme raises V_{th} in a standby mode by applying substrate bias with a voltage-switch circuit. A Self-Adjusting Threshold-Voltage (SAT) scheme reduces V_{th} fluctuation in an active mode by adjusting substrate bias with a feed-back control circuit. Test chips are fabricated and effectiveness of the circuit techniques is examined. The SPR scheme reduces 50% of the active power dissipation while maintaining the speed and the standby power dissipation. The SAT scheme improves worst case circuit speed by a factor of 3 under a 1 V V_{DD}.

1. Introduction

For many years a 5-volt power-supply was employed in digital equipment. During this period power dissipation of CMOS LSI chips such as digital signal processors and microprocessors increased as a whole four-fold every three years [1]. It was a foregone conclusion of the constant voltage scaling.

A 3.3-volt power-supply is recently used for submicron CMOS VLSI designs and lower voltages are studied for future ULSI designs [1–7]. Reduction of supply voltage has been primarily driven by two factors; reliability of gate oxides [2] and reduction of power dissipation [3–7]. The principle driver of this trend is emerging portable digital media such as Personal Digital Assistance (PDA) and digital communication. Chip power dissipation should be held down to milliwatt levels for battery life. Standby power dissipation should also be saved as much as possible. According to the forecast by the Semiconductor Industry Association (SIA) [8] supply voltage for battery-operated products is to be 0.9 volts (end-of-life battery voltage) by 2004. Another motivation is a tight budget for consumer products such as a set-top box where an inexpensive plastic package is indispensable. Permitted limit of the chip power dissipation should be a little over 3 watts. Above the criterion, an expensive ceramic package is necessary. The SIA's roadmap predicts that the main stream of supply voltages for desktop products will be at 2.5 volts in 1998 and 1.5 volts in 2004.

Lowering supply voltage brings about a quadratic improvement in CMOS power dissipation, and therefore, is the most effective means. This simple solution to low-power design, however, comes at the cost of a speed penalty [3]. High-speed and low-power features are both required for portable multimedia equipment which delivers giga operations per second (GOPS) data processing performance for digital video use.

There are two different approaches to maintain the chip performance in low V_{DD}: 1) to lower the threshold voltage, V_{th}, to recover circuit speed [4, 5, 7], or 2) to introduce parallel and/or pipeline architectures to make up for slow device speed [3, 6]. The first approach increases standby power dissipation due to low V_{th} [9],

while the second approach degrades worst case circuit speed caused by V_{th} fluctuation in low V_{DD} [10].

The focus of this paper is to address these problems in low V_{DD} or low V_{th}, and to present solutions by circuit techniques. Two circuit schemes are presented to solve these problems, in both of which V_{th} is controlled through substrate bias, V_{BB}. A Standby Power Reduction (SPR) scheme [9] raises V_{th} and cut off leakage in a standby mode by applying deep V_{BB} with a voltage-switch circuit. A Self-Adjusting Threshold-Voltage (SAT) scheme [10] reduces V_{th} fluctuation in an active mode by adjusting V_{BB} with a feed-back control circuit.

The SPR scheme is presented in Section 2, and the SAT scheme is discussed in Section 3. In both sections, problems in low-V_{DD} or low-V_{th} circuit design are addressed, followed by descriptions of the proposed schemes, details in their circuit designs, and reports on experimental results. Section 5 is dedicated for conclusions.

2. Standby Power Reduction (SPR) Scheme

2.1. Problems

In order to understand circuit delay and power dissipation dependence on V_{DD} and V_{th}, a 2-input NAND gate with fanout of 5 is simulated assuming a 0.3 μm CMOS technology. The fanout condition corresponds to the statistical average of gate loads in typical logic LSI designs. The same V_{th} is chosen for nMOS and pMOS. Gate width of all the MOSFETs is 10 μm.

Figures 1(a)–(c) show the simulation results by SPICE. Delay contour lines are projected on the V_{DD}-V_{th} plane in Fig. 1(a). If V_{th} is reduced to 0.3 V, V_{DD} can be lowered down to 2 V while maintaining the speed at $V_{th} = 0.7$ V and $V_{DD} = 3$ V, typical operation condition for high-speed LSI design. Figure 1(b) shows a simulated power dependence on V_{DD} and V_{th}. The power includes subthreshold leakage current, crowbar current, and CV^2 component. At $V_{DD} = 3$ V and $V_{th} = 0.7$ V the power dissipation is 0.107 mW, while at $V_{DD} = 2$ V and $V_{th} = 0.3$ V it is reduced to 0.048 mW. This corresponds to the active power reduction of more than 50% while maintaining the speed. The energy-delay (ED) product is also plotted in Fig. 1(c) as a function of V_{DD} and V_{th}. Reducing the ED product is a good direction for optimizing LSI design for portable use, since the ED product reflects the battery consumption (E) for completing a job in a certain time (D) [5]. The ED product is also reduced from 5.18×10^{-24} J·s to 2.32×10^{-24} J·s.

The only drawback of choosing 0.3 V V_{th} is the increase in standby power dissipation. In order to solve

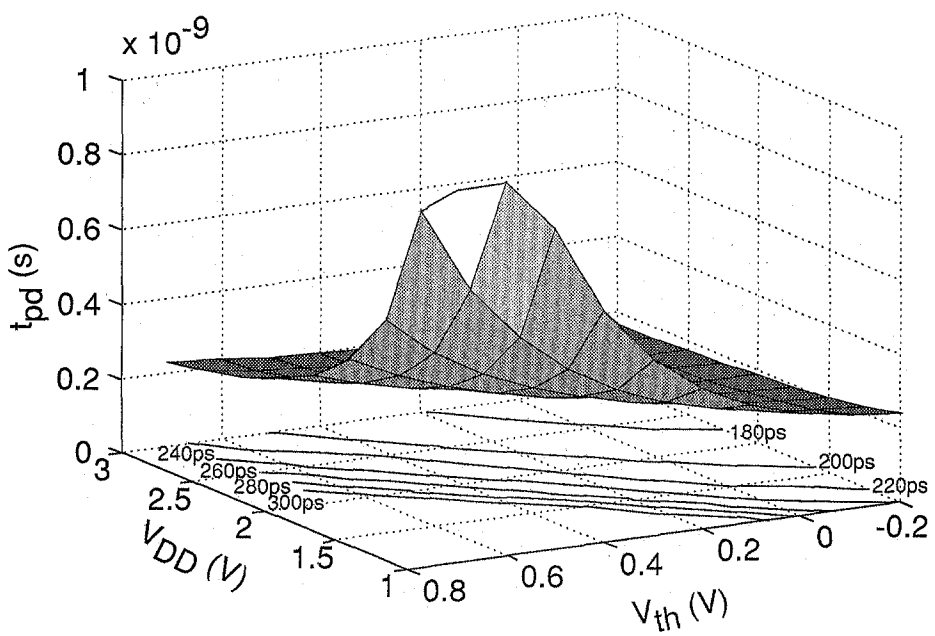

Figure 1a. Simulated delay dependence on V_{DD} and V_{th} by SPICE. V_{th} signifies the absolute value of the threshold voltage of MOSFETs. Same V_{th} is set for nMOS and pMOS.

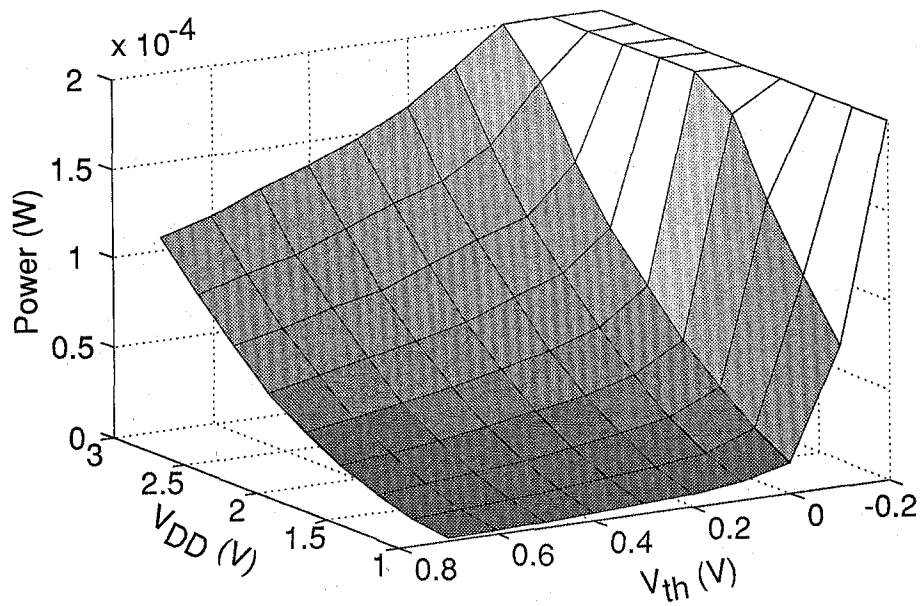

Figure 1b. Simulated power dissipation dependence on V_{DD} and V_{th} by SPICE. Activation ratio of 0.3 and cycle time of 30 × t_{pd} are assumed. The power includes subthreshold leakage current, crowbar current, and CV^2 component.

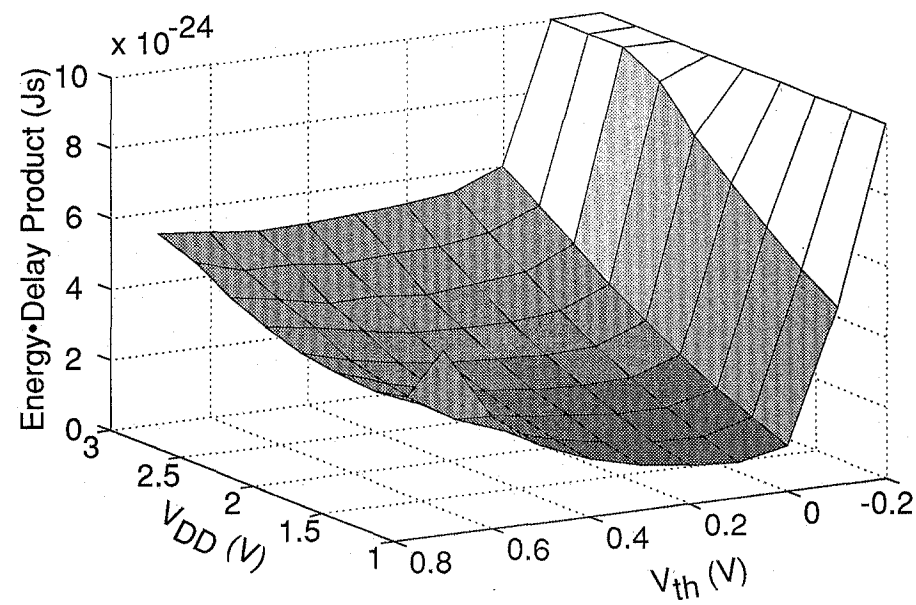

Figure 1c. Simulated dependence of energy-delay (ED) product on V_{DD} and V_{th} by SPICE.

the standby power problem, multithreshold-voltage CMOS technology was proposed [11] where two different V_{th} MOSFETs were employed; low V_{th} for fast circuit operation and high V_{th} for providing and cutting internal supply voltage. This scheme, however, requires very large transistors for the internal power-supply control to impose area and yield penalties, otherwise degrading circuit speed. Furthermore it cannot be applied to memory elements.

A new standby power reduction scheme is proposed in the next section which dynamically changes V_{th} in the active and standby mode by applying substrate bias. This scheme does not impose those penalties in area and speed, nor the limitation in usage.

2.2. *Circuit Design*

The main idea of this standby power reduction (SPR) scheme is that substrate bias is applied in the standby mode to increase V_{th} and cut off leakage current, while in the active mode the substrate bias is not applied to assure high-speed operation. Figure 2 shows a measured I_{DS}-V_{GS} characteristics of the 0.3 μm nMOS transistor. By applying V_{BB} of -2 V, V_{th} can be increased by 0.4 V. This means that if V_{BB} of -2 V is applied in the standby mode, V_{th} is increased from 0.3 V to 0.7 V, and thus realizes the same standby current as the design in $V_{th} = 0.7$ V.

Figure 3 depicts a circuit diagram of the proposed SPR scheme. Figure 4 shows the simulated waveforms of the circuit. The circuit consists of a level-shifting part and a voltage-switching part. When chip enable, CE, is asserted in the active mode, the n-well bias, V_{NWELL}, becomes equal to V_{DD} (= 2 V), and the p-well bias, V_{PWELL}, becomes V_{SS}. When CE is disabled in the standby mode, V_{NWELL} equals V_{NBB} which is set at 4 V, and V_{PWELL} becomes V_{PBB}, which is $-$ 2V. A standby-to-active mode transition and an active-to-standby mode transition take less than 100 ns. Power dissipation of the SPR circuit in the standby mode is less than 0.1 μA. V_{NBB}, V_{PBB}, V_{DD} and V_{SS} are applied from external sources, but power supply lines for V_{NBB} and V_{PBB} need to supply only 0.1 μA or less current. The diodes in the circuit are built using a junction-well structure through which current flows only in the active mode.

In designing the circuit, care is taken so that no transistor sees high-voltage stress of gate oxide and junctions. Figure 5(a) shows V_{GS}-V_{GD} trajectories of

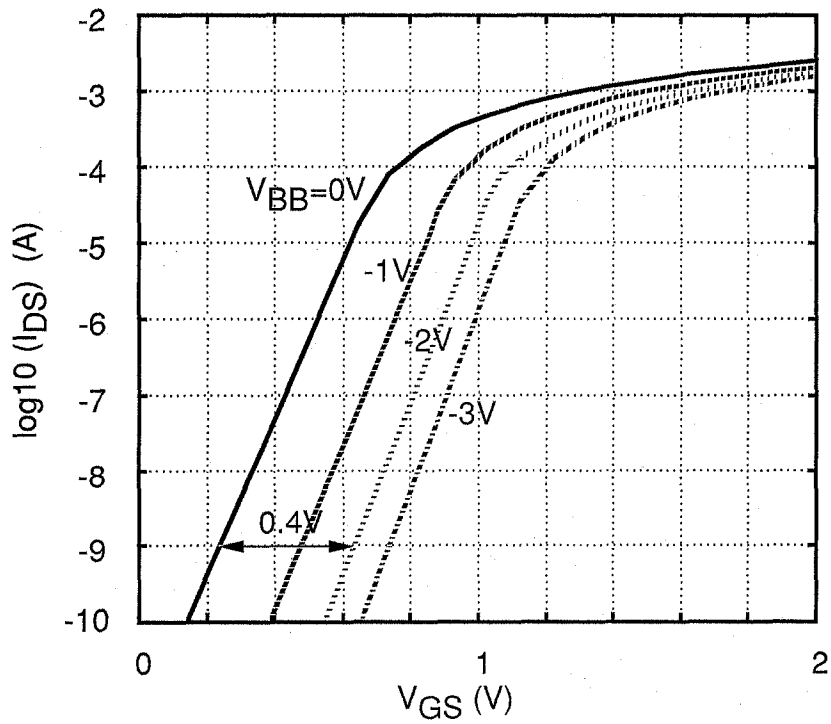

Figure 2. Measured I_{DS}-V_{GS} characteristics of 0.65 μm nMOS transistor. By applying V_{BB} of -2 V, V_{th} can be increased by 0.4 V.

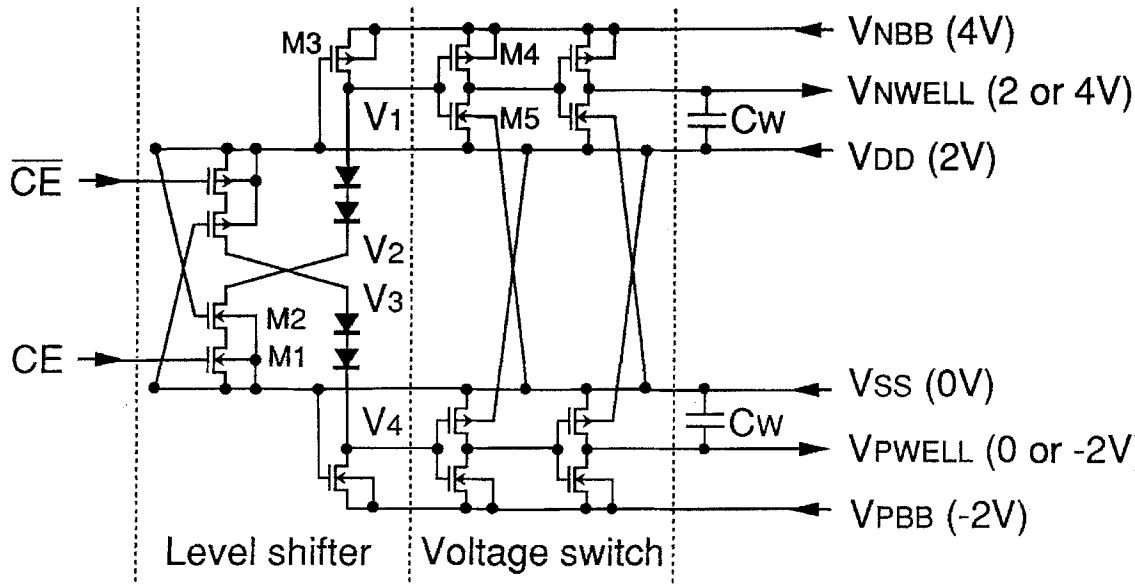

Figure 3. Circuit diagram of the SPR circuit. Well capacitance, C_w, is assumed to be 1000 pF.

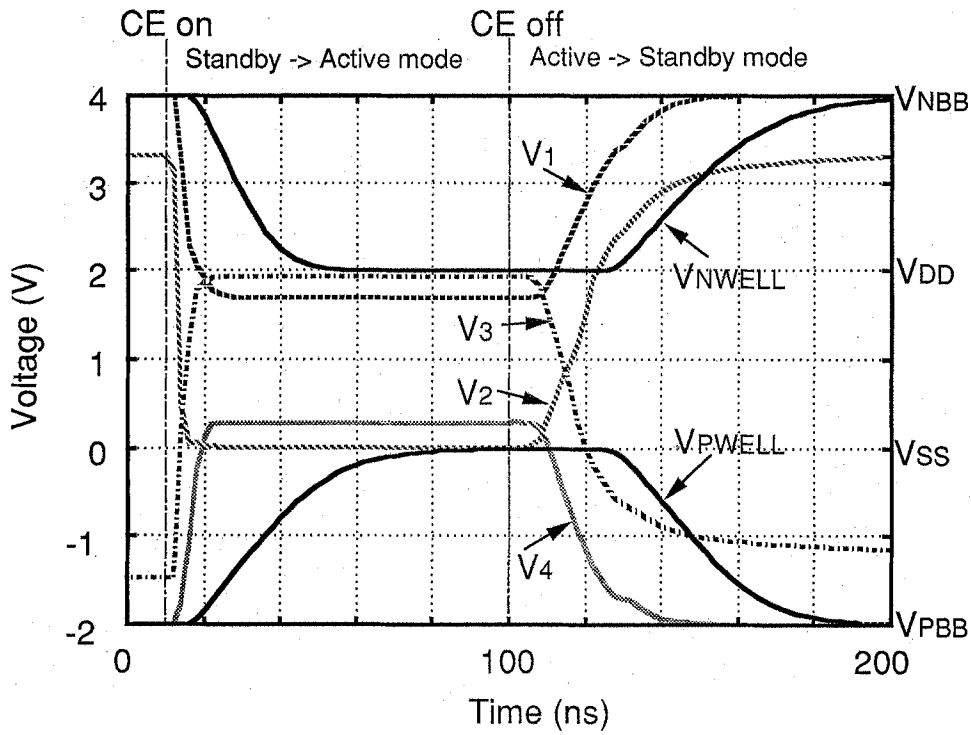

Figure 4. Simulated waveforms of the SPR circuit. Standby-to-active mode transition and active-to-standby mode transition take less than 100 ns.

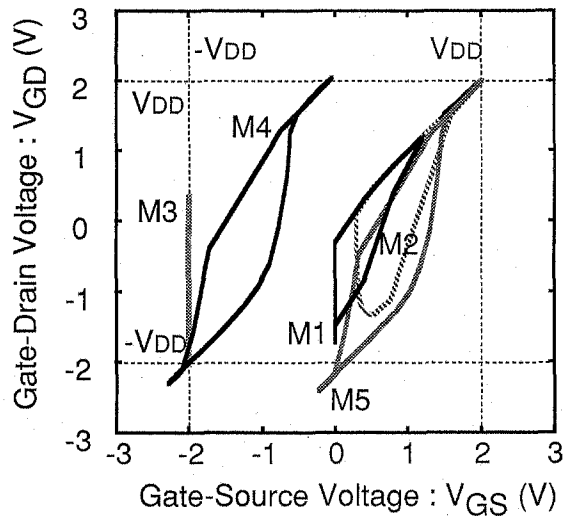

Figure 5a. V_{GS}-V_{GD} trajectories of MOSFETs used in the SPR circuit. The trajectory does not go beyond $\pm(V_{DD} + \alpha)$. Notations from M1 through M5 correspond to transistor names in Fig. 3.

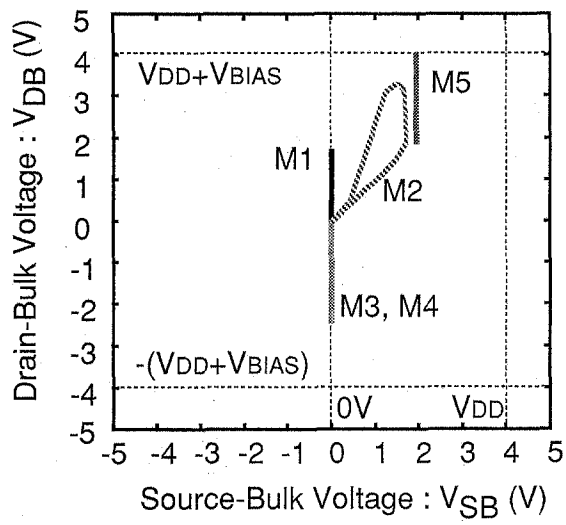

Figure 5b. V_{SB}-V_{DB} trajectories of MOSFETs used in the SPR circuit. The trajectory does not go beyond $\pm(V_{DD} + V_{BIAS})$. Notations from M1 through M5 correspond to transistor names in Fig. 3.

MOSFETs used in the SPR circuit. The trajectories do not go beyond $\pm(V_{DD} + \alpha)$, which assures sufficient reliability of gate oxide. Figure 5(b) depicts V_{SB}-V_{DB} trajectories of MOSFETs used in the SPR circuit, where V_{SB} represents the source-bulk voltage and V_{DB} represents the drain-bulk voltage. The trajectories do not go beyond $\pm(V_{DD} + V_{BIAS})$, where V_{BIAS} signifies the larger voltage of $|V_{NBB} - V_{DD}|$ and $|V_{SS} - V_{PBB}|$. This voltage is applied to junctions, but the junction breakdown voltage of the 0.3 μm MOSFETs is more than 9 V, and hence, junction breakdown does not occur for any MOSFET.

2.3. *Experimental Results*

Figure 6 shows a micrograph of a test chip. A ring oscillator constructed with 49 stages of 2-input NAND gates and the SPR circuit are implemented using the 0.3 μm process technology. The SPR circuit occupies 2500 μm^2 for either n-well or p-well bias circuit. In cases where nMOS circuit mostly determines the speed as in nMOS pass transistor logic, only V_{th} for nMOS should be lowered and hence only p-well bias circuit is needed. If both of the n-well and p-well bias circuits are required as in Fig. 3, 5000 μm^2 Si area is occupied and a triple-well technology is to be used. The standby current of less than 0.1 μA is measured on the test chip in the standby mode. In the active mode the standby current is measured larger by three orders. The speed of the 2-input NAND gate of 300 ps is achieved at $V_{DD} = 2$ V. Setting time of the substrate bias is less than 100 ns.

The proposed SPR scheme is fully compatible with the existing CAD tools including automatic placement and routers. As for standard cell library, cell layouts should be modified to separate substrate bias lines and power supply lines. The substrate bias lines, however, can be as narrow as possible and can be scaled. The area overhead to the total chip is estimated to be less than 5%.

3. Self-Adjusting Threshold-Voltage (SAT) Scheme

3.1. *Problems*

Figure 7 shows how much the V_{th} fluctuation affects gate propagation delay, t_{pd}, in various V_{DD} regime. Alpha-power law MOSFET model [12] is used to estimate t_{pd} whose expression is written as follows:

$$t_{pd} = \frac{C_L V_{DD}}{(V_{DD} - V_{th})^{\alpha}} \left[\left(\frac{1}{2} - \frac{1 - V_{th}/V_{DD}}{1 + \alpha} \right) \times \left(\frac{0.9}{0.8} + \frac{V_{D0}}{0.8 V_{DD}} \ln \frac{10 V_{D0}}{e V_{DD}} \right) + \frac{1}{2} \right],$$

where V_{D0} is a drain saturation voltage and C_L is a load capacitance. Typical parameter values that $\alpha = 1.3$ and $V_{D0}/V_{DD} = 0.5$ are employed in this estimation.

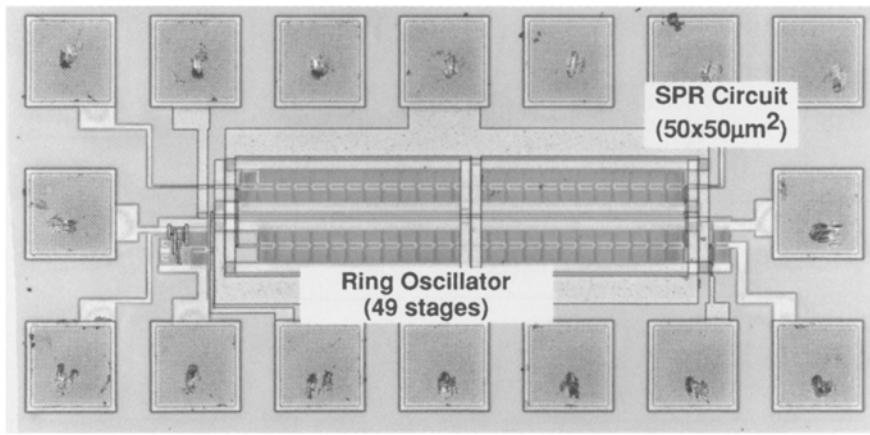

Figure 6. Micrograph of SPR test chip. The SPR circuit occupies 2500 μm^2 for either n-well or p-well bias circuit.

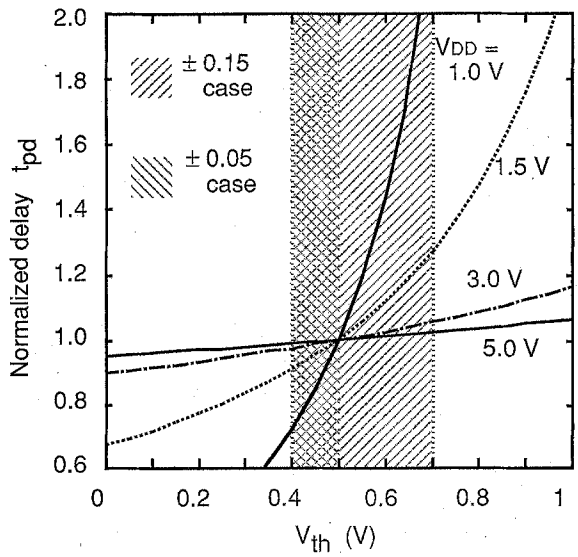

Figure 7. Calculated t_{pd} dependence on V_{th} for various V_{DD}.

The minimum V_{th} in the distribution is determined by a total leakage current of a chip. If the V_{th} is too low, the power dissipation of a chip surmounts the specified maximum power dissipation. For example, if it is specified that 0.4 V is the minimum V_{th} and the V_{th} fluctuation is ± 0.15 V, then the worst chips show the threshold voltage of 0.7 V. In order to achieve high performance yield, the speed of these worst chips determines the speed specification of the product. The V_{th} distribution of this case is suggested by a hatched region in Fig. 7.

On the other hand, if the V_{th} fluctuation can be reduced to ± 0.05 V, the worst V_{th} becomes 0.5 V. The situation is indicated by another hatched region in Fig. 7. The speed difference of the worst cases is a factor of 1.3 at 1.5 V V_{DD} and a factor of 3 at 1 V V_{DD}.

3.2. *Circuit Design*

Figure 8 illustrates a block diagram of the proposed Self-Adjusting Threshold-Voltage (SAT) scheme to reduce the V_{th} fluctuation down to ± 0.05 V. A leakage sensor senses leakage current of a representative MOSFET and outputs a control signal, V_{cont}, to Self-Substrate-Bias (SSB) circuit. V_{cont} is controlled so that it triggers the SSB only when the leakage is higher than a certain preset level. Suppose an nMOS case (a pMOS case is conceptually the same). The SSB, when triggered, draws charge from p-wells to lower substrate bias, V_{BB}. The lowered V_{BB} in turn increases V_{th} of nMOS and lowers leakage current. The V_{BB} is distributed to all the p-wells on a chip.

Thus, V_{th} is controlled to make the leakage current equal to the specified value, that is, V_{th} is set to the lowest possible value that satisfies the power specification. Consequently, the speed is optimized. Substrate bias is also good for reducing junction capacitance to further improve the performance of a chip. Process target of V_{th} should be low enough so that SSB can tune V_{th} to whatever value that is necessary. V_{th} of pMOS can be controlled in the same way at the same time.

Figure 9(a) shows a measured subthreshold I_{DS}-V_{GS} characteristics of an nMOS and Fig. 9(b) shows a measured I_{DS} dependence on V_{th}. The I_{DS} can be written as

$$I_{DS} \propto \exp\{(V_{GS} - V_{th})/s\},$$

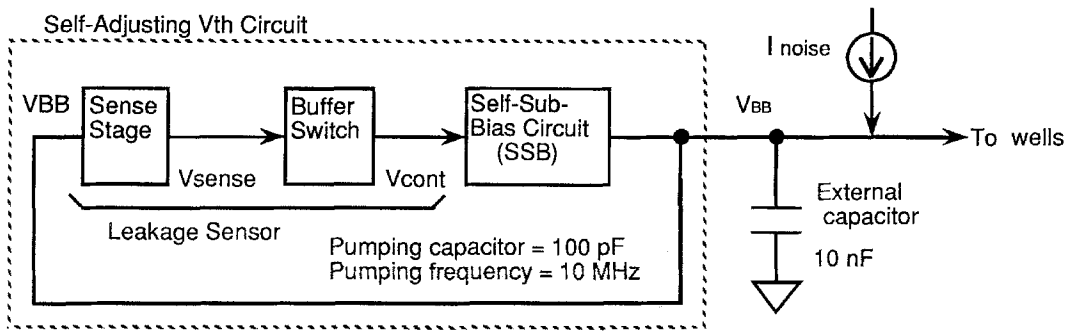

Figure 8. Block diagram of Self-Adjusting Threshold-Voltage (SAT) scheme.

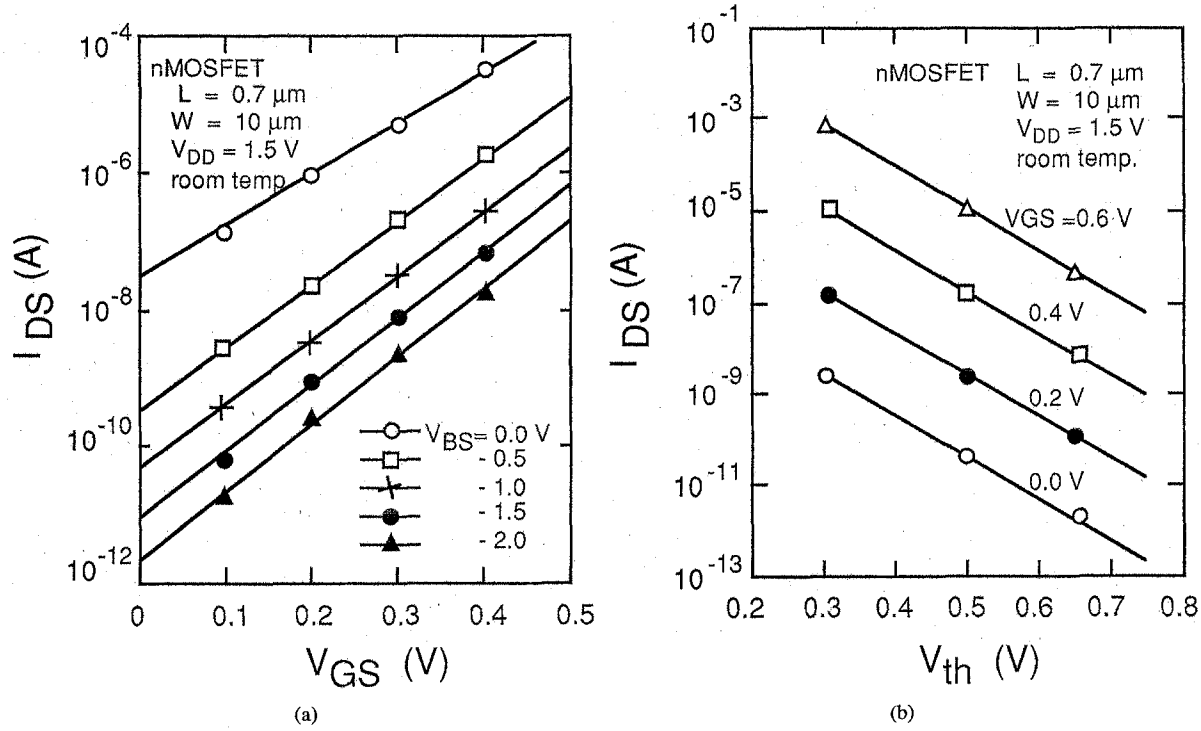

Figure 9. (a) Measured sub-threshold I_{DS}-V_{GS} characteristics for various V_{BS}. (b) Measured sub-threshold I_{DS}-V_{th} characteristics for various V_{GS}.

where s is called the s-factor and is about 110 mV/decade when V_{BS} is zero and becomes 90 mV/decade when V_{BS} is less than -1 V. This suggests that with the substrate bias, V_{th} can be set lower than in the case without the substrate bias with maintaining the leakage current the same.

Figure 10 is a circuit diagram of the leakage sensor. The leakage current through the representative MOSFET M1 can vary by a factor of as much as 10 when V_{th} is changed by only 0.1 V because of the exponential dependence of the leakage current on V_{th}. The leakage current is amplified by the load L. The load can be either a resistor made by a well diffusion of about 1 MΩ or pMOS whose process and environmental (temperature and V_{DD}) variation is within a factor of 3. This corresponds to V_{th} controllability of ±0.02 V.

V_G is generated by dividing V_{DD} and is set around 0.2 V. This finite V_G is necessary to enhance the leakage current and shortens the dynamic delay of the sensor.

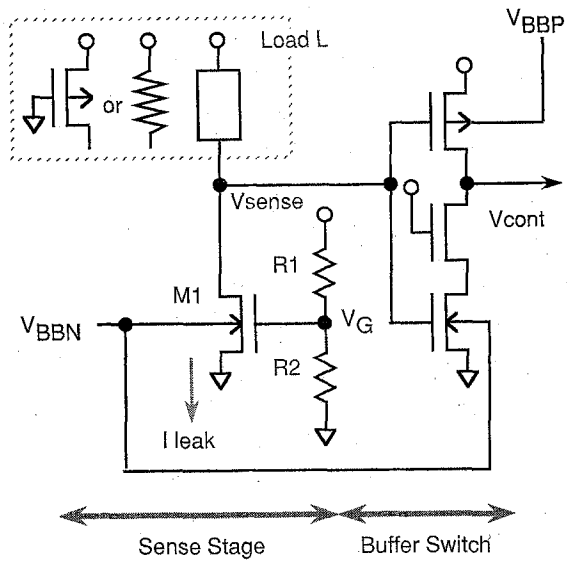

Figure 10. Leakage sensor in SAT scheme.

Since V_{DD} can be controlled within ±5%, the fluctuation of V_G is ±0.01 V. This value should be added to ±0.02 V mentioned above, totaling ±0.03 V of static controllability. The fluctuation of the switch buffer gives negligible effects to the controllability.

Figure 11 depicts dynamic behavior of the circuit. A large capacitor of 10 nF is connected to V_{BB} in external of a chip. The current noise is assumed to be 1 mA which corresponds to hot-carrier current generated by 10 A of drain channel current. The delay of the sensor introduces dynamic controllability which is additive to the static controllability. Overall V_{th} controllability including static and dynamic effects is ±0.05 V.

3.3. *Experimental Results*

A test chip is fabricated by a standard 0.7 μm CMOS process, whose micro-photograph is shown in Fig. 12. The size is 1.5 mm × 0.7 mm including SSB and the leakage sensor. The chip includes only a p-well bias generator for controlling V_{th} of nMOS so that the size should be doubled if threshold voltages of both pMOS and nMOS are to be controlled. The implemented SSB circuit employs a conventional configuration. Figure 13 shows a measured V_{th} static controllability which is shown to be less than ±0.025 V.

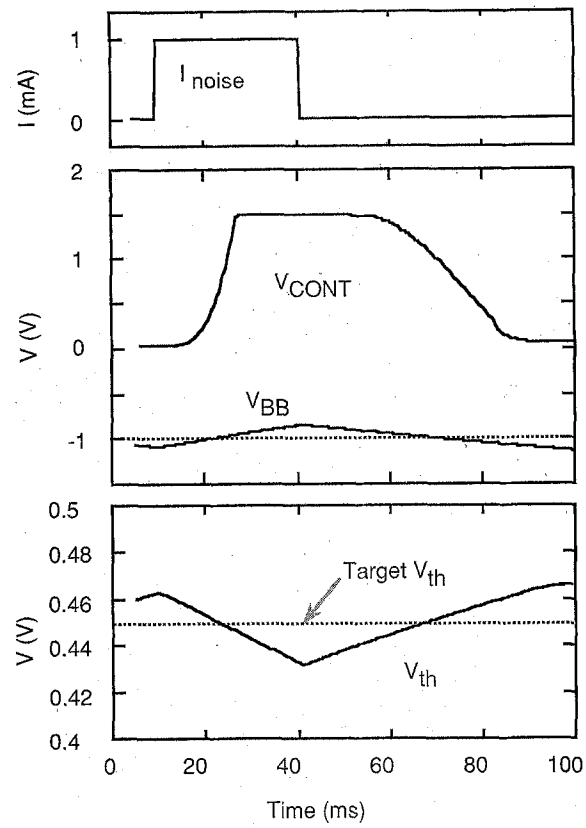

Figure 11. Simulated waveforms of V_{BB} and V_{th} in SAT scheme.

4. Conclusions

Two circuit techniques have been studied for low-power high-speed CMOS LSI design, in both of which V_{th} is controlled through substrate bias. The Standby Power Reduction (SPR) scheme raises V_{th} in the standby mode by applying substrate bias. It reduces 50% of the active power dissipation while maintaining the speed and the standby power dissipation. The Self-Adjusting Threshold-Voltage (SAT) scheme reduces V_{th} fluctuation in the active mode by adjusting substrate bias. It improves worst case circuit speed by a factor of 3 under a 1 V V_{DD}.

The SPR scheme is mainly used for low V_{DD} and low V_{th} design for portable use, while the SAT scheme is primarily employed for low V_{DD} and standard V_{th} design. The two schemes, therefore, can take different approaches; in the SPR the substrate bias is applied from external sources with the voltage switch circuit, while in the SAT the substrate bias is generated internally with the SSB circuit. If V_{DD} is reduced below 1 V,

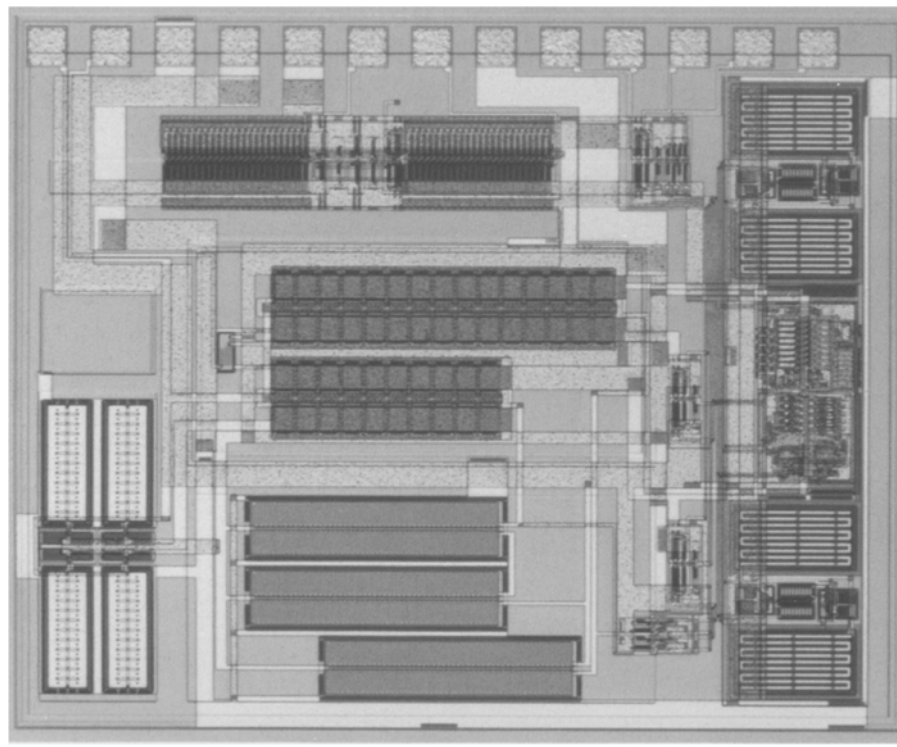

Figure 12. Micrograph of SAT test chip.

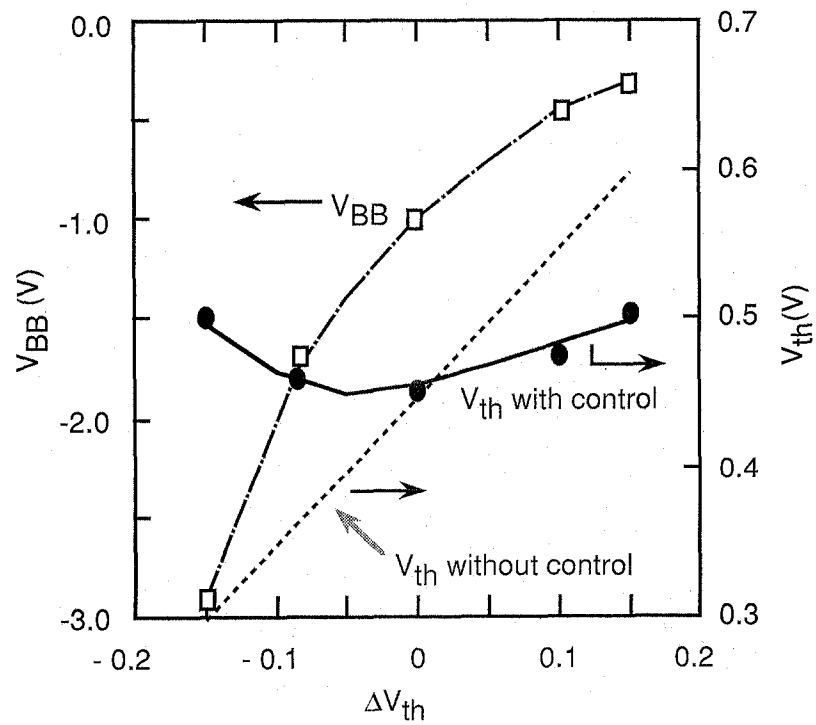

Figure 13. Measured V_{th} controllability dependence on process fluctuation ΔV_{th}.

however, the speed variation due to the V_{th} fluctuation cannot be ignored even in low V_{th}. A unified scheme which can solve the two problems in a unified way will be required in the future and should be studied.

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