Using Commercial Semiconductor Technologies in Space†

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Abstract

New issues are discussed that must be considered when unhardened commercial technologies are used in space applications, as well as hardness assurance techniques. Large differences in dose-rate effects were observed for different circuit types from the same manufacturer, which may be due to differences in the thickness of isolation oxides used in processing. Data are presented for scaled MOS devices that show how total dose hardness and hard error rates are projected as devices are scaled to smaller feature size. Hard errors are expected to be a significant problem for devices with feature size below 0.6 μm.

I. Introduction

The increase in capitalization cost of semiconductor fabrication facilities has gradually changed the economics of semiconductor production,*[1]* with the result that few manufacturers can afford to produce devices for special niche markets, such as radiation-hardened devices.[††] This factor, coupled with the recent decline in the military semiconductor market, has increased the pressure to adapt unhardened commercial devices for space applications.

This paper discusses recent results from the Jet Propulsion Laboratory that provide insight into behavior of commercial devices in space environments, along with the types of controls and tests that are required to successfully use them in space applications. Three issues are particularly significant: the new problem of enhanced damage in bipolar devices at low dose rate; mixed-signal devices, which are difficult to evaluate because of their complexity and requirements for close tolerances; and single-event hard errors, which are likely to increase in importance as digital devices are scaled to smaller dimensions.

In addition to these issues, there is a basic problem in dealing with radiation test data on complex devices from commercial processes. In most cases data is available from only a small sample, and it is not at all clear how to apply statistical factors that will satisfactorily bound the behavior of the total population. This is especially true for devices that respond to radiation in discontinuous ways, e.g. with sudden changes in key electrical parameters, or abrupt functional failure.

II. Dose Rate Effects in Bipolar Technologies

A. Experimental Results

The discovery that some bipolar device technologies exhibit more damage at low dose rates*[2-4]* greatly increases the difficulty of testing and qualifying these devices for space applications. The problem is most severe for special pnp devices used in many linear circuits with conventional junction isolation. Damage in pnp devices can be 6-7 times greater at low dose rates than at high dose rates.*[2]* The pnp devices that are fabricated with conventional junction isolation remain sensitive to dose rate at very low rates -- ≈ 0.002 to 0.005 rad(Si)/s -- which are impractical for routine testing because of the extremely long test times required. Note that npn devices from these processes are generally not sensitive to dose rate effects below approximately 1 rad(Si)/s. Thus, circuits which use both types of components may exhibit different failure modes at low and high dose rates because of the different amount of relative damage that occurs in the two types of components at low dose rates.

Dose rate effects are relatively easy to evaluate in linear circuits with pnp input transistors because the input bias current provides a straightforward way to measure input transistor gain degradation. However, different circuit types from the same basic manufacturing process may respond somewhat differently at low dose rates. For example, Figure 1 compares input bias current degradation of two devices with similar input stage designs from the

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††A limited number of part types is available from hardened or radiation-tolerant lines, and it is preferable to use such devices for space applications because their radiation hardness is explicitly controlled. When commercial parts are used , the user must ensure that testing and control of the parts is sufficient to detect devices with marginal radiation capability.

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same manufacturer (Motorola). Both devices use substrate pnp transistors, but the typical value of input bias current is three times greater for the LM111 than for the LM324.

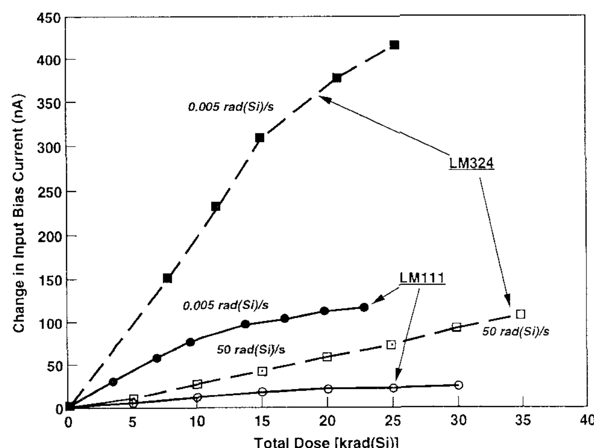

Figure 1. Degradation of input bias current of two different circuits from the same manufacturer with similar input stages.

At high dose rates, degradation of input bias current is nearly identical for the two circuits, taking into account the factor of three difference in initial values. Although both circuits are more damaged when they are irradiated at low dose rate, degradation in the LM324 is much greater. Damage in the LM111 saturates at relatively low total dose levels, reducing the significance of enhanced damage. Input bias current of the LM324 continues to degrade at low dose rate as the radiation level increases, and consequently it is well above the specification limit even at 10 krad(Si). Even higher damage occurred in this device at 0.002 rad(Si)/s, although this is not shown in the figure. As discussed later, there are significant differences in oxide thickness of these two circuits that may be a factor in the different way that they respond under low dose-rate irradiations. These results show that large differences can occur between different circuit types produced by the same manufacturer, and that it is risky to make blanket assessments about dose-rate effects on the basis of tests on a small number of device types.

Although input bias current is a straightforward parameter to evaluate, failure modes in linear circuits are quite complex, which can make it very difficult to extrapolate test results to lower dose rates. In some cases, small differences in damage can lead to large differences in the radiation degradation of critical circuit parameters. For example, Figure 2 shows how input offset voltage of the LM324 operational amplifier depends on total dose at different dose rates. Input bias current measurements showed that the substrate pnp input transistors degraded severely at low dose rates, but the dose rate dependence appeared to level off at about 0.005 rad(Si)/s. Tests at still lower dose rates showed that input offset voltage began to change significantly at low levels, even though this parameter changed very little at much higher levels when the part was tested at higher dose rates. This is attributed to degradation of the internal current sources in the device, which use lateral pnp transistors that are highly susceptible to dose-rate effects.

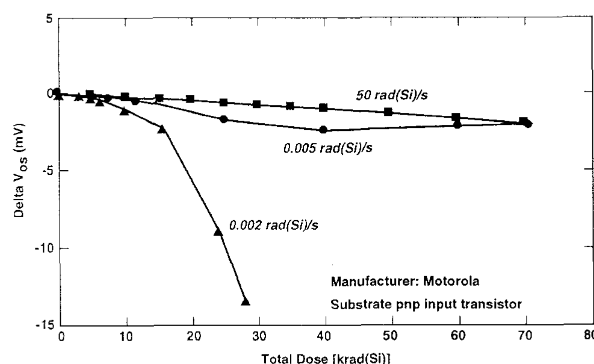

Figure 2. Degradation of input offset voltage of the LM324 operational amplifier at various dose rates.

As shown by previous tests of voltage regulators,*[3]* enhanced damage can vary substantially between manufacturers of the same part type, and it is sometimes possible to select a specific manufacturer with less severe dose rate behavior. Figure 3 shows input bias current degradation for LM111 voltage comparators, which use substrate pnp input

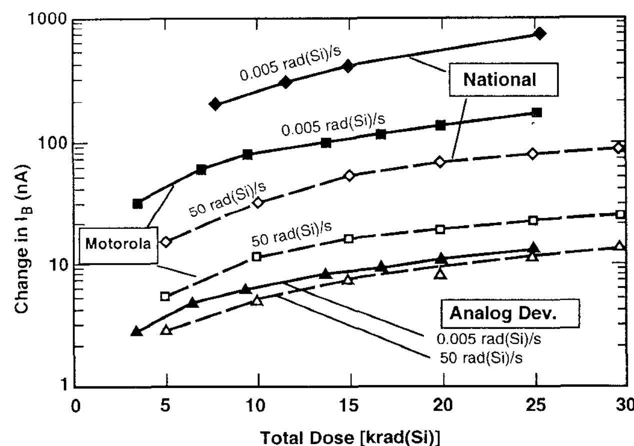

Figure 3. Total dose degradation of LM111 comparators from three manufacturers at high and very low dose rates.

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transistors, procured from three different vendors, and tested at two widely different dose rates. For two of the manufacturers, damage of the input transistors is about six times greater at low dose rates. Devices from the third manufacturer show only a small increase in damage at the lowest dose rate, even though the geometry of the input transistors of this vendor are identical to that of the vendor with the highest damage at low dose rates. Thus, in this instance it is possible to select a vendor with little dose rate dependence, and thereby avoid the need for costly testing at very low dose rates. However, tests at intermediate dose rates -- ≈ 0.02 - 0.05 rad(Si)/s -- would still be required during lot hardness assurance tests in order to verify that dose rate effects are sufficiently low.

Although LM111 comparators produced by this manufacturer were relatively insensitive to total dose and exhibited only a slight dose rate effect, this was not true for OP42 op-amps produced by the same manufacturer. The OP42 uses a similar process that includes compatible JFETs along with the usual bipolar components. The manufacturer's data sheet includes representative data showing that its parameters are only slightly affected by total dose out to 1 Mrad(Si), based on many years of testing at high dose rate. However, tests at low dose rates produced an entirely different result. As shown in Figure 4, extremely large changes in input offset voltage occurred in this device at relatively low levels that were only apparent during low dose rate tests. Similar results were obtained for two different production lots, fabricated in 1988 and 1994. The degradation was so severe that the part was removed from applications in the Cassini spacecraft. Initial modeling of the device indicates that degradation of internal pnp transistors in the second stage are responsible for the large change in offset voltage.

Other operational amplifiers with JFET input designs also appear to be sensitive to dose-rate effects. Figure 4 also shows a typical result for a different device type. Because of the JFET inputs, it is more difficult to evaluate ionization damage in circuits of this type. It is even more difficult to determine how severe the changes in offset voltage could be for a larger sample size because of the abrupt changes that occur. For this reason, linear devices with FET structures should be considered high risk, and require very thorough characterization over a range of dose rates before they are used in space applications.

B. Physical Features and Potential Mechanisms

Oxide Thickness

The dramatic difference in dose-rate effects between the LM111 and OP42 from Analog Devices suggests that physical differences in the construction of these devices may play a role in their radiation response. To investigate this, a scanning electron microscope was used to measure device cross sections in various regions of the circuit. Die were removed from the package, mounted on metal holders, and lapped to allow cross section measurements to be made.

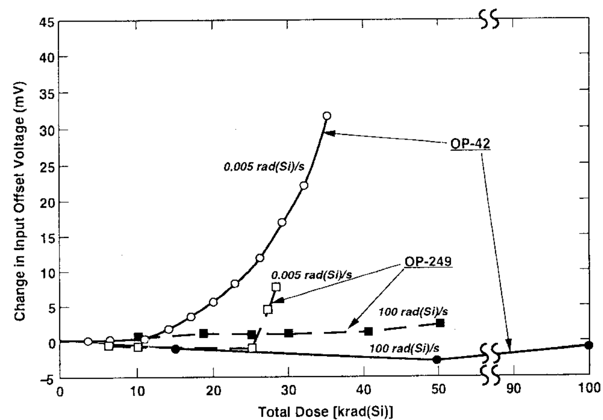

Figure 4. Offset voltage degradation of the OP42 op-amp at high and low dose rates. The large changes in offset voltage that occurred at low dose rates were not evident in tests under high dose rate conditions.

In conventional junction-isolated devices, one of the earliest steps in processing is formation of isolated n-type pockets in the epitaxial region by diffusion of boron. The boron must eventually diffuse completely through the epitaxial region -- typically 15 μm thick for these processes -- to the underlying p-substrate. This step requires a very thick oxide at the surface in order to prevent boron from diffusing in regions other than the regions in which the isolation diffusion is made.

The n-type pockets are used as the collector of npn transistors, but function as the base region of substrate and lateral pnp transistors. After subsequent processing the thick isolation oxide is only present over the n-collector regions. Thus, the oxide thickness is quite different in the emitter-base region of the normal npn transistor and the pnp transistors in these processes.

Figure 5 shows the oxide profiles of the LM111 and OP42 devices manufactured by Analog Devices. The oxide over the base region is essentially the same

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for both processes. However, the isolation oxides are quite different, as shown in the figure. The isolation oxide of the OP42 is nearly twice as thick as the isolation oxide used in the LM111.

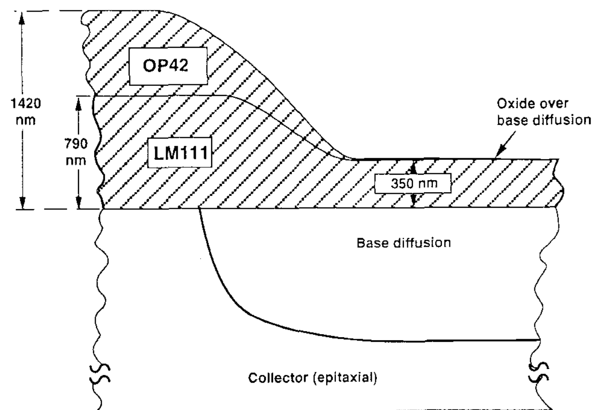

Figure 5. Base-emitter oxide thicknesses of the substrate transistor of the LM111 and OP42 (measured with a scanning electron microscope).

Oxide thickness measurements were also made on LM111 and LM324 circuits from Motorola. The oxide thickness of the LM324, which exhibited substantially more damage (see Figure 1), was 9800 Å, about 15% greater than that of the LM111

Bulk Charge Trapping

Only limited work has been done on charge transport and trapping in thick oxides under low-field conditions. Some of these results appear to be consistent with dose-rate effects in bipolar devices, and provide support for a model based on bulk charge trapping deep within the oxide.

Earlier studies of transport in field oxides showed that the charge transport time was extended approximately three orders of magnitude under low field conditions, and that the time for half the charge to be transported depended on the cube of oxide thickness.[6] This work also showed that for thick oxides a significant fraction of the charge was not transported, but appeared to remain trapped in bulk regions of the oxide. The bulk charge component was very low for oxides with thicknesses below 5000 Å, but appeared to increase rapidly for thicker oxides.

Thus, the earlier charge transport work implies that there are two separate charge components, one of which is permanently trapped within the bulk region of the oxide, and the other which acts like the mobile charge that has been widely studied in gate oxides.

One possible explanation for the increased damage in pnp transistors is simply the increased oxide thickness, which has a larger relative amount of bulk charge. Transport studies showed that the bulk charge component was a very strong function of oxide thickness, and this is consistent with the behavior of some of bipolar circuit results discussed earlier.

The dose rate dependence can be explained by postulating that bulk charge trapping is reduced because of higher recombination with the excess electron density that is present during higher dose rates. Charge transport times are in approximate agreement with the time scale for dose-rate effects. It explains why the npn and pnp devices in junction-isolated linear ICs have different dose-rate dependencies, and suggests that devices with very thick oxides -- such as the OP42 op-amp, may continue to affected by dose rate even below 0.001 rad(Si)/s. Experiments that combine successive irradiation at high and low dose rate have verified that the bulk charge component acts independently from the mobile charge component, corroborating the above interpretation for junction-isolated devices with thick oxides.*[7]*

Comparison with Other Mechanisms

Other mechanisms for bipolar dose rate effects have been proposed by Fleetwood et al.[8] They propose that some holes are trapped in metastable states within the bulk region of the oxide. During high dose-rate irradiation, the large number of defects in the bulk region of the oxide retard the hole transport process. The metastable trapped holes act in conjunction with the space charge near the interface to reduce charge yield in the bulk.

This model was primarily developed for oxides of intermediate thickness, and assumes that long-term trapping in the bulk of the oxide is small. The authors used thermally stimulated current measurements to investigate the differences in trapped charge for low- and high-field irradiation conditions, However, none of their oxides exhibited the permanent deep traps that appear to occur in thicker oxides. Thus, although the model of Fleetwood et al. describes effects in thinner oxides, it does not appear to be consistent with the more permanent bulk charge that apparently occurs in thick oxides.

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C. Potential Solutions

The difference in the behavior of pnp and npn devices at low dose rates makes it impossible to properly account for dose rate effects in complex circuits by applying a guardband factor to high dose rate data. The OP42 results shows that different mechanisms can appear at low dose rates which are not at all evident at high dose rates.

Tests at Multiple Dose Rates

One way to deal with this problem is to require tests at two different dose rates, selecting the lower dose rate so that it is sufficiently high to allow tests to be completed in days or weeks instead of the extremely long time periods imposed by the very low dose rates discussed above. Although this is not a substitute for doing tests at very low dose rates for devices that have severe enhanced damage at low dose rate, it is a more pragmatic way to identify devices that have minimal sensitivity to dose-rate effects. JPL has implemented this approach for several devices, using 0.02 rad(Si)/s for the lowest dose rate.

High-Temperature Irradiation

Irradiation at 60 °C was proposed by Fleetwood et al. as a possible alternative to tests at low dose rate.[8] They found that irradiation at elevated temperature produced essentially the same results as low dose-rate irradiation at room temperature for the oxide structures in their study. More recent work has been done by Schrimpf, et al. which show that the damage continues to increase at the temperature is raised above 100 °C.[9] They suggest that irradiation at 100 - 125 °C may be a good alternative to low dose-rate testing.

This work is very promising, but more work needs to be done before such a procedure can be implemented in test standards. The high-temperature data does not appear to level off, but is still increasing rapidly above 100 °C. Elevated temperature irradiations need to be evaluated for additional processes in order to provide a more accurate data base for test standards, and verify that a suitable combination of temperature and dose rate can be selected.

III. MIXED-SIGNAL DEVICES

Most spacecraft use analog-to-digital converters in key interface applications. Great strides have been made in the design of A/D converters, increasing their accuracy and precision. Two different technologies are generally used for successive-approximation converters: (1) BiCMOS designs, which employ conventional architectures, and selectively use bipolar devices in key circuit areas to decrease offset voltage and simplify design of input amplifiers and comparators; and (2) full CMOS designs, some of which employ complex internal calibration and error correction methods to overcome the inherent limitations of CMOS devices in linear amplifiers. Both technologies generally have much higher voltage ratings than conventional digital CMOS circuits, which in turn requires thicker gate and field oxides. Because of the thicker oxides, these devices are generally far more sensitive to ionizing radiation than digital technologies, and anneal relatively quickly after irradiation. They are also sensitive to rebound effects. Evaluating the radiation performance of A/D converters is especially difficult because of the close electrical tolerances, complex design, and the difficulty of interpreting annealing and dose-rate effects for parameters that often change in an abrupt way once a critical total dose level is exceeded.

Somewhat surprisingly, the dominant failure modes are generally not small deviations in the conversion accuracy, but global failure modes such as increase in leakage current ,changes in offset of internal amplifiers and reference circuits, or stuck bits in the digital output stage. At high dose rates commercial devices typically fail between 5 and 20 krad(Si), but often recover after initial irradiation within a few hours. However, rebound and annealing may cause them to have a different response at low dose rates, and in some cases they may fail at even lower levels under low dose-rate conditions. For CMOS devices standard rebound testing using high-temperature annealing is satisfactory,*[12]* but this approach has not been verified for BiCMOS devices, which may be affected differently because of the interplay between bipolar and CMOS devices. Dose rate effects in bipolar devices may also limit the applicability of accelerated temperature for rebound testing of BiCMOS devices.

These types of A/D converters usually exhibit different failure mechanisms when they are irradiated at low dose rate. Specific failure modes depend on the device architecture. Internal reference voltages are typically one of the key parameters, even though buried zener references are generally used. Figure 6 shows the change in reference voltage for three different comparator technologies. The CMOS technology uses a self-calibrating architecture. Changes in the two BiCMOS devices are sufficient to

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cause them to fail specifications at levels below 10 krad(Si). Although the CMOS converter exhibits much larger changes, the internal calibration scheme partially compensates for the degradation.

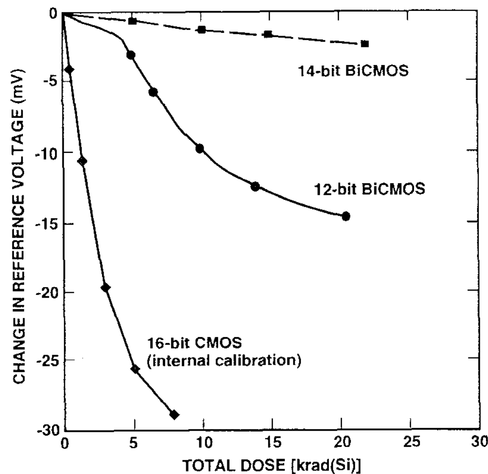

Figure 6. Changes in reference voltage after total dose degradation for three different A/D converter technologies.

Significant differences in radiation hardness can occur for different lots of A/D converters, and for this reason it is generally necessary to use sample testing on a lot-by-lot basis for these technologies. JPL has observed differences of as much as a factor of three in the total dose hardness, and in some cases the dominant failure mode differs for different lots. This is not surprising because of the complex design of these parts, but it increases the difficulty of characterizing and controlling their radiation response.

IV. Scaled MOS Technologies

Highly scaled MOS devices are extremely competitive, and production lines are frequently upgraded to provide technical and cost advantages. These changes can affect their radiation response, and it is necessary to evaluate the radiation performance of these devices on a regular basis in order to ensure compliance with radiation requirements. For example, some manufacturers use on-chip voltage regulators to provide a lower operating voltage for internal circuitry. The internal voltage is usually not specified, and may be lowered for future design upgrades with smaller feature size

Device scaling can affect radiation behavior in several ways, including total dose sensitivity, which remains an important issue; SEU; latchup sensitivity; and the new problem of single-event hard errors.*[10-13]* The latter issue is particularly important because it may limit the effectiveness of system solutions, such as error-detection-and-correction, that are often used to correct single-event upset effects.

A. Total Dose Effects.

Recent test data shows that field oxide leakage often dominates total dose degradation in advanced MOS devices, *[14]* and hence total dose hardness levels have not followed first-order scaling predictions based on gate oxide sensitivity. Even though gate oxide threshold voltage shifts are expected to decrease as gate oxide thicknesses are reduced, second-order effects become increasingly important, particularly for devices with reduced power supply voltage and reduced internal operating margins.*[15]* The increased sensitivity of scaled devices to threshold voltage will generally make them more sensitive to small variations in threshold voltage than older devices with 5 V power supplies, which have much larger operating margins .

An additional factor to be considered is the statistical variation of threshold voltage on devices from a single chip, which results primarily from statistical fluctuations in the number of dopant atoms. Figure 7 shows the spread in retention times for a 16 Mb DRAM; the distribution is consistent with a three-standard deviation range of 26 mV in threshold voltage of internal transistors, and agrees closely with predictions of the effect of doping atom fluctuations. *[16]*

The voltage fluctuation remains nearly constant after irradiation, further corroborating the assumption that internal threshold voltage variations are responsible for the spread in retention times.

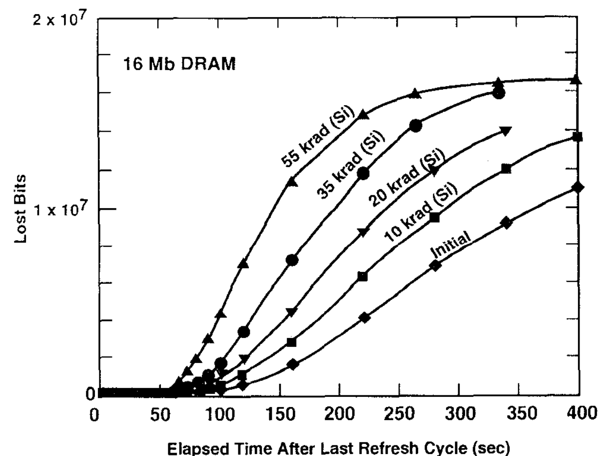

Figure 7. Lost bits vs. refresh delay for a 16 Mbit DRAM at various dose rates. The dispersion is due to threshold voltage variations of pass transistors within the DRAM array.

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These variations will cause a small number of transistors within a large chip to fail at much lower total dose levels than average transistors on the chip, and can only be detected by implementing very thorough test methods. As shown in Figure 6, the effect is already apparent in the radiation response of devices with feature sizes in the 0.6 to 0.8 u range, and will be more severe as devices are scaled further because of larger statistical fluctuations and reduced internal operating margins.

B. Hard Errors.

Two types of single-event hard errors have been discovered, one involving microdose deposition from a single ion (or a small number of single ions) in the gate region,*[10-12]* and a second which appears to cause catastrophic gate failure, similar to gate rupture.*[13]* The second mechanism is particularly important because it causes catastrophic failure, not just a small increase in subthreshold leakage, and may affect devices other than storage arrays, such as random logic in microprocessors. This type of hard error could occur in any MOS transistor with a gate that is biased with a positive voltage during the time that it is struck by a heavy ion.

Initial results have shown that device scaling lowers the threshold for the onset of the second mechanism. Figure 8 shows the dependence of the failure threshold LET on gate oxide field strength for two devices from the same vendor with different oxide thickness. The process with the reduced oxide thickness is a "shrunk" version of the initial design that is electrically equivalent, and supersedes the original version. The slope is very close to the square root dependence that was established for gate rupture in power MOSFETs, and suggests that the threshold LET for this mechanism will continue to decrease as devices are scaled further, nearing the iron threshold as devices are scaled to the third generation (2.5 V power supplies).

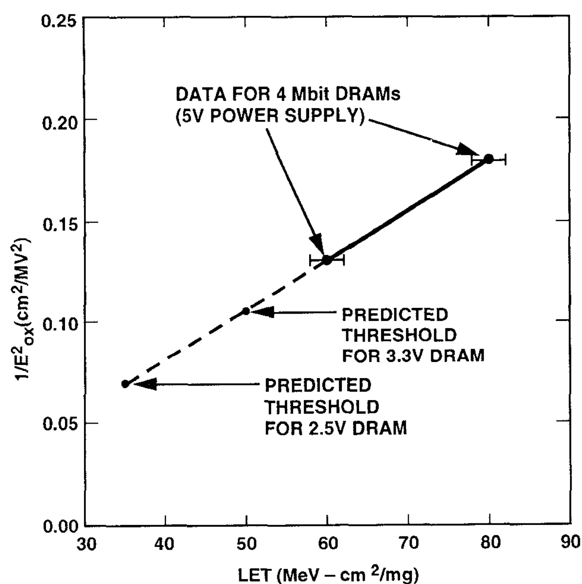

Figure 8. Dependence of threshold LET for gate rupture from heavy ions on scaled DRAM technologies.

The hard error rate of devices with feature size above approximately 0.6 μm is sufficiently low to keep this problem from becoming significant. However, the error rate is expected to increase significantly as devices are scaled further. Figure 9 shows the projected hard error rate vs. feature size for a circuit with one-million transistors,[†] which was calculated by combining the assumed field dependence for catastrophic hard errors with the galactic cosmic-ray environment. Curves are shown for two different scaling approaches, taken from the electron device literature: one for circuits optimized for speed,*[17]* and the other optimized for low power.*[18]* The abrupt increase in the error rate for the high-speed scaling curve occurs because of the change in GCR particles when the LET falls below the "iron" threshold.

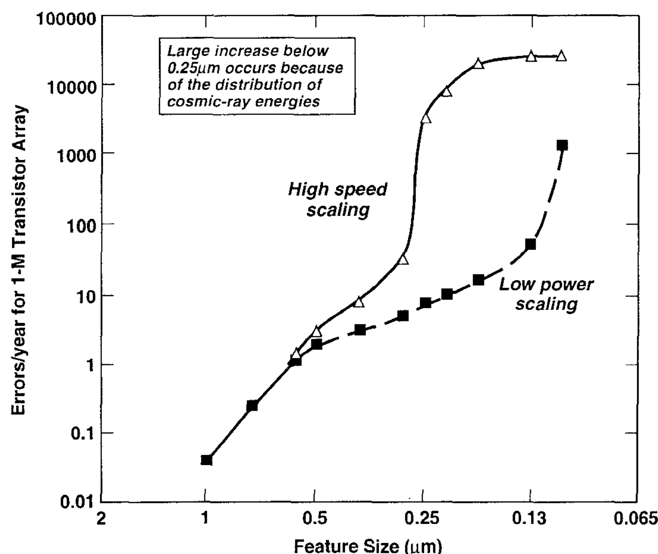

Figure 9. Predicted error rate for a one-million transistor array in space for devices with different feature sizes

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[†]The array size is arbitrary, and is chosen simply to allow the projected hard-error rate to be compared for different scaling approaches. In most cases, larger numbers of transistors would likely occur on a single die as devices are scaled, so the circuit error rate would increase even faster than shown in the figure.

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Although the scaling predictions strongly suggest that hard errors will become a dominant problem for scaled devices in space, more work needs to be done to increase the understanding of this phenomenon. Oxide field strength clearly plays an important role, but other device characteristics are also important which may cause the hard-error rate to be less severe. Thickness of semiconductor regions are generally reduced as devices are scaled, and higher doping levels are required. These factors may reduce the transient charge that is coupled to the oxide region from a heavy-ion strike, modifying the expected error rate. Nevertheless, the projected increase in hard-error rate with increasing density is so large that it appears likely that hard errors will be an important issue in the future. Similar effects have been seen in programmable logic arrays, so there appear to be a number of related phenomena that are becoming significant as devices are scaled to feature sizes below one micron.*[19]*

V. Discussion

The wide range of device functions and increased performance of commercial devices provides advantages in designs that are sensitive to weight and power, particularly in small spacecraft. However, device complexity and new radiation problems that are exacerbated by device scaling make it more difficult to verify that commercial designs will work satisfactorily in space. Careful attention must be given to device failure modes and test methods,, as well as variations in the response of devices produced at different time periods. Increased emphasis is needed on low dose rate testing in order to establish a better technical framework for hardness assurance and qualification of these technologies, as well as on new effects such as single-event hard errors that must be accounted for when new technologies are applied in space.

Other factors can also be important in commercial technologies which have not been discussed in this paper. This includes latchup, which remains an important problem, and the issue of package type and burn-in, that not only affect reliability but can also affect the sensitivity of devices to ionizing radiation.*[20]*

Because less is known about commercial device technology, greater effort must be spent on radiation testing and hardness assurance in order to use these devices in space. Lot-sample testing is required for many devices because of the lower margins that generally exist for these technologies along with the possibility that changes will occur in the manufacturing process that affect the radiation response.

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