Radiation hardened high performance CMOS VLSI circuit designs

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Abstract: For space or nuclear plant applications, radiation tolerant high performance CMOS VLSI circuit designs, utilising scaled CMOS/SOS technology and scaled bulk CMOS technology, have been reviewed, placing strong emphasis on total dose radiation hardness. Based on radiation induced degradations for conventional CMOS circuits, such as inverters, ring oscillators and memory circuits, total dose radiation hardening technologies have been discussed. Low temperature process and thin oxide introductions are effective for radiation induced threshold voltage shift reduction. Total dose radiation induced field leakage is suppressed by introducing a thin field oxide between the source/drain diffusion layers and a thick field oxide in NMOS transistors, combined with the buried P^+ diffusion layer at the P well edge, without sacrificing speed performance. In addition to device/process technologies for total dose radiation hardening, usefulness for NAND logics and static circuits in radiation tolerant CMOS VLSI designs, are shown. Furthermore, radiation tolerance superiority of clocked gate CMOS circuits to transfer gate CMOS circuits in SOS devices, are indicated. Latchup immunity and SEU immunity have also been discussed, for both SOS and bulk devices. Effectiveness of epitaxial substrate and wide transistor introductions for latchup and SEU prevention, is shown, respectively. CMOS/SOS radiation hardened VLSIs and bulk CMOS radiation hardened VLSIs which have been developed by utilising above mentioned technologies, are reported. The entire work described in this paper has made it possible to design radiation hardened high performance VLSI circuits for space or nuclear plant applications, utilising both CMOS/SOS technology and bulk CMOS technology.

1 Introduction

The sophistication trend in space satellite or nuclear reactor electronic systems requires microelectronic components with high performance and high levels of tolerance to severe radiation environments.

Among microelectronic devices, MOS devices are most attractive for VLSI circuits realisation, because of their high packing density superiority over other semiconductor microelectronic devices. Among MOS technologies, CMOS technology has many features that makes it ideal for use in VLSI circuit designs. These features include high noise immunity, low power and high speed operation.

However, in radiation environments, MOS devices suffer from serious degradations and failures. Ionising radiation effects in MOS transistors such as buildup of positive charge in the oxide layer and interface state production, lead to threshold voltage shifts and channel mobility degradation [1–8]. These parameter shifts and radiation induced leakage cause MOS circuits characteristics degradations and failures [9–12]. In addition to these total dose radiation effects which cause permanent failures, transient ionising radiation exposure produces photocurrents in every junction in integrated circuits [13–15]. These photocurrents can cause logic upset or latchup [16–22] as the dose rate is increased. Latchup is caused by SCR action of parasitic bipolar transistors in bulk CMOS structures.

To design radiation tolerant CMOS VLSIs for space and nuclear plant applications, it is necessary to prevent these radiation induced characteristic degradations and circuit failures.

In this paper, radiation tolerant high performance CMOS VLSI circuit designs for space and nuclear plant applications are reviewed, mainly from the viewpoints of total dose radiation hardness, latchup immunity, circuit performance, and packing density.

2 Total dose effects and hardening

2.1 Total dose radiation effects

Although it is well known that positive charge buildup in the oxide layer and interface state production, due to ionising radiation effects, lead to threshold voltage shifts and channel mobility degradation, it was confirmed experimentally that total dose effects, ranging to 10^5 rad (Si), lead to NMOS and PMOS threshold negative shifts and negligibly small mobility degradation [23–25]. Furthermore, the threshold voltage shifts depend on the gate oxide bias condition during irradiation [26].

The NMOS and PMOS threshold voltage negative shifts cause CMOS inverter logic threshold to shift negatively. Fig. 1 shows CMOS/SOS inverter logic threshold shift as a function of γ ray total dose [23]. Utilising a CMOS/SOS ring oscillator with NMOS and PMOS substrate electrodes [27, 28], the postradiation logic delay difference was also observed, which is caused by threshold voltage shift difference due to effective gate oxide radiation bias difference. Fig. 2 shows logic delay ratio, tpd(postrad)/tpd(prerad), as a function of supply voltage,

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taking NMOS substrate terminal bias during irradiation as a parameter [29].

CMOS current mirror sense amplifier [30] unbalance caused by driver NMOS threshold voltage difference due to irradiation bias difference is shown in Fig. 3. The dashed line indicates ideal characteristics. Deviation from the ideal characteristics causes sense amplifier performance degradation, resulting in memory performance degradation. After 1.7×10^4 rad(Si) irradiation, the deviation was 5% of supply voltage V_{DD}. After 6.3×10^4 rad(Si) irradiation, it was 20% of supply voltage. Six transistor Flip Flop CMOS memory cell [30] failures were also observed, which are caused by driver NMOS leakage in memory cells due to negative threshold voltage shifts. After 1.7×10^4 rad(Si) irradiation, data could not be written into the cell when a 4 V supply voltage was applied to V_{DD}, but could when a 5 V supply voltage was applied. After 6.3×10^4 rad(Si) irradiation, data could not be written into the cell even when a 5 V supply voltage was applied to V_{DD}.

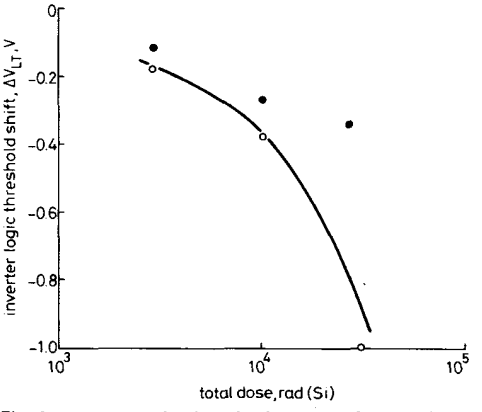

Fig. 1 *Experimental and simulated CMOS/SOS inverter logic threshold shift as function of γ-ray total dose*

Logic threshold defined as input voltage at which the output is half supply voltage V_{DD}.
$L_{eff} = 2.5$ μm
$t_{ox} = 500$ Å
Irradiation bias $V_{DD} = V_{IN} = 5$ V
○ Experiment — Calculation
Irradiation bias $V_{DD} = V_{IN} = 0$ V
● Experiment

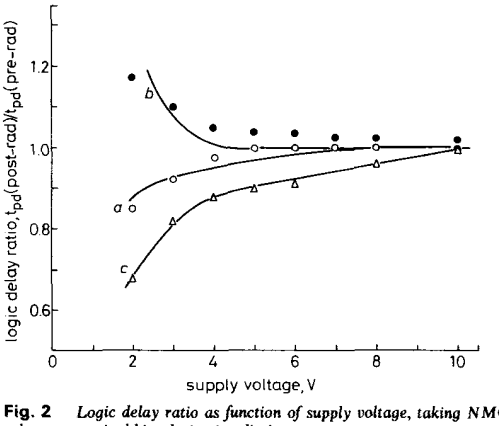

Fig. 2 *Logic delay ratio as function of supply voltage, taking NMOS substrate terminal bias during irradiation as parameter*

tpd(postrad) is delay time after 10^5 rad (Si) irradiation, and tpd(prerad) is logic delay before exposure. NMOS substrate terminal biasing conditions: *a* 0 V, *b* 5 V, *c* −5 V
Irradiation biasing condition: V_{DD} 5 V, $V_{PMOS\,SUB}$ 5 V, V_{SS} 0 V
a Experimental and simulated logic delay decreased after irradiation at low operating voltage
b Experimental and simulated logic delay increased after irradiation at low operating voltage
c Experimentally and theoretically, decreasing logic delay more pronounced than in *a*.
$L_{eff} = 1.5$ μm
$t_{ox} = 500$ Å
——— Simulation
○△○ Experiment

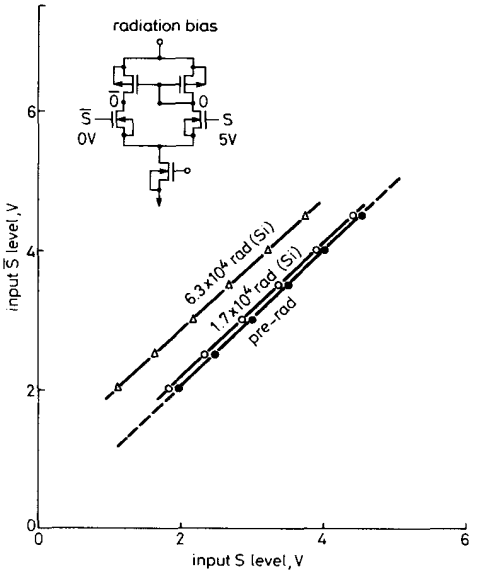

Fig. 3 *Input levels into sense amplifier when node 0 level is equal to node $\bar{0}$*

Irradiation biases for inputs S, $\bar{S}$ = 5 V, 0 V, respectively. Deviation from dashed line causes circuit performance degradation

All the results for conventional devices mentioned above indicate that threshold voltage shift prevention is necessary in radiation tolerant VLSI designs.

Total dose ionising effects in any material can be defined in terms of the energy deposited, by ionisation, in the material per unit mass. The unit of the energy deposition has been defined in cgs units as

1 rad(material) = 100 erg of energy

absorbed by ionisation per gram of material.

2.2 Process technology for hardening

Threshold voltage shifts due to radiation effects, strongly depend on oxidation temperature and postoxidation process temperature [31–34]. For >950°C processes, threshold voltage shifts are significantly large. However, threshold voltage shifts and their process temperature dependence are small for <900°C processes. Therefore, it is possible to suppress threshold voltage shifts due to radiation by lowering gate oxidation temperature and postoxidation process temperature below 900°C [31–33].

Furthermore, threshold voltage shifts depend strongly on the gate oxide thickness, and are substantially greater for thicker oxide MOS transistor [26, 31, 34, 35]. Therefore, it is useful to introduce thin oxide transistors in radiation hardened VLSI designs [32, 33].

2.3 Device technology for hardening

Structural hardening is useful to suppress NMOS field leakage, caused by large negative threshold voltage shifts in parasitic field MOS transistors, due to total dose radiation effects [36–38].

There are two kinds of thick field oxide leakage. One is source/drain leakage under NMOS gate edges. The other is field leakage between NMOS transistors.

Thin field oxide between source/drain diffusion layer and thick field oxide was successfully introduced to suppress the former radiation induced field leakage, as shown in Fig. 4. A boron implantation, $1 \times 10^{12}/cm^2$ at 40 keV, was applied to the thin oxide region. Fig. 5

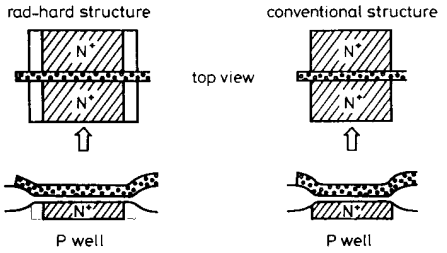

Fig. 4 *Structurally radiation hardened and conventional bulk NMOS transistors*

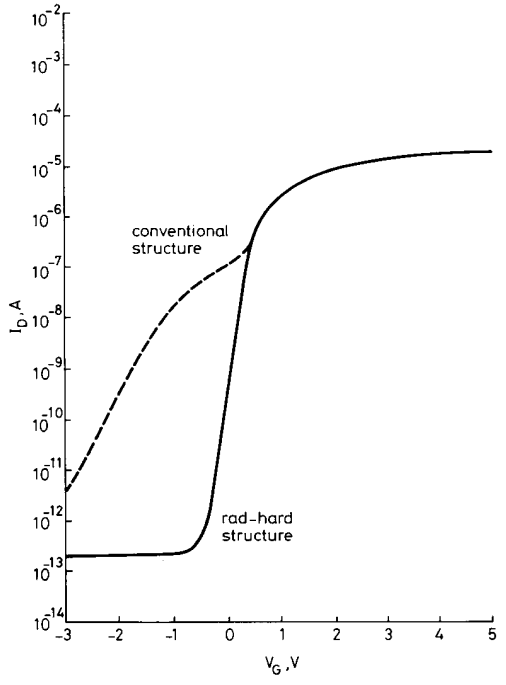

Fig. 5 *Postradiation subthreshold characteristics for structurally radiation hardened and conventional bulk NMOS transistors*

γ-ray total dose = 3×10^5 rad (Si)
Radiation bias: $V_G = 5$ V
Bulk NMOS: $W/L = 10\ \mu m/3\ \mu m$
$V_D = 0.1$ V

shows a postradiation subthreshold leakage current comparison between a structurally radiation hardened NMOS transistor and a conventional one. 3×10^5 rad(Si) total dose γ ray was irradiated to transistors with a 5 V gate bias. Marked improvement in postradiation leakage increase prevention in the new transistor is shown in Fig. 5.

A guard band structure was also successfully introduced to suppress the latter radiation induced field leakage. Fig. 6 shows a radiation hardened basic cell for radiation tolerant gate arrays. A buried P^+ diffusion layer was introduced under the polySi layer at the P well edge [32, 33].

2.4 Circuit technology for hardening

Since negative threshold voltage shifts due to radiation reduce postradiation PMOS drive current, NAND circuits should be used instead of NOR circuits, in which PMOS transistors are connected in series, in radiation hardened VLSI designs [23, 39]. From the point of view of obtaining a maximum circuit noise margin for the radiation tolerance, NAND and NOR CMOS logic circuits were studied by optimising β ratio and threshold voltage, based on the transistor parameter shift data due to radiation effects. The obtained results indicate high noise immunity, high packing density and high speed superiority of NAND to NOR in radiation hardened VLSI circuits. Fig. 7 shows worst case transfer characteristics for optimised, NAND and NOR CMOS/SOS circuits for radiation tolerance.

The limitations of dynamic circuits in radiation tolerant circuit designs were also investigated, compared with static circuits [36, 37]. Figs. 8 and 9 show postradiation functional frequency limits for static and dynamic CMOS shift register circuits, respectively. The results indicate that both the maximum frequency decrease due to threshold voltage shift and the minimum frequency increase due to radiation induced leakage determine the useful radiation level in dynamic circuits.

Furthermore, radiation tolerance superiority of clocked gate CMOS circuits to transfer gate CMOS circuits was discussed, in Silicon On Sapphire (SOS) devices, placing emphasis mainly on radiation bias effects [40]. Figs. 10 and 11 show worst case radiation bias conditions for a CMOS transfer gate and a clocked CMOS circuit, respectively. Since worst radiation bias for clocked gate CMOS circuits is half of that for transfer gate CMOS circuits, the maximum threshold voltage shift in clocked gate circuits is smaller than that in transfer gate circuits. Therefore, actual degradation in clocked gate CMOS circuits can be considered to be smaller than that in transfer gate CMOS circuits for the same total dose.

3 Latch-up hardening

In CMOS devices, latchup phenomena are induced by turning on of parasitic SCR. By transient radiation or a single charged particle irradiation, latchup is induced, not only in I/O circuits but also in internal circuits. The continued reduced scaling of devices will exacerbate parasitic effects, such as latchup. In radiation tolerant bulk CMOS circuit designs, latchup is fatal. Therefore, latchup prevention is essential for radiation tolerant CMOS VLSI realisation.

The latchup free condition can be realised when latchup holding voltage is higher than the power supply voltage. Latchup holding voltage is the turning point in the latchup I–V curve, which occurs when the internal positive feedback loop gain of the PNPN structure decreases below unity as the supply voltage is decreased. Utilising a curve tracer, latchup characteristics for six different radiation hardened structure introduced CMOS

circuits were measured and investigated [38]. Epitaxial substrate introduction realised a 7.0 V latchup holding voltage. The result indicates that epitaxial layer substrate introduction is a solution to 5 V supply voltage circuits pletely latchup free. Therefore, epitaxial or SOI and SOS substrate introduction is a realistic solution for latchup free CMOS VLSI circuits, which does not sacrifice the packing density.

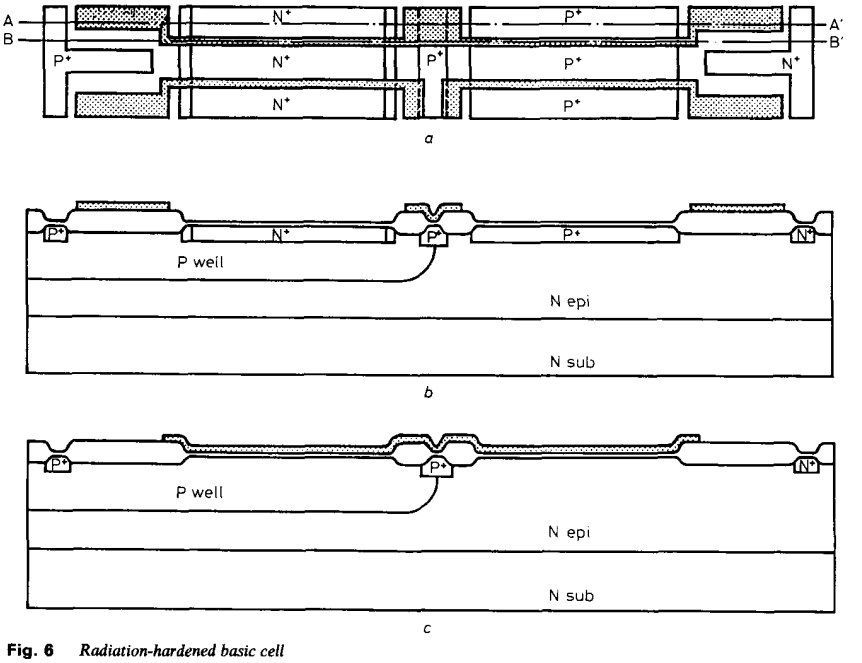

Fig. 6 *Radiation-hardened basic cell*
a Top view
b *A–A* cross section
c *B–B* cross section

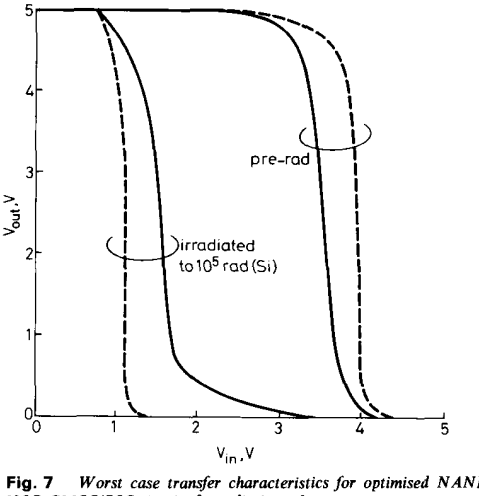

Fig. 7 *Worst case transfer characteristics for optimised NAND and NOR CMOS/SOS circuits for radiation tolerance*
DC noise immunity of 1.5 μm optimised NAND CMOS logic circuit for radiation tolerance is 36% greater than for NOR, $L_{eff} = 1.5$ μm
——— 3-input NAND
– – – – 3-input NOR

latchup prevention. A marked improvement in latchup resistance with decreasing epitaxial layer thickness was also reported [41].

Since SOI (Silicon On Insulator) devices, and SOS devices have no parasitic SCR, these devices are com-

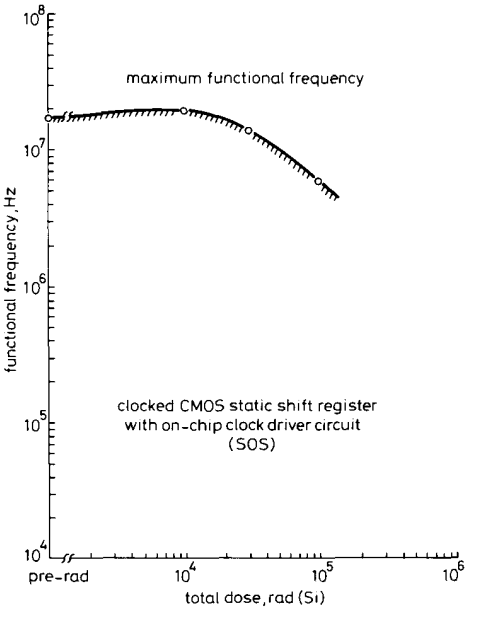

Fig. 8 *Maximum functional frequency at 5 V for clocked CMOS static shift register with onchip clock driver circuits as function of γ-ray total dose*

4 Single event upset hardening

In the galactic cosmic ray environment typical of high altitude satellite orbits, a single event upset (SEU), which occurs when a charged particle passing through a cell deposits enough energy for the cell to change its state, should be taken into account. The continued reduced scaling of devices will also exacerbate this effect.

When the device surface area decreases, without scaling device dimensions, the number of particles passing through decreases, maintaining the critical charge constant [40]. For the same design rules, layout area for a clocked gate CMOS shift register circuit was found to be smaller than for a transfer gate CMOS shift register circuit, as shown in Fig. 12. Therefore, the upset rate for clocked gate CMOS shift registers can be considered to be smaller than for transfer gate CMOS shift registers.

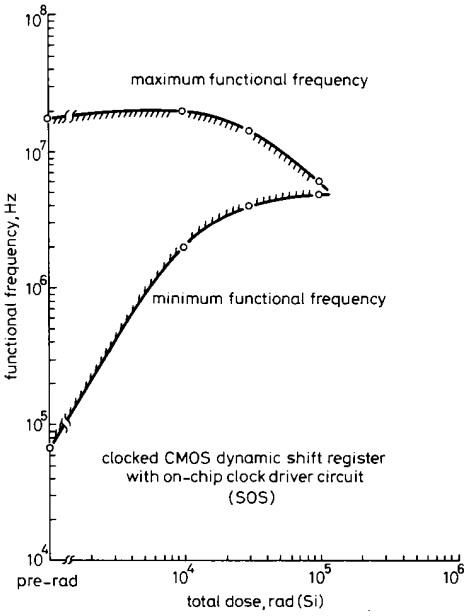

Fig. 9 *Maximum and minimum functional frequency at 5 V for clocked CMOS dynamic shift register with onchip clock driver circuits as function of γ-ray total dose*

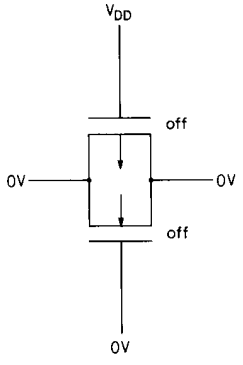

Fig. 10 *Worst case radiation bias condition for CMOS transfer gate*
When transfer gate is cut off after data 0 transferred, and next data 0 introduced, supply voltage V_{DD} effectively applied to PMOS/SOS gate, since SOS transistor substrate is electrically floating

The wide gate width transistor introduction also shows to be effective for SEU protection. CMOS gate arrays are generally immune to SEU, because of wide gate cell transistors [33].

Decoupling resistor introduction into memory cells or logic circuits is well known to be useful in SEU immune VLSI designs [42, 43]. Fig. 13 shows the six transistor CMOS static RAM cell with decoupling resistor. This cell design is utilised for 16k, 64k and 256k CMOS SRAM hardening [44–47]. Resistors were also introduced in latch designs for 8 bit, 16 bit and 32 bit microprocessor hardening [43, 48].

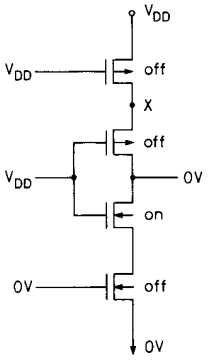

Fig. 11 *Worst case radiation bias condition for clocked CMOS circuit*
When clocked gate is cut off after data 0 transferred, and next data 1 is applied to inverter input gate, voltage at intermediate node, X, is about (1/2) V_{DD}. Since SOS transistor substrate is electrically floating, each substrate potential is equal to each source potential. Worst case PMOS effective gate bias is (1/2) V_{DD}

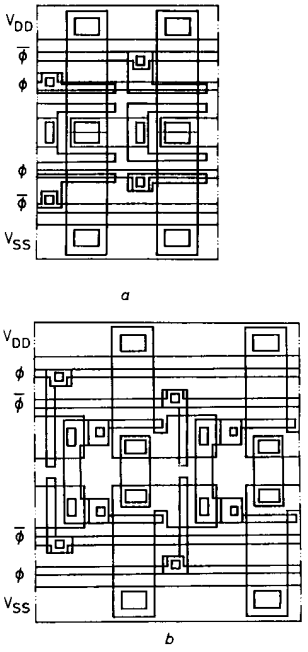

Fig. 12 *CMOS/SOS dynamic shift register circuit layout for same design rule*
a Clocked gate
b Transfer gate
Packing density of clocked gate CMOS shift register is about 1.7 times greater than that of transfer gate CMOS shift register

The design of a CMOS data latch that can withstand single particle hits without logic upset, was reported [49]. Since the hardness against upset is achieved solely by virtue of the design, no fabrication process development for resistor is required.

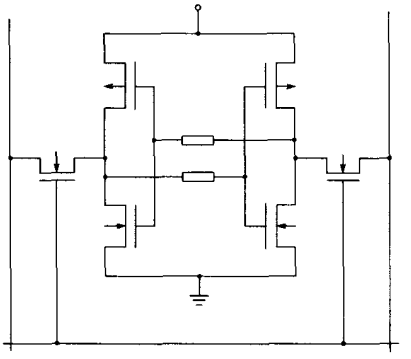

Fig. 13 *SEU immune six transistor CMOS static RAM cell with decoupling resistor*

Since SOS and SOI devices have reduced pn junction area, SOS and SOI devices are well known to be immune to SEU. A 64k SOS SRAM and a 64k SIMOX SRAM demonstrated the effectiveness of SOS and SOI devices [50, 51].

In addition to chip level SEU hardening, fault tolerant redundancy systems are usually introduced for space satellite applications. After investigation for the necessary number of CPUs to establish a high reliable onboard computing system, four 16 bit microprocessors were reported to be employed in a next generation satellite with 10 years of mission life, for successful execution of missions that will be imposed in the 1990s [52].

5 Radiation-hardened CMOS VLSIs

5.1 Radiation-hardened CMOS/SOS VLSIs

CMOS/SOS technology, combined with the radiation hardened process, is ideal for use in radiation tolerant VLSI designs because SOS devices have no parasitic SCR structure and no parasitic field transistor and because they have reduced pn junction area.

A 64k radiation hardened CMOS/SOS static RAM [50] was presented in 1989 Nuclear and Space Radiation Effects Conference. A six transistor memory cell was employed. A 256 channel C^2 MOS/SOS satellite time switch LSI for digital telecommunication switching, was designed [53].

The features used in the 256 channel time switch LSI hardening were as follows. The initial NMOS and PMOS threshold voltages were set to be $+1.3$ V and -0.5 V, respectively. Moreover, circuit dimension optimisation was carried out for -0.8 V NMOS threshold voltage shift and -1.0 V PMOS threshold voltage shift. The ratio of PMOS transistor width to NMOS transistor width was determined, so that the preradiation signal data fall time should be equal to the postradiation signal data rise time [37]. Clocked gate CMOS circuits and NAND logics were successfully introduced, instead of transfer gate CMOS circuits and NOR logics, respectively. Total dose radiation test results showed the possibility of >10 MHz operation VLSI circuits at 5 V after radiation doses in excess of 10^5 rad (Si).

5.2 Radiation-hardened bulk CMOS VLSIs

A 256k radiation hardened bulk CMOS SRAM was successfully developed [46, 47]. A 10k gate radiation hardened CMOS gate array was also developed [33]. By personalising the 10k gate radiation hardened gate array, a 16 bit microprocessor for a space satellite with 10 years of mission life was successfully developed [52]. NOR gates were suppressed to use in this chip design [32]. Moreover, a 32 bit radiation hardened microprocessor was reported [48].

The features used in the 10k gate CMOS gate array hardening were as follows. A total dose of 100k rad (Si) radiation hardness was realised by introducing a thin field oxide between the source/drain diffusion layers and a thick field oxide in NMOS transistors both in basic cells and I/O cells, and a buried P^+ diffusion layer at the P well edge in basic cells without sacrificing speed performance. NMOS and PMOS gate lengths in basic cells were 2 μm, and the gate widths were 36.9 μm and 38.5 μm, respectively. The wide gate width transistor introduction is effective for SEU protection. The chips were fabricated with a gate oxide thickness of 250 Å using Si gate Epi CMOS technology.

6 Conclusions

For space or nuclear plant applications, radiation tolerant high performance CMOS VLSI circuit designs, utilising scaled CMOS/SOS technology and scaled bulk CMOS technology, have been reviewed, placing strong emphasis on total dose radiation hardness.

Process, device, and circuit technologies for total dose radiation hardening have been discussed, based on radiation induced degradations for logic threshold in a CMOS inverter, logic delay in a CMOS ring oscillator, balance operation in a CMOS current mirror sense amplifier, and write/read operation in a six transistor Flip Flop CMOS memory cell.

Low temperature process and thin oxide introductions have been shown to be effective for radiation induced threshold voltage shift reduction. Total dose radiation induced field leakage is suppressed by introducing a thin field oxide between the source/drain diffusion layers, and a thick field oxide in NMOS transistors, combined with the buried P^+ diffusion layer at the P well edge, without sacrificing speed performance.

In addition to process and device technologies for total dose radiation hardening, usefulness for NAND logics and static circuits in radiation tolerant CMOS VLSI designs have been shown. Furthermore, radiation tolerance superiority of clocked gate CMOS circuits to transfer gate CMOS circuits in SOS devices, have been indicated.

Latchup immunity and SEU immunity have also been discussed for both SOS and bulk devices.

Based on above mentioned investigations, radiation hardened CMOS/SOS VLSIs, and radiation hardened bulk CMOS VLSIs have been successfully developed.

The entire work described in this paper has made it possible to design radiation hardened high performance VLSI circuits for space or nuclear plant applications, utilising both CMOS/SOS and bulk CMOS technology.

7 Acknowledgment

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paper were performed at the Semiconductor Device Engineering Laboratory (SDEL), Toshiba Corporation, sponsored by the National Space Development Agency of Japan.

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