Multiple-Valued Logic in FPGAs

Zeljko Zilic and Zvonko G. Vranesic

Department of Electrical and Computer Engineering
University of Toronto

Abstract

This paper considers the applicability of multiple-valued logic (MVL) circuits in implementation of field-programmable gate arrays (FPGAs). It proposes an FPGA logic block architecture that features MVL current-mode CMOS circuitry. The logic block combines the lookup-table and multiplexer approaches found in commercial FPGAs, and provides additional versatility through its current-mode operation.

1.0 Introduction

Field Programmable Gate Arrays (FPGAs) are rapidly becoming a popular choice for implementation of digital circuits where quick turn-around time and low cost are important considerations. They are replacing the more traditional application-specific integrated circuits (ASICs) in a growing number of applications. The disadvantages of FPGAs are primarily due to lower density and speed, in comparison with ASICs and mask-programmable gate arrays.

Both speed and density in FPGAs are affected by the structure of the logic blocks and the interconnect between them. The interconnect is of particular importance because it can occupy as much as 75 percent of the chip area [1], [4]. While all existing FPGAs are based on binary circuits, it is interesting to consider the possibility of using multiple-valued logic (MVL) circuits instead. In particular, it may be attractive to use current-mode CMOS technology for this purpose. Current-mode circuits may result in significant speed improvements, while the use of MVL signals may reduce the size of the interconnect. A recent study gives an example of improved speed in the case of a typical SRAM bit-line, where a delay was found to be 5 ns for conventional voltage-mode operation and less than 0.3 ns for current-mode signals [8].

This paper presents an attempt to investigate the possibility of exploiting MVL circuits in the FPGA environment. Its main purpose is to motivate future work in this direction, by discussing the feasibility of MVL logic blocks and their impact on the architecture of FPGAs.

2.0 Current-Mode MVL Circuits

Recent experience shows that current-mode circuits are attractive for implementation of MVL functions. Most of the circuits and synthesis techniques in the literature have been intended for the 4-valued (quarternary) environment [2], [7]. Current-mode circuits offer several advantages, but they also have some disadvantages. Perhaps the most important advantage is the ease of summation of signals, while the main difficulty lies in the signal distribution limitations caused by the natural fanout being equal to one. In practice, it is useful to augment the current-mode circuits with some intermediate voltage-mode circuits, which often results in more effective designs. Figure 1 gives the basic blocks used in our design. All of these blocks have been used before [2], [7], [9]. Here, we will only summarize their characteristics.

Currents are summed by means of a simple wired connection. Current sources are realized as an N-type or a P-type transistor with the gate connected to a reference voltage. The amount (value) of current is proportional to the ratio of W/L. Signal distribution can be performed using *current mirrors*, which can be of either N-type or P-type. We will use both types. The current produced at the output is determined by the input current and the ratio of the W/L values of output and input transistors. In addition to signal distribution, the current mirror can be used for multiplication with a constant and for sign reversal. A *threshold detector* block takes a multiple-valued input current signal and produces a voltage signal. The output signal is High if the input exceeds a predefined reference value; otherwise the output signal is Low. Threshold detectors generate signals that can be used with normal binary logic gates and for control of pass-transistor networks. A *pass transistor* is a voltage-controlled device, which enables or disables the

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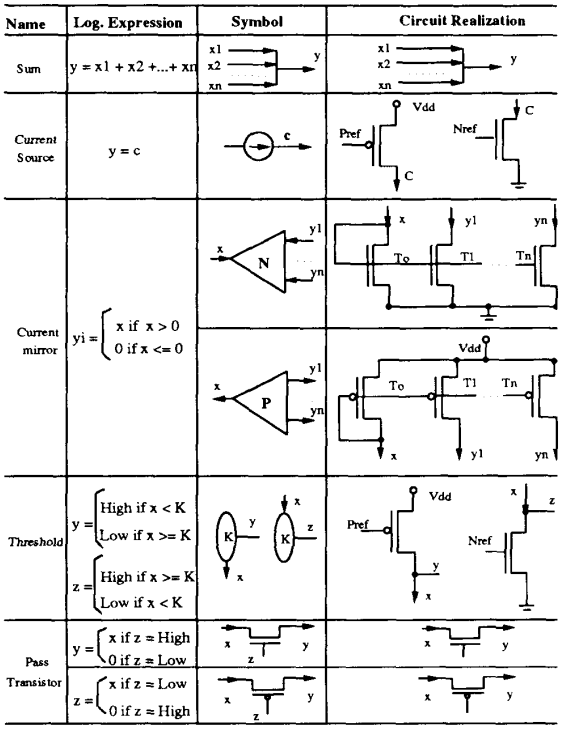
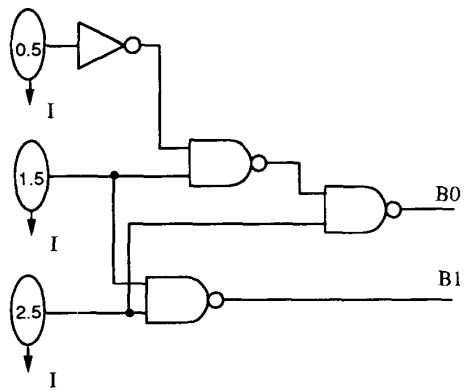
current flow, depending on the gate voltage. We will use both N and P-type pass transistors.

FIGURE 1. Basic Current Mode Blocks



As an example of how these primitives are used, a converter from quaternary current mode to binary voltage-mode signals is shown in Figure 2. The input current to the threshold comparators is distributed by the n-type current mirror.

FIGURE 2. Quaternary to Binary Converter



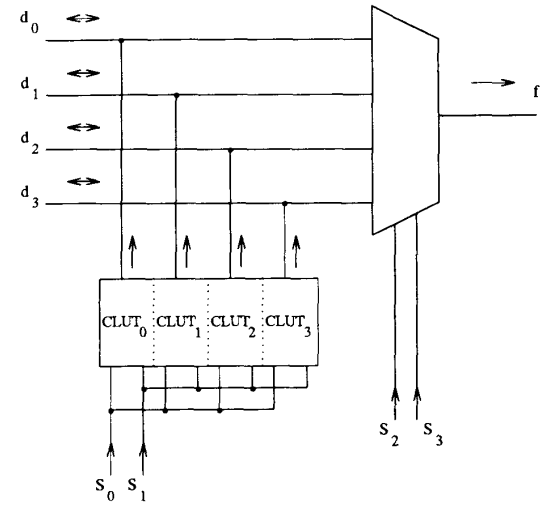
3.0 MVL in FPGA Environment

Our goal is to investigate how beneficial it is to use current mode CMOS MVL for FPGAs and to propose an architecture that will exploit the useful properties of such technology. An FPGA consists of a number of *logic blocks* interconnected by a flexible routing structure. Two of the most popular types of logic blocks are lookup tables and multiplexer-based blocks. In the case of lookup tables with *k* inputs, *LUTk*, each logic block can perform any k-variable function, while the multiplexer-based blocks can perform a limited set of functions, defined by the multiplexer size and the amount of additional logic in the logic block. Each of these basic blocks has its advantages and disadvantages and it is not clear which approach is better.

In order to exploit the advantage of using MVL and to avoid its demerits, we think that the FPGA architecture should employ both binary voltage and 4-valued current-mode signals. Current signals should be used when the fanout of one is needed. This is often the case in practice. Indeed, our examination of a set of practical FPGA designs showed that about 50 percent of the interconnection lines had the fanout equal to one. When a larger fanout is needed, we suggest the use of voltage-mode signals.

3.1 Proposed MVL Logic Block Architecture

FIGURE 3. Current Mode Logic Block- the Idea

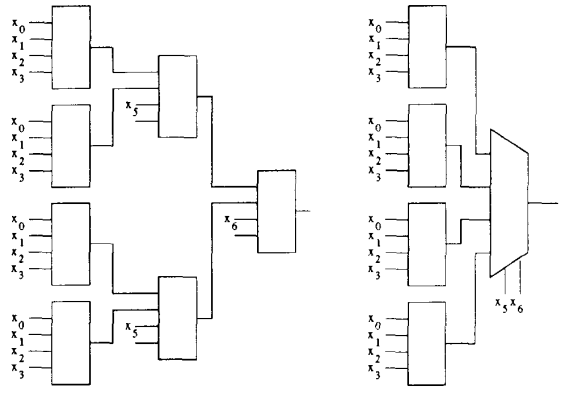


Many studies have investigated the effectiveness of the FPGA logic block architectures and it is believed that the lookup table and the multiplexer-based blocks are both reasonable choices. We are proposing an architecture which combines these approaches. The essence of our

scheme is illustrated in Figure 3. The block contains 4 lookup tables, $CLUT_{0-3}$, which generate 4-valued current-mode outputs. The entries in the lookup tables are selected using the binary voltage-mode signals, s_0 and s_1. The outputs of the CLUTs are connected to lines d_{0-3}, which can be used as both inputs and outputs to/from the block. A 4-to-1 multiplexer selects as output f one of the four current-mode signals, comprising the sum of the current input d_i and the output of $CLUT_i$. Binary voltage-mode signals s_2 and s_3 determine the multiplexer choice. To differentiate between the two types of signals in the figure, we use arrowheads on the lines that carry voltage-mode signals and arrowheads adjacent to lines that carry current-mode signals.

The logic block in Figure 3 can be used in a number of different ways. The extreme possibilities are to use it either as a pure lookup table, or as a pure multiplexer. The former results when the lines d_{0-3} are not used as external connections, in which case the block functions as a 4-input lookup table where the inputs are s_{0-3}. The latter arises when $CLUT_{0-3}$ generate zero output currents and the lines d_{0-3} are used as inputs. Thus, the block behaves simply as a 4-to-1 multiplexer. Between these extremes, there are different possibilities for exploiting the functionality of the lookup tables, the lines d_{0-3} , and the multiplexer.

FIGURE 4. Expandabillity with and without Multiplexer

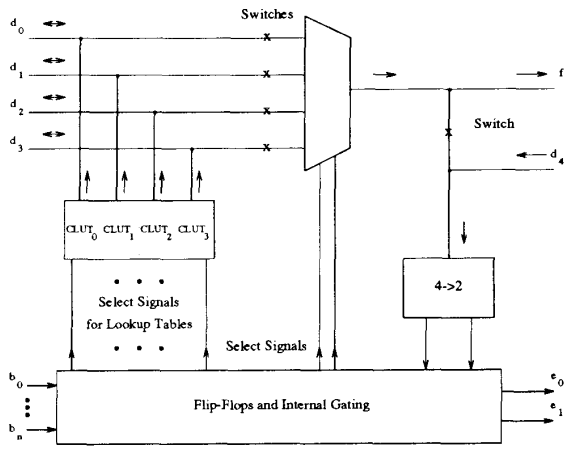


Combining a multiplexer and a lookup table in the logic block allows easy expansion of functions. If the logic block consists of only a lookup table, it is awkward to synthesize functions that have more variables than the size of the table. For example, in an FPGA consisting of LUT4 logic blocks, any 6-variable function can be realized as shown in Figure 4a. The difficulty lies in the fact that one LUT4 can perform the function of only one 2-input multiplexer. However, if the multiplexer is available as part of the logic block, the same 6-variable function can be implemented as indicated in Figure 4b. This implementation requires five logic blocks of the type shown in Figure 3.

A possible basic block is depicted in Figure 5. It comprises the circuit in Figure 3 (which includes four current mode lookup tables), a circuit that converts a 4-valued current signal into two binary voltage signals (given in Figure 2) and flip-flops to facilitate implementation of sequential circuits.

Instead of connecting the select inputs for CLUTs together, as in Figure 3, it is better to have separate select inputs for each table in order to provide greater flexibility in using the CLUTs. This is similar to the approach used in ORCA FPGAs produced by AT&T company [5], [6] where the equivalent of d_{0-3} lines are used as outputs only. The logic block also includes the current input d_4, connected to the *4->2* converter. The output voltage-mode signals of this converter may be used as control signals within the block, but they may also be available as outputs from the block, on lines e_0 and e_1. We note that the converter can also be used conveniently for signal-level restoration purposes. This is useful in view of the fact that MVL-signal levels may deteriorate when a number of MVL elements are connected in series. Voltage-mode inputs to the block are provided on lines b_{0-n}.

FIGURE 5. Current Mode Logic Block- Detailed Schematics



It is not clear at present time what the size of CLUTs should be. The number of select lines and the degree of sharing of the select lines should be investigated.

4.0 Performance Estimate

The proposed logic block offers rich possibilities in implementing general logic functions. At present time we do not have the tools that would enable us to assess its full capa-

bility on commonly used benchmark circuits. However, we attempted to evaluate the effectiveness of a much simplified binary version of this block, consisting of two-input lookup tables and a multiplexer. We used the library based mapper MIS [3] to map 15 MCNC benchmark circuits. Using the same mapping procedure, we then mapped the same circuits onto the closest lookup table, LUT3. Two kinds of mappings were performed - one optimizing the area and the other optimizing the delay. For both optimizing procedures, we compared the area and the delay. The results showed that, on average, our architecture needs 12.7 percent fewer blocks when then mapping is optimized for area and that implementations with our blocks are 10.9 percent faster, when the speed optimization is used. Of course, this simplified assessment does not take any advantage of the MVL capability of the block, but it does suggest that the basic structure is reasonable.

5.0 Concluding Remarks

We have proposed an FPGA logic block architecture that exploits the advantages of current-mode CMOS logic. We believe that the block offers a high degree of flexibility, compared to the types of blocks found in presently available FPGAs. The lack of synthesis tools has prevented us from doing a full evaluation of this architecture.

The main purpose of this paper is to present some new ideas about the possible use of both the current-mode and MVL techniques in the FPGA environment, and to encourage future work in this direction.

6.0 References

[1] Brown, S. D., Francis, R. J., Rose, J. and Vranesic, Z. G., *Field-Programmable Gate Arrays,* Kluwer Academic Publishers, 1992.

[2] Chang, Y. H. and Butler, J. T., *The Design of Current Mode CMOS Multiple--Valued Circuits,* Proceedings of the 21st ISVML, pp. 130-138, May 1991.

[3] Detjens, E. et. al, *Technology Mapping in MIS,* Proc. ICCAD 87, pp. 116-119, 1987.

[4] Ebeling, C., Boriello, G., Hauck, S. A., Song, D. and Walkup, E. A., *Triptych: A New FPGA Architecture,* in W. Moore and W. Luk (editors), "FPGAs", pp. 75-90, Abingdon EECS Books, Abingdon UK, 1991.

[5] Hill, D. and Woo, N. S., *The benefits of Flexibility in Look-up Table FPGAs,* in W. Moore and W. Luk (editors), "FPGAs", pp. 127-136, Abingdon EECS Books, Abingdon UK, 1991.

[6] Hill, D. D., Britton, B. B., Oswald, B., Woo, N. S., Singh, S., Poon, T. and Krambeck, B.*A New Architecture for High-Performance FPGAs,* Proc. Workshop on Field-Programmable Logic and Applications, Aug. 1992.

[7] Lei, K. and Vranesic, Z., *On the Synthesis of 4-Valued Current Mode Circuits,* Proceedings of the 21st ISMVL, pp. 147-155, May 1991.

[8] Seevinck, E., van Beers, P. J. and Ontrop, H., *Current-Mode Techniques for High-Speed VLSI Circuits with Applications to Current Sense Amplifier for CMOS SRAM's,* IEEE Journal of Solid-State Circuits, Vol. ***26*** No. 4, pp. 525-536, Apr., 1991.

[9] Zilic, Z and Vranesic, Z., *Current Mode CMOS Galois Field Circuits,* Proceedings of the 23rd ISMVL, May 1993.