Realization of Quaternary Logic Circuits by n-Channel MOS Devices

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Abstract — **A new method to implement quaternary circuits using NMOS devices is proposed. We have designed a simplified elementary form of inverter and have implemented a series of fundamental logic and memory circuits. These circuits are comprised of MOS transistors with three values of enhancement-mode threshold voltage and one depletion-mode threshold voltage. The features of these circuits are a small number of MOS transistors, a simple structure, and an exact transfer characteristic. Several fundamental circuits such as inverter, NAND, NOR, and delta literal have been fabricated by conventional NMOS technology. Comparisons between the measured and calculated results indicate a good agreement taking into account some back-bias effect. Performance of inverter including speed, noise margin, and pattern area is also discussed.**

I. Introduction

THERE HAS BEEN a marked increase in the scale and packing density of very-large-scale integration (VLSI). As the number of devices in a VLSI chip increases, the interconnection between active devices inside and outside a silicon chip becomes remarkably complicated and the area percentage occupied by interconnections increases rapidly. The need for a reduction in interconnections becomes more and more pressing. In this situation, there has been a continuous interest in the possibility of multiple-valued logic (MVL) as a solution for the above problems. The major advantages expected from MVL are: 1) reduced interconnection; 2) decreased number of bonding pads and package pins; and 3) increased packing density [1], [2]. Nowadays, the occupied area of interconnections is more than 70 percent of a chip area, and has been increasing.

Up to the present, the implementation of MVL has been studied by using various devices, such as I^2L [3], ECL [4], CCD [5], CMOS [6], NMOS [7], [8], and MESFET [8]. NMOS devices are superior both in speed and density and so are used more than any other device in the binary circuit field. However, only a few theoretical studies on MVL circuits using NMOS devices have been reported and, moreover, their main stress has been laid on ternary logic circuits [7], [8].

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In the present work, a new circuit structure to implement MVL circuits using NMOS devices is proposed. We have devised an elementary circuit form of inverter and designed a series of fundamental logic and memory circuits in the manner very similar to the binary circuits, based on the inverter structure, which enables us to realize ternary or quaternary circuits with full functionality. The present paper describes the construction, characteristics, and performance of quaternary logic and memory circuits. In order to transfer quaternary voltages accurately, enhancement-mode (*E*-mode) MOST's with three values of threshold voltage are used. The present new circuits have several advantages: a small number of MOST's, a simple structure, and an exact transfer characteristic, compared with those consisting of a single threshold voltage for *E*-mode MOST. Based on this concept, a system of quaternary logic circuits using NMOS devices has been implemented. Calculation and fabrication of quaternary inverter, NAND, NOR, and delta literal circuits have been performed. Measurement and calculation have proved the possibility of realization. Performance of inverter including static transfer characteristic, transient response time, and pattern area is discussed from the viewpoint of finding the optimum device parameters.

II. Design of Quarternary Logic Circuits

A. Simplified Forms of Fundamental Logic Circuits

Fig. 1 shows a quarternary inverter circuit, being an elementary form of various logic circuits proposed in the present paper. Circuit complexity has been reduced by using three values of *E*-mode threshold voltage and by utilizing a priority rule in establishing the output voltage. The inverter consists of five *E*-mode MOST's and one depletion mode (*D*-mode) MOST. In order to exactly transfer the four values of voltage, three values of *E*-mode threshold voltage, as indicated in Table I, are used. In this table, there is a correspondence between the magnitude of logic level value and of voltage value, so that a logic threshold value of 0.5 means a threshold voltage between voltages of logic level "0" and "1." Values of 1.5 and 2.5 have corresponding meanings. For a given input level, MOST's with threshold voltage levels smaller than the

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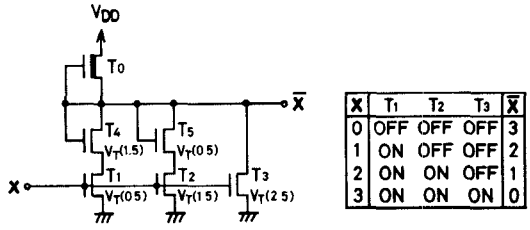


X	T1	T2	T3	X̄
0	OFF	OFF	OFF	3
1	ON	OFF	OFF	2
2	ON	ON	OFF	1
3	ON	ON	ON	0

(a) (b)

Fig. 1. A quaternary inverter: (a) circuit and (b) relationships among the input level, operation states of the input transistors, and the output level.

TABLE I
RELATION BETWEEN THE LOGIC VALUES (VOLTAGES) AND THE THRESHOLD VALUES (VOLTAGES) OF ENHANCEMENT-MODE MOST'S

Logic Value	0	1	2	3
Threshold Value of MOST		0.5	1.5	2.5

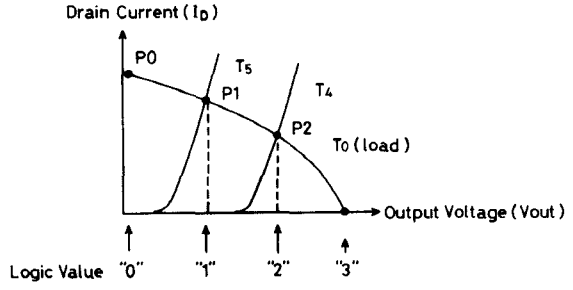
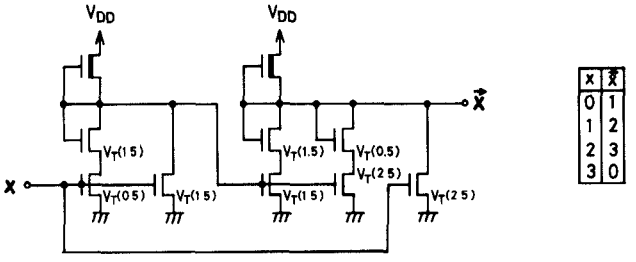


Fig. 2. Drain currents of the transistors associated with output in Fig. 1 as a function of output voltage, explaining the operation principle of the lowest output voltage priority.

input level are turned "on." In Fig. 1, the input level is distinguished by the three transistors (T_1, T_2, and T_3). On the output stage, voltages of logic levels "0" and "3" are the ground and power-supply voltages, respectively, while the two intermediate voltages of logic levels "1" and "2" can be obtained by voltage dividers consisting of one D-mode MOST (T_0) and one E-mode MOST (T_4 or T_5), connected in series. The threshold voltages of T_4 and T_5 are adjusted to levels of 1.5 and 0.5 (hereafter designated as $V_T(1.5)$ and $V_T(0.5)$), respectively.

The process of establishing output voltages is explained in Fig. 2, which shows the drain currents of T_0, T_4, and T_5 as a function of output voltage. The channel width-to-length (W/L) ratio in T_1, T_2, and T_3 is so large that the transistors can be regarded simply as switches. The relationships among the input level, operation states of T_1, T_2, and T_3, and the output level are listed in Fig. 1(b). It should be noted that the priority is given to the lowest level at all times when several driver transistors are in the ON state, as seen in Fig. 1(b) and Fig. 2. This operating principle in which the lowest level has priority leads not only to a marked decrease in transistor number and a simplification of layout pattern, but also to an exact transfer characteristic. A further merit of the circuit is a small power dissipation, resulting from a small number of load transistors.

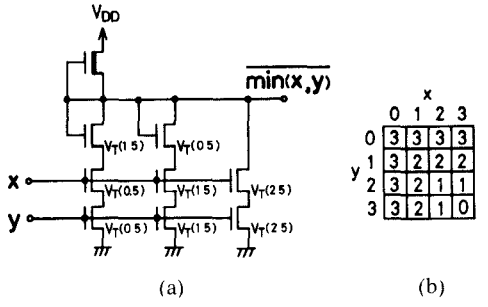
Fundamental quaternary logic circuits can be designed on the basis of the above standard form of inverter, exactly



X	X̄
0	1
1	2
2	3
3	0

(a) (b)

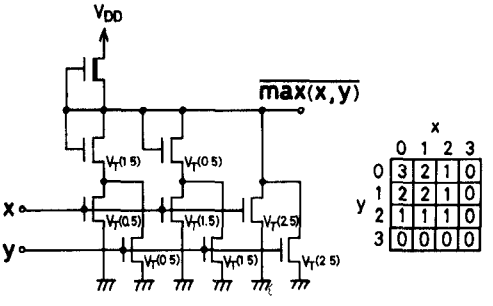
Fig 3 A quaternary successor: (a) circuit and (b) truth table.



y \ x	0	1	2	3
0	3	3	3	3
1	3	2	2	2
2	3	2	1	1
3	3	2	1	0

(a) (b)

Fig. 4. A quaternary two-input NAND: (a) circuit and (b) truth table.



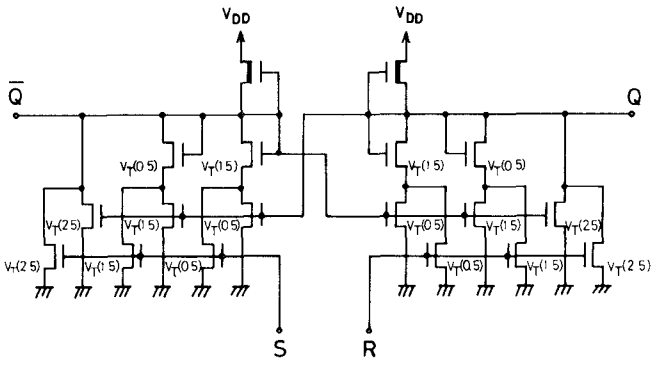
y \ x	0	1	2	3
0	3	2	1	0
1	2	2	1	0
2	1	1	1	0
3	0	0	0	0

(a) (b)

Fig. 5. A quaternary two-input NOR: (a) circuit and (b) truth table

similarly to the binary case. Fig. 3 shows a quaternary successor circuit. The truth table in Fig. 3(b) is realized by this circuit. Figs. 4 and 5 show quaternary NAND and NOR circuit structures for two inputs, respectively. These NAND and NOR circuits show the same input structure as their binary counterparts, in which the driver transistors for input are connected in series and parallel, respectively. Each of these circuits can be implemented by adding only three transistors to the inverter circuit. As the truth tables indicate in Figs. 4(b) and 5(b), the logic functions of NAND and NOR are $\overline{\min(x, y)}$ and $\overline{\max(x, y)}$, respectively. Consequently, if the inverter circuit in Fig. 1 is connected to each output, the logic functions of $\min(x, y)$ and $\max(x, y)$ can be obtained. The use of the above-mentioned fundamental circuits gives us any quanternary logic function, that is, full functionality [9].

Furthermore, quaternary memory circuits can be realized by using the inverter, NAND or NOR. The restoring circuit, which has the same output logic levels as the input levels, is formed by a series connection of two stages of inverters. This circuit can be used as components of dynamic memory, buffers, and so forth. A quaternary static

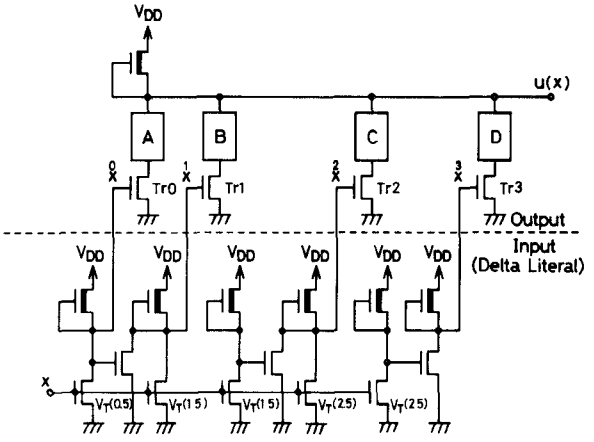


(a)

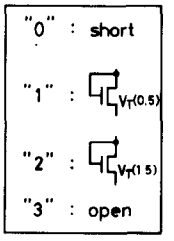
S \ R	0		1		2		3	
	Q^{n+1}	$\overline{Q^{n+1}}$	Q^{n+1}	$\overline{Q^{n+1}}$	Q^{n+1}	$\overline{Q^{n+1}}$	Q^{n+1}	$\overline{Q^{n+1}}$
0	Q^n	$\overline{Q^n}$	$1 \vee Q^n$	$\overline{1 \vee Q^n}$	$2 \vee Q^n$	$\overline{2 \vee Q^n}$	3	0
1	$2 \cdot Q^n$	$\overline{2 \cdot Q^n}$	$2 \cdot Q^n \vee 1$	$\overline{2 \cdot Q^n \vee 1}$	2	1	2^x	0^x
2	$1 \cdot Q^n$	$\overline{1 \cdot Q^n}$	1	2	1^x	1^x	1^x	0^x
3	0	3	0^x	2^x	0^x	1^x	0^x	0^x

(b)

Fig. 6. A quaternary *RS* flip-flop circuit using NOR circuits in Fig. 5: (a) circuit and (b) truth table. In the truth table, symbols "$\vee$" and "$\cdot$" denote OR ($\max(x, y)$) and AND ($\min(x, y)$), respectively. States signed by symbol "$\times$" indicate forbidden states.



(a)



(b)

Fig. 7. A generalized form of quaternary unary function circuit. The input part is a delta literal circuit. Respectively desired connections of *A*, *B*, *C*, and *D* of the output part in (a) are indicated in (b)

random access memory (RAM) is constructed by cross-coupled interconnections between input and output terminals in two inverters, similarly to the binary static RAM. Quaternary flip-flop circuits are also constructed by cross-coupled NAND (Fig. 4) or NOR (Fig. 5) circuit. Fig. 6 illustrates the quaternary *RS* flip-flop circuit and its truth table using the NOR circuit in Fig. 5. The truth table follows the same expression as the binary *RS* flip-flop, $Q^{n+1} = S + \overline{R} \cdot Q^n$. The interconnection between the two NAND circuits is the same as in Fig. 6, as well. These circuits are useful and important in register, shift register, and counter applications.

It is emphasized that all logic and memory circuits necessary to quaternary integrated circuits are formed on the basis of inverter structure by following the same procedure as binary circuits. Furthermore, it should be noted that the principle in construction of the inverter structure can be applied to implement every MVL circuit, that is, ternary, quaternary, and so forth.

B. Unary Function Circuits for General Use

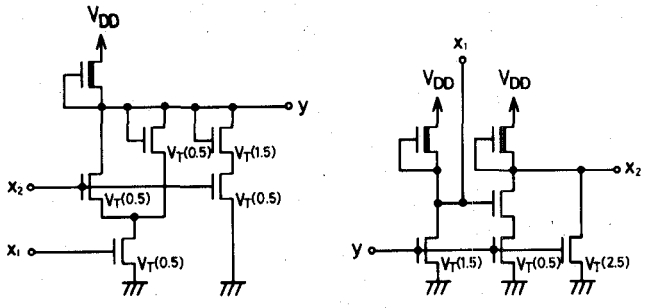
The implementation of arbitrary unary functions is indispensable in constructing MVL circuits [10]. There are $256 (= 4^4)$ kinds of functions. A generalized construct for these quaternary unary circuits is presented in Fig. 7. This circuit can be divided into input and output parts. The input part is a delta literal circuit. Kameyama *et al.* [11] have also described the same delta literal circuit.

The circuit comprises *E*-mode MOST's with three or four values of threshold voltage and *D*-mode MOST's having a single threshold. Threshold voltages of $V_T(0.5)$, $V_T(1.5)$, and $V_T(2.5)$ indicated in Fig. 7 are the same as used above. The fourth kind of MOST's, in which the threshold voltage is not indicated, can have any threshold voltage between $V_T(0.5)$ and $V_T(2.5)$, but the use of $V_T(0.5)$ proves the most desirable in decreasing the geometrical β ratio. The output levels of $x^0 - x^3$ appear in accordance with the truth table in Table II. The output of level "3," corresponding to the power-supply voltage V_{DD}, appears in particular input ranges between 0, $V_T(0.5)$, $V_T(1.5)$, $V_T(2.5)$, and V_{DD} for the lines of x^0, x^1, x^2, and x^3, respectively. These output lines are connected to the gate electrodes of $Tr_0 - Tr_3$ in the output part, which act as switches. In accordance with the desired output levels, the connections indicated in Fig. 7(b) should be made in the positions $A - D$. By using this general form, any desired unary function can be designed.

TABLE II
TRUTH TABLE OF A QUATERNARY DELTA LITERAL

Input	Output			
x	x^0	x^1	x^2	x^3
0	3	0	0	0
1	0	3	0	0
2	0	0	3	0
3	0	0	0	3

The inverter circuit in Fig. 1 is one of the circuits equivalent to the output circuit in Fig. 7 because the circuit to be connected for the "open" case (level "3" case) can be eliminated. That is, the circuit elements for logic levels "2," "1," and "0" in Fig. 7(b) are set in the positions *B*, *C*, and *D* in Fig. 7(a) and the circuit corresponding to the position



Binary		Quaternary
X_1	X_2	y
1	1	0
1	0	1
0	1	2
0	0	3

(c)

Fig. 8. Converters between binary and quaternary signals: (a) encoder circuit, (b) decorder circuit, and (c) truth table. The voltage for binary logic level "1" corresponds to the voltage for quaternary logic level "3," which is the power-supply voltage V_{DD}.

A is eliminated. In this circuit, twenty MOST's are necessary. Compared with Fig. 1, it can be seen that the inverter and its family circuits mentioned above are remarkably simplified by utilizing the principle of priority in establishing the output level. The appropriate combination use of both styles of circuits gives us the increase in design flexibility.

C. Combination Use with Binary Circuits

Fig. 8 shows decoder and encoder circuits for such conversion between binary and quaternary, as in the truth table in Fig. 8(c), in which binary voltages corresponding to logic levels "0" and "1" are the ground and power-supply voltages, respectively. These circuits are also formed on the basis of the ideas proposed in Fig. 1. As seen in the next section, the quaternary circuits mentioned above and these conversion circuits can be fabricated by typical binary NMOS processes. Process compatibility enables us to fabricate both binary and quaternary circuits on one silicon chip and, thus, to utilize effectively the combination of both types of circuits. We can consider one-chip circuits to decode the quaternary signals into binary signals, process them by using binary circuits, encode into quaternary signals, and return to the quaternary circuits.

III. Evaluation by Fabrication and Simulation

A. Device Fabrication Procedure

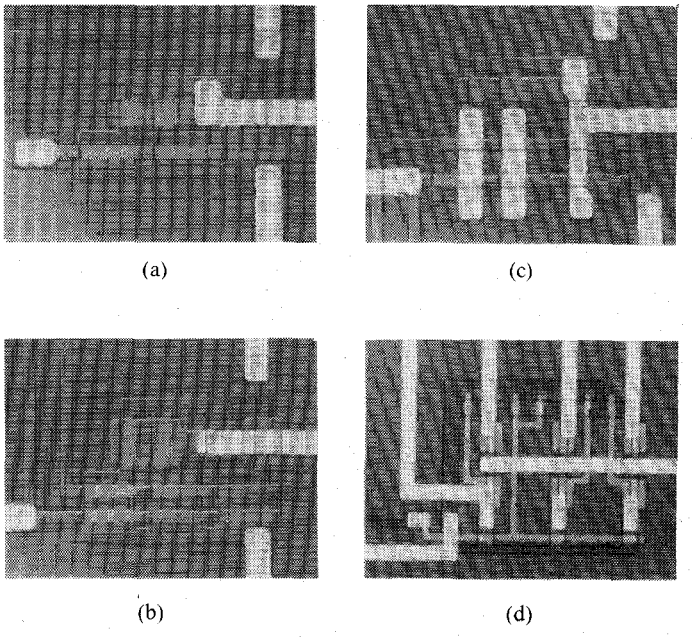
In order to identify all sorts of problems in the realization of the circuits proposed, we have fabricated the logic circuits including the inverter, NAND, NOR, and delta literal. The fabrication process used was the same as for a typical

TABLE III
Fabrication Process Conditions of the NMOS Quaternary Devices

Transistor	E-mode(1)	E-mode(2)	E-mode(3)	D-mode
Ion Implantation	Boron			Phosphorus
Dose (cm^{-2})	2.5×10^{11}	2.0×10^{12}	6.3×10^{12}	3.2×10^{11}
Threshold Voltage (V)	2.0	4.2	7.5	-3.5

Substrate: p-type(100), 6~12Ω-cm

Gate Oxide: 1000~1150Å



(a) (c) (b) (d)

Fig. 9. Optical micrographs of quaternary logic circuit patterns fabricated on a silicon chip: (a) inverter, (b) NAND, (c) NOR, and (d) delta literal. These patterns correspond to Figs. 1, 4, 5, and the input part in Fig. 7, respectively.

binary NMOS process, except for the addition of two processes of boron implantation to obtain three values of E-mode threshold. The process used was a silicon-gate NMOS process using the local oxidation technique for field oxide, and is described briefly here. Five types of ion implantations were carried out: one for the field region with boron, three for E-mode threshold voltages with boron, and one for the D-mode threshold voltage with phosphorus. The field oxide, about 1 μm thick, was grown at 1000°C by a local oxidation technique using a plasma-assisted CVD film of Si_xN_y as an oxidation mask. The gate oxide, 0.1 μm thick, was formed at 1000°C. The n^+-doped layers were diffused with phosphorus at 1040°C. Nine photolithography steps were necessary including Al interconnection patterning. Typical device parameters fabricated are listed in Table III.

Fig. 9 shows optical micrographs of the inverter, NAND, NOR, and delta literal circuit patterns fabricated on a silicon chip. It can be seen that the layout patterns are very simple and have easily understandable structures corresponding to the circuit diagrams of Figs. 1, 4, 5, and 7. This feature is one of the necessary conditions required in VLSI fabrication.

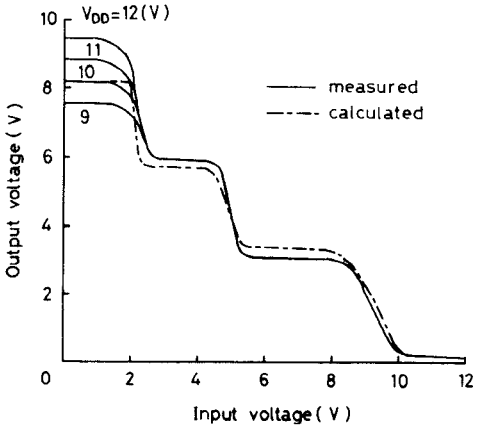


Fig. 10. A comparison between calculated and measured transfer characteristics of such the inverter shown in Fig. 9(a). For the calculations device parameters listed in Table IV were used, which were the same values as those of fabricated devices. Measured characteristics are shown for several power-supply voltages.

TABLE IV
CIRCUIT PARAMETERS USED FOR THE CALCULATIONS OF INVERTER CHARACTERISTICS, BEING THE SAME AS THOSE OF FABRICATED DEVICES

Power supply Voltage		10.0V
Threshold Voltage	(E-mode)	$V_T(0.5)=2.0V$, $V_T(1.5)=4.2V$, $V_T(2.5)=7.5V$
	(D-mode)	$V_T(D)=-3.5V$
β Ratio		$(W/L)T_5/(W/L)T_0=1.5$ $(W/L)T_4/(W/L)T_0=1.0$ $(W/L)T_1,T_2,T_3/(W/L)T_0=8.0$

Note: Symbols used are identical to those in Fig. 1.

B. Comparison Between Measured and Calculated Characteristics

Fig. 10 shows measured and calculated transfer characteristics of the inverter in Fig. 1. The calculations were performed by SPICE-2, using device parameters in Table IV that were the same as those of fabricated devices in Fig. 9(a). On the other hand, measured characteristics from such the inverter shown in Fig. 9(a) are indicated for several power-supply voltages. A good agreement can be seen between both the characteristics. It is observed in this figure that the highest output voltage for logic level "3" is lower than the power-supply voltage. The lowering is found to become more marked with increasing power-supply voltage and is analyzed to be attributed to a substrate back-bias effect. That is, as the output voltage increases the p-n junctions between p-type substrate and n-type channel regions in the *D*-mode MOST's are increasingly reverse-biased, and the depletion layer width in the substrate side of the channel region increases in proportion to $(\phi_b + V_{out})^{1/2}$, where ϕ_b is the built-in potential of the p-n junction. This narrowing of the channel due to the back-bias effect brings about an increase in the threshold voltage of *D*-mode load MOST's and their cutoff at a source (output) voltage lower than the power-supply voltage. It can be considered that the cutoff phenomenon does not appear by increasing the implanted dose of n-type impurity. This increase, however, corresponds to the increase in the conductance of load MOST. Consequently, the β ratio of driver to load MOST must be increased, which results in an increase in the pattern area.

TABLE V
DEVICE PARAMETERS USED IN CALCULATIONS OF PERFORMANCE AT A SUPPLY VOLTAGE OF 5 V

Gate Oxide Thickness	700A
Power Supply Voltage	5V
Diffusion Resistance	20Ω/□
Gate Capacitance	4.9×10^{-4}pF/μm^2
Diffusion Capacitance	1.5×10^{-4}pF/μm^2
Lateral Underdiffusion	0.3μm
Junction Depth	0.5μm
Minimum Line width	4μm

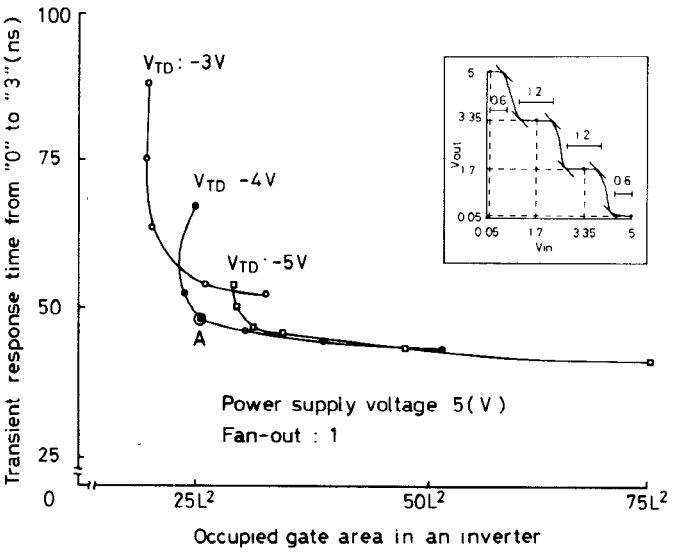


Fig. 11. Calculated correlation between occupied gate area in an inverter and the transient rise time from 0 V to the power-supply voltage of 5 V at a fan-out of 1 Each point corresponds to different W/L values of *D*-mode MOST under the condition of maintaining the transfer characteristic illustrated in the inset.

One of the most suitable solutions for this problem is to lower the power-supply voltage. Influences of the supply voltage on the transfer characteristics do not appear except for the highest output voltage, as seen in Fig. 10. In the next section, characteristics and performance of the inverter at a power-supply voltage of 5 V are evaluated.

C. Evaluation of Circuit Performance

Calculations on the inverter in Fig. 1 at a power-supply voltage of 5 V have been performed using SPICE-2 to evaluate the circuit performance and find out the optimized device parameters. Device parameters used in the calculations are shown in Table V, in which a 4-μm design rule was employed. Correlations between transient response time and occupied pattern area of inverters have been examined on the major premise that the desirable

TABLE VI
CALCULATED THRESHOLD VOLTAGES OF E-MODE MOST'S AND β RATIOS OF E-MODE TO D-MODE MOST FOR SEVERAL D-MODE THRESHOLD VOLTAGES, TO OBTAIN THE TRANSFER CHARACTERISTIC SHOWN IN THE INSET IN FIG. 11

V_{TD}(V)	$V_T(0.5)$ (V)	$V_T(1.5)$ (V)	$V_T(2.5)$ (V)	β_1	β_2	β_3	β_4	β_5
-3	0.61	2.2	3.7	22.6	31.9	37.7	7.1	6.1
-4	0.64	2.1	3.5	41.9	54.5	37.7	11.7	13.2
-5	0.65	2.2	3.3	58.7	104.8	41.9	19.5	19.3

Note: β_1–β_5 are $(W/L)T_1/(W/L)T_0$ to $(W/L)T_5/(W/L)T_0$, respectively. T_0 to T_5 are indicated in Fig. 1.

TABLE VII
A COMPARISON OF TRANSIENT RESPONSE TIMES FOR THE TRANSITION BETWEEN EVERY PAIR OF LOGIC LEVELS AT POINT A IN FIG. 11

		Logic Level after Transition			
		"3"	"2"	"1"	"0"
Logic	"3"		7.8ns	6.8ns	6.7ns
Level	"2"	37.5ns		9.2ns	5.2ns
before	"1"	39.5ns	21.0ns		5.0ns
Transition	"0"	48.0ns	24.0ns	20.5ns	

static transfer characteristic with high reliability shown in the inset in Fig. 11 can be obtained. This transfer characteristic has output logic level voltages of 5, 3.35, 1.70, and 0.05 V, which are divided the supply voltage of 5 V into three equal parts, and a noise margin of 0.6 V, for all operating points, in which the noise margin is defined as the voltage difference between the input operating points (0.5, 1.70, 3.35, or 5 V) and the nearest unity gain points ($dV_{out}/dV_{in} = -1$). The static transfer characteristic is perfectly determined by β ratios of the E-mode MOST's to the D-mode MOST and their threshold voltages. Table VI is the calculated results of the β ratios and E-mode threshold voltages for several D-mode threshold voltages.

Under the above conditions, the transient response time and occupied area of inverter depend on the W/L value of D-mode MOST. Fig. 11 indicates the correlation between the occupied gate area in an inverter and the transient rise time from 0 V (logic "0") to V_{DD} (logic "3") at a fan-out of 1 being the slowest of all transient rise and fall times between two operating points, for several D-mode threshold voltages. Each point in Fig. 11 corresponds to different W/L values of D-mode MOST, ranged from 2 to 14, under the condition of keeping the β ratios shown in Table VI. It can be seen that the occupied area increases with decreasing the response time. The product of both values has a minimum value at point A indicated in Fig. 11, which is related to an optimum condition. This condition corresponds to a threshold voltage of -4 V and a W/L value of 1/8 for the D-mode MOST and brings a response time of 48 ns and a gate area of $25L^2$ ($L = 4$ μm). Table VII shows transient response times for the rise and fall transitions between every pair of logic levels at point A in Fig. 11. These values calculated give us the suggestion that the realization of the quaternary logic circuits is possible, judging synthetically.

IV. SUMMARY

We have proposed a new system of quaternary circuits using NMOS devices and have confirmed that these circuits have various advantages suitable for VLSI fabrication through the processes of simulation, fabrication, and measurement. The main advantages are the small number of MOST's required, using simple layout patterns which allow direct comparison with circuit diagrams, and exact transfer characteristics. The construction of quaternary logic and memory circuits can be performed by the procedure exactly similar to that of binary circuits based on the inverter structure, and the quaternary system with full functionality can be realized. Furthermore, in order to implement more extensive quaternary circuits a general form of an arbitrary unary function as well as binary/quaternary decorder and encorder circuits has also been proposed. The present system has the potential both for extension and application.

A lowering of output voltage has been found in initially fabricated samples, arising from the substrate back-bias effect due to high-power-supply voltages near 10 V. On the other hand, calculations of performance including noise margin, transient response time, and occupied area give us the possibility of realization at a power-supply voltage of 5 V, in which practically satisfied performance has been obtained without lowering of output voltage. At present, with extending the above calculations various functional circuit blocks have been designed and fabricated using the circuit structures proposed in this paper.

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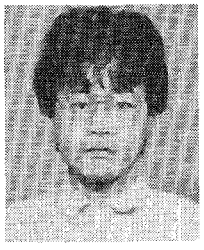

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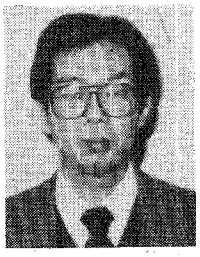

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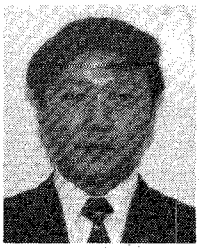

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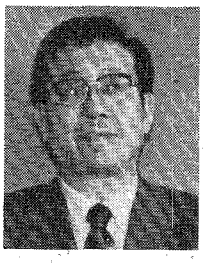

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