IV. Summary

In summary, we have presented the results on the performance of 0.25-μm gate-length AlGaN/GaN HEMTs with varying field-plate length. These devices exhibited high current densities of more than 1.4 A/mm and peak extrinsic transconductances of more than 430 mS/mm. DC I–V as well as transfer characteristics were essentially independent of the length of the field plate, but there was significant improvement in breakdown voltage as the length of the field plate increased. With increase in field-plate length, degradation in the values of f_T and $f_{\max}$ was observed, but there was significant improvement in power densities. Also, at 18 GHz, a CW output power density of 9.1 W/mm with PAE of 23.7% was obtained for device with a field-plate length of 1.1 μm, yielding the highest reported power performance of AlGaN/GaN HEMTs at 18 GHz.

References

[1] S. T. Sheppard, K. Doverspike, W. L. Pribble, S. T. Allen, J. W. Palmour, L. T. Kehias, and T. J. Jenkins, "High power microwave GaN/AlGaN HEMTs on silicon carbide," *IEEE Electron Device Lett.*, vol. 20, no. 4, pp. 161–163, Apr. 1999.

[2] N. X. Nguyen, M. Micovic, W. S. Wong, P. Hashimoto, L. M. McCray, P. Janke, and C. Nguyen, "High performance microwave power GaN/AlGaN MODFETs grown by RF-assisted MBE," *Electron. Lett.*, vol. 36, no. 5, pp. 468–469, Mar. 2000.

[3] W. Lu, J. Yang, M. A. Khan, and I. Adesida, "AlGaN/GaN HEMTs on SiC with over 100 f_T GHz and low microwave noise," *IEEE Trans. Electron Devices*, vol. 48, no. 3, pp. 581–585, Mar. 2001.

[4] S. J. Pearton, J. C. Zolper, R. J. Shul, and F. Ren, "GaN: Processing, defects, and devices," *J. Appl. Phys.*, vol. 86, no. 1, pp. 1–78, Jul. 1999.

[5] V. Tilak, B. Green, V. Kaper, H. Kim, T. Prunty, J. Smart, J. Shealy, and L. Eastman, "Influence of barrier thickness on the high-power performance of AlGaN/GaN HEMTs," *IEEE Electron Device Lett.*, vol. 22, no. 11, pp. 504–506, Nov. 2001.

[6] Y.-F. Wu, A. Saxler, M. Moore, R. P. Smith, S. Sheppard, P. M. Chavarkar, T. Wisleder, U. K. Mishra, and P. Parikh, "30 W/mm GaN HEMTs by field plate optimization," *IEEE Electron Device Lett.*, vol. 25, no. 3, pp. 117–119, Mar. 2004.

[7] Y. Ando, Y. Okamoto, H. Miamoto, T. Nakayama, T. Inoue, and M. Kuzuhara, "10 W/mm AlGaN–GaN HFETs with a field modulating plate," *IEEE Electron Device Lett.*, vol. 24, no. 5, pp. 289–291, May 2003.

[8] C. Lee, T. Tserng, L. Witkowski, P. Saunier, S. Guo, B. Albert, R. Birkhahn, and G. Munns, "Effects of RF stress on power and pulsed IV characteristics of AlGaN/GaN HEMTs with field-plate gates," *Electron. Lett.*, vol. 40, no. 24, pp. 1547–1548, Nov. 2004.

[9] C. Lee, L. Witkowski, T. Tserng, P. Saunier, R. Birkhahn, D. Olson, G. Munns, S. Guo, and B. Albert, "Effects of AlGaN/GaN HEMT structure on RF reliability," *Electron. Lett.*, vol. 41, no. 3, pp. 155–157, Feb. 2005.

[10] R. Thompson, T. Prunty, V. Kaper, and J. Shealy, "Performance of the AlGaN/GaN HEMT structure with gate extension," *IEEE Trans. Electron Devices*, vol. 51, no. 2, pp. 292–295, Feb. 2004.

[11] A. Chini, D. Buttari, R. Coffie, S. Heikman, S. Keller, and U. K. Mishra, "12 W/mm power density AlGaN/GaN HEMT on sapphire substrate," *Electron. Lett.*, vol. 40, no. 1, pp. 73–74, Jan. 2004.

[12] J. S. Moon, S. Wu, D. Wong, I. Milosavljevic, A. Conway, P. Hashimoto, M. Hu, M. Antcliffe, and M. Micovic, "Gate-recessed AlGaN–GaN HEMTs for high-performance millimeter-wave applications," *IEEE Electron Device Lett.*, vol. 26, no. 6, pp. 348–350, Jun. 2005.

[13] V. Kumar, L. Zhou, D. Selvanathan, and I. Adesida, "Thermally-stable low-resistance Ti/Al/Mo/Au multilayer ohmic contacts on n-GaN," *J. Appl. Phys.*, vol. 92, no. 3, pp. 1712–1714, Aug. 2002.

A Novel Voltage-Mode CMOS Quaternary Logic Design

Ricardo Cunha G. da Silva, Henri Boudinov, and Luigi Carro

***Abstract*—This brief presents a novel kind of voltage-mode CMOS design that uses multiple threshold voltage transistors and three power supply lines to implement quaternary logic gates, showing lower power dissipation and using less area than the present voltage-mode quaternary circuits. Inverter, NMIN, and NMAX gates are simulated with the Spice tool using TSMC 0.18-μm technology. The proposed logic circuits overcome the limitations of previous implementations used for multiple-valued logic circuits, such as static power consumption and noise vulnerability.**

***Index Terms*—Inverter, multiple-valued logic (MVL) circuits, NMAX, NMIN, voltage-mode quaternary CMOS design.**

I. Introduction

The interest in electronic circuits that employ more than two discrete levels of signal has recently increased [1]. To go beyond regular CMOS, several researchers have tried to compact more information in a single gate or wire. This has been successfully accomplished in Flash memories, for example, where a single memory bit can hold different logic values. Regarding combinational circuits, most of the efforts have been targeted for the use of multiple-valued logic (MVL) circuits [2]–[4]. Several kinds of MVL circuits have been developed in the past decades, starting from early works on three-valued designs. MVL circuits have been implemented in bipolar technology such as integrated injection logic (I^2L) [5], emitter-coupled logic (ECL) [6], and charge-coupled devices (CCDs) [7] in CMOS technology and using quantum devices [8]. Among the suggested MVL designs concerning the standard IC fabrication process, the most promising was the current-mode CMOS [1]. Several prototype chips of current-mode CMOS circuits have been fabricated, showing somewhat better performances compared with the corresponding binary circuits [9]–[12]. However, some disadvantages are inherent to current-mode CMOS technology, the most critical ones being static power dissipation and variations on the output impedance. To overcome these limitations, some works regarding voltage-mode MVL have been recently published [13]–[15]. In [16], a low-power quaternary adder is presented as a promising way to solve the static power problem using some features of current-mode and voltage-mode combination, but it does not present other basic gates.

To deal with the static power dissipation problem and still maintain the logic compaction allowed by MVL gates, this brief proposes a novel quaternary voltage-mode CMOS logic using transistors with different threshold voltages (V_t) and three levels of power supply. We present inverter, NMAX, and NMIN logic gates.

Spice simulations have been done to confirm the functionality and performance of the proposed voltage-mode CMOS quaternary logic as compared with previous voltage-mode quaternary circuits.

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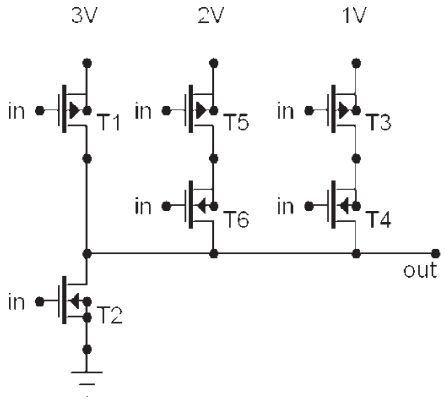
TABLE I
TRANSISTOR V_t VALUES RELATED TO V_s

	T1	T2	T3	T4	T5	T6
Vt	-2.2	2.2	1.8	0.2	-0.2	-1.8
type	PMOS	NMOS	PMOS	NMOS	PMOS	NMOS



in	out
0	3
1	2
2	1
3	0

(a) (b)

Fig. 1. (a) Inverter circuit and (b) its truth table.

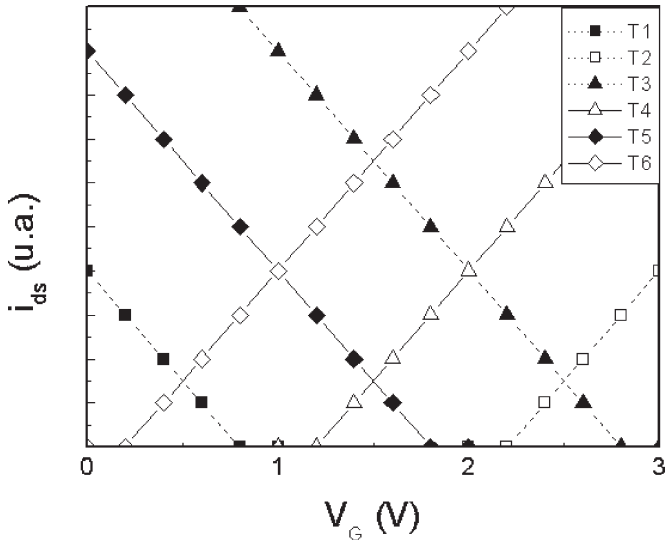


Fig. 2. Schematic $I_{\rm ds} \times V_{\rm gs}$ curves for the 6 transistors used in inverter circuit.

II. QUATERNARY CMOS INVERTER

The proposed voltage-mode quaternary logic CMOS circuits operate with four voltage levels, corresponding to 0 V and three power supply lines of 1, 2, and 3 V. The quaternary logic circuits are designed by using standard CMOS technology with three different V_t for pMOS transistors and three different V_t for nMOS transistors. Table I shows the V_t values relative to the transistor source–bulk voltage. The V_t adjustment is possible by using multiple ion implants in standard fabrication process.

Fig. 1(a) shows a quaternary inverter circuit that accomplishes the logic described in the truth table in Fig. 1(b). The inverter consists of three pMOS and three nMOS transistors. In the case of three different $V_{\rm DD}$, one can connect transistor sources in 0, 1, 2, or 3 V, and the real threshold values depend on this connection. The $I_{\rm ds} \times V_{\rm gs}$ curves of

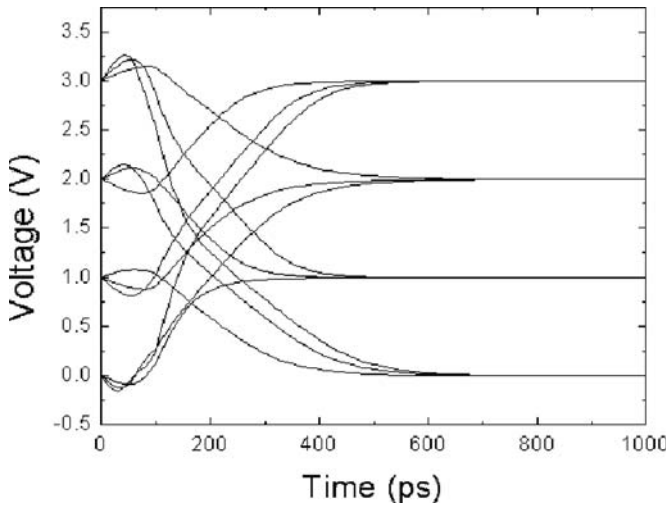


Fig. 3. Output curves for all possible input transitions.

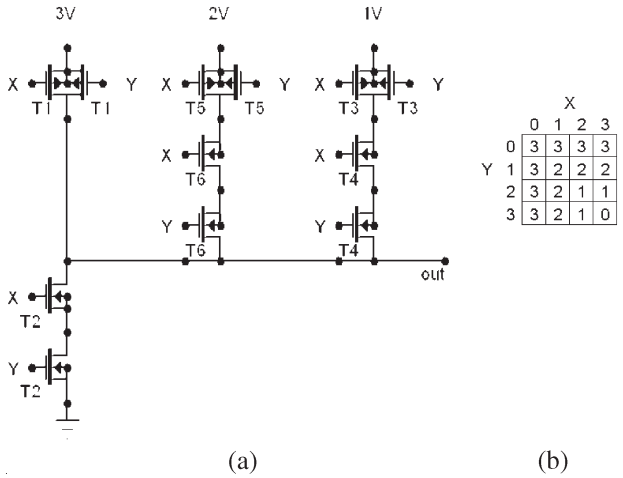
TABLE II
PERFORMANCE COMPARISON OF NEW CMOS QUATERNARY INVERTER CIRCUIT AND NMOS QUATERNARY INVERTER CIRCUIT

	Av. delay time (ps)	Av. power dissipation (μW) at 1 GHz	at 0.1 GHz	Static	Area (u.a.)
this work	282	50	5	0,003	1
[13]	236	626	550	539	1.35

the inverter transistors are shown in Fig. 2. This way, it is possible to ensure that only one of the voltage levels is shorted to the output for a certain input voltage. If the input value is 0 V, transistor T1 is turned on, driving the output to 3 V, whereas T2, T4, and T6 are turned off, cutting the remain paths. When the input is set to 1 V, T1 is turned off, whereas T6 is turned on, driving the output to 2 V. When the input is set to be 2 V, T5 is turned off, whereas T4 is turned on, hence driving the output to 1 V. T2 sinks the output to zero only when the input goes to 3 V, turning off T3.

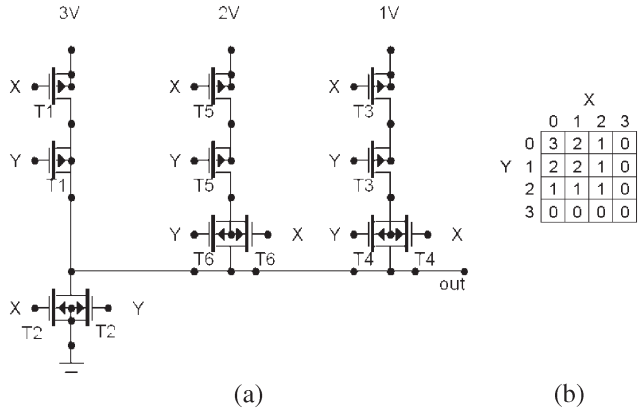
The first point to consider comparing the present CMOS voltage-mode quaternary logic with other voltage-mode technologies is noise margin. The four voltage levels are supplied by external sources, so that levels are well defined and independent of fabrication process variations of the components and immune to noise. Some voltage-mode circuits have their levels achieved by resistance voltage divider [13]. In this kind of circuit, process variations can change the voltage levels. Moreover, variations on entry voltages cause change on transistor resistances resulting in variations on the output.

Transient analyses of the inverter circuit were carried out using TSMC 0.18-μm technology. Transistor widths were 2, 2, 2, 1, 2, and 1 μm for transistors T1, T2, T3, T4, T5, and T6, respectively. Fig. 3 shows the inverter output transients for all possible input logic sequences. The average propagation delay time value was 282 ps using as a load a binary inverter with $L = 0.18$ μm and $W = 1$ μm at the output. Simulation of the nMOS inverter circuit in [13] using TSMC 0.18 μm and the same output load showed a mean delay time of 236 ps. However, the inverter circuit presented here has an average power consumption of 50.6 μW at 1 GHz and a negligible static consumption. Yasuda *et al.* [13] circuits presented a mean power consumption of 626.7 μW at 1 GHz and a much higher static consumption. The summary of the results is shown in Table II. In [14] and [15], the inverter circuit was not demonstrated and could not be compared.



Y \ X	0	1	2	3
0	3	3	3	3
1	3	2	2	2
2	3	2	1	1
3	3	2	1	0

Fig. 4. (a) NMIN circuit and (b) its truth table.



Y \ X	0	1	2	3
0	3	2	1	0
1	2	2	1	0
2	1	1	1	0
3	0	0	0	0

Fig. 5. (a) NMAX circuit and (b) its truth table.

Despite the fact that electron mobility is approximately three times greater than the holes in CMOS standard technology, when designing CMOS quaternary circuits using multipower supply, one does not need to use pMOS and nMOS transistor width ratio of more than two. (We have used $W_p = 2W_n$.) This is due to the current flow to the other sources when the output is transitioning between levels, e.g., when the output goes from 0 to 3 V, we have current contributions from the 1- and 2-V supply sources during the transient. This is faster than if we had only the 0- and 3-V power supplies. Multipower supply also helps reduce power consumption. Some circuits can make a charge sharing among sources during the transients, e.g., two inverters in series. In this circuit, when the output of the first inverter is transitioning from 1 to 2 V, the output of the second inverter is transitioning from 2 to 1 V, and a charge sharing between 1- and 2-V supply lines takes place, lowering the external current need. This feature can be applied for low-power buffers.

Concerning technological issues, a new feature can be seen in the transistor bulk connections that can be implemented in silicon wafer, but their full potential can only be achieved using silicon-on-insulator (SOI) wafer. The ability to set bulk contact of each transistor in different voltages in SOI wafers is a feature never explored before to make circuits like the ones presented in this brief.

III. NMIN and NMAX Circuits

In quaternary logic, the AND/NAND logic gates are replaced by MIN/NMIN gates. The MIN operation sets the output of the MIN circuit to be the lowest value of several inputs. The implementation of an NMIN circuit with two quaternary inputs is shown in Fig. 4(a). The circuit is based on the inverter circuit in Fig. 1 and a common binary nand circuit. An input set to zero will produce the output of 3 V regardless of the other input voltage level. The nMOS transistors disposed in series make the paths to 1 V, 2 V, and ground to be opened only when both inputs are equal to or higher than the V_t of both transistors. pMOS transistors are responsible to close the path when both inputs are higher than their V_t values. Fig. 4(b) shows the truth table of the NMIN gate.

Logic gates OR and NOR also have no meaning in quaternary logic, and these gates are replaced by MAX and NMAX gates, respectively. The MAX gate is a circuit of multiple inputs and sets the output in the higher value of all entries. Fig. 5(a) shows an NMAX circuit with two quaternary inputs, designed for voltage-mode quaternary CMOS logic. The truth table of this gate is shown in Fig. 5(b). The highest value of all the inputs sets the output. When both inputs are in 0 V, both T1 transistors are turned on, driving the output to 3 V. One of the inputs set on a higher value is enough to close the path from the output to the 3-V power supply and to open all other paths. Any input in 1 V opens one of the T6 transistors and turns off one of the T1 transistors, placing the output at 2 V. In the same way, any 2-V inputs will turn on any T4 transistor while at the same time turning T1 and T5 off. Any 3-V input turns on a T2 transistor and turns off the T1, T5, and T3 transistors.

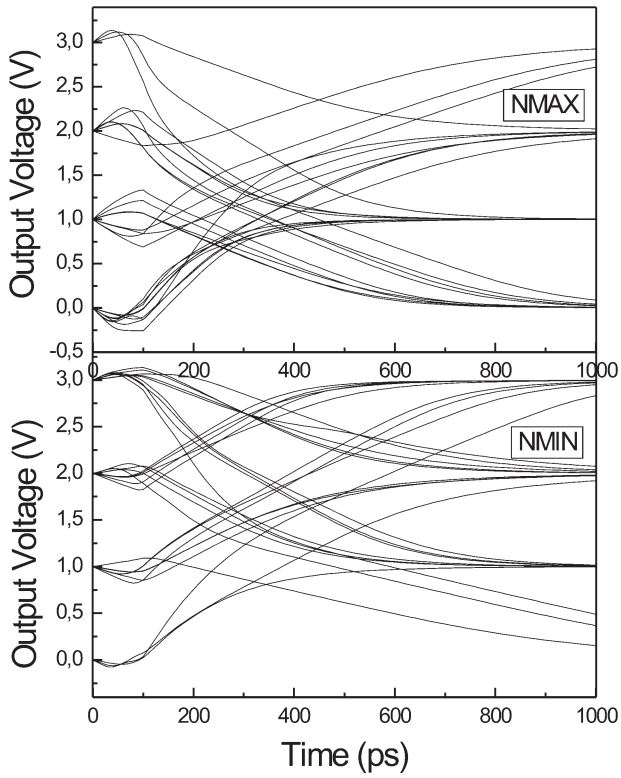


Fig. 6. NMIN and NMAX output curves for all possible transients.

Transient results for NMIN and NMAX circuits using TSMC 0.18-μm technology are shown in Fig. 6. The analysis was carried out with one of the entries in a constant voltage and varying the second input. The average propagation delay was 451 and 422 ps for NMIN and NMAX circuits, respectively, and the average consumption was approximately 58.4 μW for NMIN and 72.7 μW for NMAX at 1 GHz.

In [15], using 0.35-μm technology, the average power dissipation was 4.9 μW at 0.25 MHz. Our simulation of NMIN and NMAX circuits at the same frequency using TSMC 0.35 μm showed an average consumption of 0.045 μW.

IV. Conclusion

A novel CMOS quaternary logic is proposed using multi-V_t transistors and three-level power supply lines. Inverter, NMIN, and NMAX gates have been simulated by Spice using TSMC 0.18-μm technology. Circuit simulations have shown high speed and low power consumption when compared with previous voltage-mode quaternary circuits.

Logic functions like NMIN and NMAX do not have a binary direct correspondence, and no comparisons can be done at this level. The comparison shall be done on a higher level with more complex circuits.

References

[1] E. Dubrova, "Multiple-valued logic in VLSI: Challenges and opportunities," in *Proc. NORCHIP*, 1999, pp. 340–350.

[2] K. C. Smith, "The prospects for multivalued logic: A technology and applications view," *IEEE Trans. Comput.*, vol. C-30, no. 9, pp. 619–634, Sep. 1981.

[3] S. L. Hurst, "Multiple-valued logic—Its status and its future," *IEEE Trans. Comput.*, vol. C-33, no. 12, pp. 1160–1179, Dec. 1984.

[4] J. T. Butler, "Multiple-valued logic," *IEEE Potentials*, vol. 14, no. 2, pp. 11–14, Apr./May 1995.

[5] E. J. McCluskey, "Logic design of multivalued I^2L logic circuits," *IEEE Trans. Comput.*, vol. C-28, no. 8, pp. 546–559, Aug. 1979.

[6] A. Druzeta, Z. G. Vranesic, and A. S. Sedra, "Applications of multithreshold elements in the realization of many-valued logic networks," *IEEE Trans. Comput.*, vol. C-23, no. 11, pp. 1194–1198, Nov. 1974.

[7] H. G. Kerkhoff and M. L. Tervoert, "Multiple-valued logic charge-coupled devices," *IEEE Trans. Comput.*, vol. C-30, no. 9, pp. 644–652, Sep. 1981.

[8] F. Capasso *et al.*, "Quantum functional devices: Resonant-tunneling transistors, circuits with reduced complexity, and multiple-valued logic," *IEEE Trans. Electron Devices*, vol. 36, no. 10, pp. 2065–2082, Oct. 1989.

[9] T. Hanyu and M. Kameyama, "A 200 MHz pipelined multiplier using 1.5 V-supply multiple valued MOS current-mode circuits with dual-rail source-coupled logic," *IEEE J. Solid-State Circuits*, vol. 30, no. 11, pp. 1239–1245, Nov. 1995.

[10] B. Radanovic and M. Syrzycki, "Current-mode CMOS adders using multiple-valued logic," in *Proc. Can. Conf. Elect. Comput. Eng.*, 1996, pp. 190–193.

[11] J. Shen *et al.*, "Neuron-MOS current mirror circuit and its application to multi-valued logic," *IEICE Trans. Inf. Syst.*, vol. E82-D, no. 5, pp. 940–948, May 1999.

[12] D. H. Y. Teng and R. J. Bolton, "A self-restored current-mode CMOS multiple-valued logic design architecture," in *Proc. IEEE PACRIM*, 1999, pp. 436–439.

[13] Y. Yasuda, Y. Tokuda, S. Zhaima, K. Pak, T. Nakamura, and A. Yoshida, "Realization of quaternary logic circuits by n-channel MOS devices," *IEEE J. Solid-State Circuits*, vol. SC-21, no. 1, pp. 162–168, Feb. 1986.

[14] I. Thoidis, D. Soudris, I. Karafyllidis, S. Christoforidis, and A. Thanailakis, "Quaternary voltage-mode CMOS circuits for multiple-valued logic," *Proc. Inst. Elect. Eng.—Circuits Devices Syst.*, vol. 145, no. 2, pp. 71–77, Apr. 1998.

[15] S. J. Park, B. H. Yoon, K. S. Yoon, and H. S. Kim, "Design of quaternary logic gate using double pass-transistor logic with neuron MOS down literal circuit," in *Proc. 34th Symp. Multiple-Valued Logic*, 2004, pp. 198–203.

[16] T. Hanyu, A. Mochizuki, and K. Kameyama, "Multiple-valued dynamic source-coupled logic," in *Proc. 33rd IEEE Int. Symp. Multiple-Valued Logic*, May 2003, vol. 33, pp. 207–212.

Indium–Tin–Oxide-Free Organic Light-Emitting Device

Lin Ke, Peng Chen, Ramadas Senthil Kumar, Adrian Paul Burden, and Soo-Jin Chua

***Abstract*—Sapphire substrates coated with a gold (Au) layer in place of indium–tin–oxide (ITO) on glass substrates are used as hole-injecting anodes in organic light-emitting devices (OLEDs). Due to the unique quality of the sapphire/Au interface and the match of the Au work function with the highest occupied molecular orbital level of the adjacent hole transport layer (HTL) and the smoothness of the interface, the ITO-free OLED, with the structure sapphire/Au/HTL/poly(*p*-phenylenevinylene)/Ca/Ag, achieved an increase in current efficiency by more than a factor of three. In addition, the flawless sapphire substrate and anode/polymer interface make dark nonemissive areas decrease in number and area. The diodes show substantially slower degradation, and the lifetime in air increases by a factor of two or more.**

***Index Terms*—Highest occupied molecular orbital (HOMO), Indium–tin–oxide-free (ITO-free), lowest unoccupied molecular orbital (LUMO), organic light-emitting device (OLED).**

I. Introduction

Organic light-emitting diodes (OLEDs) have been intensively studied in the past several years owing to their potential commercial application in full-color flat-panel displays. The typical OLED structure consists of a glass substrate coated with a transparent conductor, indium–tin–oxide (ITO), coated with organic electroluminescent (EL) materials, and followed by a vapor-deposited metal cathode [1]. The device quantum efficiency and driving voltage depend on the charge-injection property at the interfaces between the EL polymer and electrodes.

The choice of anode material for OLEDs is based on several criteria. The anode in a conventional OLED must have good optical transparency, good electrical conductivity and chemical stability, and a work function that lies near the highest occupied molecular orbital (HOMO) levels of the organic materials to which it will inject holes. ITO generally fits these criteria and is the most widely used anode material in OLEDs. Much effort has been made to improve the device performance. Recent studies have shown that ITO/hole transport layer (HTL) interface plays an important role in device performance and lifetime [2]–[4]. The ITO anode has been modified with both thin films [5], [6] and self-assembled monolayers [7]–[9] to reduce the barrier-to-hole injection, improve adhesion at the anode–organic film interface [10], [11], and inhibit possible diffusion of material across the interface [12]. Introducing an ultrathin interlayer of different materials at the interface, the efficiency of the devices could be improved through a better contact and smoothened interface, and reduced barrier for holes has also been attempted [13], [14].

In an earlier publication [12], [15]–[20], the dark nonemissive area formation mechanism has also been elaborated, having much relationship with the ITO spikes and polymer interface roughens. Under electrical stress and metal migration, there are areas where Ca

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