Power Modeling and Characteristics of Field Programmable Gate Arrays

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***Abstract*—This paper studies power modeling for field programmable gate arrays (FPGAs) and investigates FPGA power characteristics in nanometer technologies. Considering both dynamic and leakage power, a mixed-level power model that combines switch-level models for interconnects and macromodels for look-up tables (LUTs) is developed. Gate-level netlists back-annotated with postlayout capacitances and delays are generated and cycle-accurate power simulation is performed using the mixed-level power model. The resulting power analysis framework is named as fpgaEVA-LP2. Experiments show that fpgaEVA-LP2 achieves high fidelity compared to SPICE simulation, and the absolute error is merely 8% on average. fpgaEVA-LP2 can be used to examine the power impact of FPGA circuits, architectures, and CAD algorithms, and it is used to study the power characteristics of existing FPGA architectures in this paper. It is shown that interconnect power is dominant and leakage power is significant in nanometer technologies. In addition, tuning cluster and LUT sizes lead to $1.7\times$ energy difference and $0.8\times$ delay difference between the resulting min-energy and min-delay FPGA architectures, and FPGA area and power are reduced at the same time by tuning the cluster and LUT sizes. The existing commercial architectures are similar to the min-energy (and min-area at the same time) architecture according to this study. Therefore, innovative FPGA circuits, architectures, and CAD algorithms, for example, considering programmable power supply voltage, are needed to further reduce FPGA power.**

***Index Terms*—FPGA architecture, FPGA power model, power characteristics.**

I. Introduction

POWER has become an increasingly important design constraint in nanometer technologies. Field programmable gate arrays (FPGAs) are known to be less power efficient than application-specific integrated circuits (ASICs) because a large number of transistors are used to provide field programmability. For example, [1] compared an 8-bit adder implemented in a Xilinx XC4003A FPGA with the same adder implemented in a fully customized complementary metal oxide semiconductor (CMOS) ASIC, and showed a $100\times$ difference in energy consumption (4.2 mW/MHz at 5 V for FPGA versus 5.5 μW/MHz at 3.3 V for ASIC counterpart). Therefore, it is important to study power modeling and reduction for nanometer FPGAs.

Manuscript received July 10, 2003; revised May 20, 2004 and December 13, 2004. This work was supported in part by NSF CAREER Award CCR-0401682 and NSF Grant CCR-0306682. This paper was recommended by Associate Editor M. Pedram.

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Digital Object Identifier 10.1109/TCAD.2005.852293

There is limited published work about FPGA power modeling and power characteristics. Kussey and Rabaey [1] used a Xilinx XC4003A FPGA test board to measure power and reported a power breakdown for FPGA components. Shang *et al.* [2] analyzed the dynamic power for Xilinx Virtex-II FPGA family based on measurement and simulation. Weiß *et al.* [3] presented the power consumption for Xilinx Virtex architecture using an emulation environment. Tuan and Lai [4] studied the leakage power of Xilinx architectures. The aforementioned work was all carried out for specific FPGA architectures. Parameterized power models were proposed for generic FPGA architectures in [5] and an early version [6] of this paper. However, both [5] and [6] oversimplified the models for short-circuit and leakage power, and verification by measurement or circuit-level simulation was not reported in [5] and [6].

This paper first develops a mixed-level power model more accurate than those in [5] and [6] for parameterized FPGA architectures. Cluster-based logic blocks and island-style routing structures are assumed. One logic block is a cluster of look-up tables (LUTs) with the cluster size N (i.e., the number of LUTs inside one cluster) and the LUT size k (i.e., the number of inputs to the LUT) as the architectural parameters. Logic blocks are embedded into the routing resources as logic "islands" and segmented wires are used to connect these logic "islands." This parameterized FPGA architecture is general enough to cover the architectural features of most commercial FPGAs such as [7] and [8]. The proposed new power model considers both dynamic and leakage power, and combines switch-level models for interconnects and macromodels for logic cells. Gate-level netlists back-annotated with postlayout capacitances and delays are generated, and cycle-accurate power simulation is performed. A detailed delay model is used for glitch power analysis and short-circuit power is modeled as a function of signal transition time. Experiments show that the proposed power model achieves high fidelity compared to SPICE simulation, and the absolute error is around 8% on average.

The resulting power analysis framework is named as fpgaEVA-LP2 and is applied to evaluating the power characteristics of existing FPGA architectures in 100 nm technology. It is shown that interconnect power is dominant and leakage power is significant in nanometer technologies. In addition, tuning cluster and LUT sizes lead to $1.7\times$ energy difference and $0.8\times$ delay difference between the resulting min-energy and min-delay FPGA architectures, and FPGA area and power can be reduced at the same time by tuning cluster and LUT sizes. The existing commercial architectures are similar to the min-energy (and min-area at the same time) architecture according to this study. Therefore, innovative FPGA circuits, architectures,

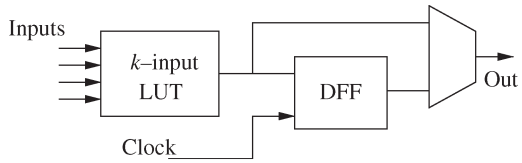

Fig. 1. Basic logic element (BLE).

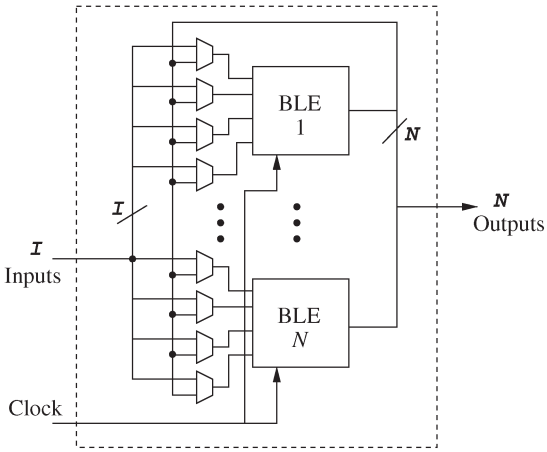

Fig. 2. Cluster-based logic block.

and CAD algorithms, for example, applying programmable power supply, are needed to further reduce FPGA power. fpgaEVA-LP2 has been employed in a few recent studies on FPGA power reduction [9]–[13].

The paper is organized as follows. Section II introduces background knowledge. Section III discusses the proposed mixed-level power model. Section IV introduces the power analysis framework fpgaEVA-LP2 and studies power characteristics of the existing FPGA architectures. Section V concludes the paper with discussion of recent research progress for FPGA power reduction. An extended abstract of this paper was presented in [13].

II. FPGA Background

A. Candidate Architectures

An FPGA architecture is mainly defined by its logic block and routing structure. By varying the architectural parameters for logic blocks and routing structure, one can create many different FPGA architectures. LUT-based FPGAs are assumed, where the basic logic element (BLE) (see Fig. 1) consists of one k-input look-up table (k-LUT) and one flip-flop. The output of the k-LUT can be programmed to be either registered or unregistered. Previous work [14] has shown that a different LUT input number k leads to a different tradeoff between FPGA area and performance. It will be interesting to investigate how the LUT input number k affects FPGA power consumption. N BLEs can further form a cluster-based logic block as shown in Fig. 2. The cluster inputs and outputs are fully connected to the inputs of each LUT [15]. Cluster size N is another important architectural parameter that affects FPGA performance and power.

Routing structure is critical to FPGA designs because routing wires consume a large portion of the total FPGA area [16] and

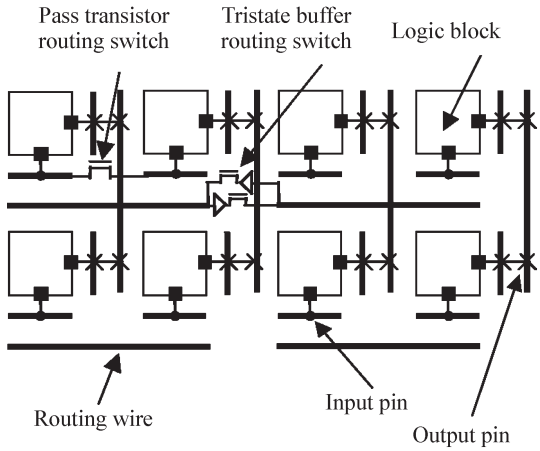

Fig. 3. Island-style routing structure.

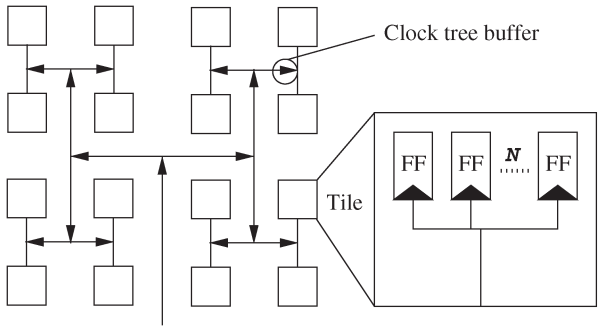

Fig. 4. Clock network.

power [1]. This paper assumes island-style routing that is used in most commercial FPGAs such as [7], [8] and [17]. The logic blocks are connected by a two-dimensional (2-D) mesh-like interconnect structure, and horizontal and vertical routing channels are connected by programmable switch blocks. Fig. 3 presents a simplified view of an example island-style routing structure, where half of the routing tracks consist of length-1 wires (wires spanning one logic block) and the other half consist of length-2 wires. Programmable routing switches are either pass transistors or tristate buffers. There are also switches (called connection blocks) connecting the wire segments to the logic block inputs and outputs. Betz *et al.* [18] define the routing architectural parameters including channel width (W), switch block flexibility (Fs—the number of wires to which each incoming wire can connect in a switch block), connection block flexibility (Fc—the number of wires in each channel to which a logic block input or output pin can connect) and segmented wire lengths.

In addition to logic block and routing architectures, clock distribution structure is another aspect in FPGA designs. A simple H-tree structure is assumed for FPGA clock networks (see Fig. 4). A tile is a cluster-based logic block with cluster size N. Each clock tree buffer in the H-tree has two branches. Clock tree buffers in the H-tree are considered to be clock network resources. Chip area, tile size, and routing channel width determine the clock tree depth and the branch lengths. Commercial FPGA architectures usually have multiple clock

networks. For example, Altera Stratix [8] has 16 global clock networks and 16 regional clock networks. Each global clock network drives through the entire device, and each regional clock network provides clock signals to one quadrant of the chip. In this paper, it is simply assumed that there are four clock networks, and each of them provides a clock signal to the whole chip. More realistic clock networks can be modeled and studied with details of clock network design.

B. Area Model

The area model in fpgaEVA-LP2 is based on the technology-scalable area model implemented in VPR [18]. Basically, the number of minimum-width transistor areas required to implement a specific FPGA architecture is counted. By using the number of minimum-width transistor areas instead of the number of microsquares, this area model can be easily applied to future technologies.

C. Delay Model

The delay model in fpgaEVA-LP2 uses delay values obtained by SPICE simulations in the predictive 100 nm CMOS technology [19]. BSIM4 SPICE model is used in the circuit simulation. Table I shows some key model parameters for the proposed device and interconnect model. Various circuit paths inside a logic block are simulated and path delays are precharacterized. Fig. 5 presents the schematic of a cluster-based logic block, which is extended from the schematics presented in [14]. Table II shows some key delay values corresponding to the paths in Fig. 5 (only data for $k = 4$ are shown in the table). Note that the delay of path C $\rightarrow$ E is larger than the delay of path C $\rightarrow$ D. This is because path C $\rightarrow$ E is for the BLE sequential mode, and its delay includes both LUT delay and setup time of the flip-flop. Path C $\rightarrow$ D is for the BLE combinational mode and the flip-flop is bypassed. The area model in VPR is further used to estimate FPGA layout geometry by assuming the tile-based layout [18]. The resistance and capacitance of wires in the routing channels are estimated by using the proposed interconnect model. Pass transistors connecting different wire segments are modeled by the equivalent resistance and capacitance. Elmore delay is then calculated for the interconnect resistance–capacitance (RC) trees in a given netlist. The details of interconnect delay calculation are discussed in Section IV-A.

TABLE I
DEVICE AND INTERCONNECT MODEL IN OUR SPICE SIMULATION AT 100 nm TECHNOLOGY

Device model		
Parameters	NMOS	PMOS
V_t	0.26 V	-3.3 V
T_{ox}	2.5 nm	2.5 nm
V_{dd}	1.3 V	1.3 V

Interconnect model			
wire width	wire spacing	wire thickness	dielectric constant
0.56 μm	0.52 μm	1.08 μm	2.7

III. MIXED-LEVEL POWER MODEL

A. Overview

There are three power sources in FPGAs, namely: 1) switching power; 2) short-circuit power; and 3) static power. The first two types of power together are called dynamic power, and they can only occur when a signal transition happens. There are two types of signal transitions. 1) Functional transition is the necessary signal transition to perform the required logic functions between two consecutive clock ticks. 2) Spurious transition or glitch is the unnecessary signal transition due to the unbalanced path delays to the inputs of a gate. Glitch power can be a significant portion of the dynamic power. The third type of power, static power, is the power consumed when there is no signal transition for a gate or a circuit module. As the technology advances to feature size of 100 nm and below, static power will become comparable to dynamic power. The different power sources are summarized in columns 1–3 of Table III.

To consider the above power sources, both switch-level model and macromodel are developed as summarized in columns 4 and 5 of Table III. A switch-level model uses formulas and extracted parameters, such as capacitance and resistance, to model the power consumption related to signal transitions. A macromodel precharacterizes a circuit module using SPICE simulation and builds an LUT for power values. In the following, the dynamic power models are discussed, which include the switch-level model for interconnects and clock networks as presented in Section III-B1 and the macromodels for LUTs as discussed in Section III-B2. The transition density and glitch analysis applicable to both interconnects and LUTs are discussed in Section III-B3. Section III-C then introduces the proposed static power model and Section III-D summarizes the overall power calculation.

B. Dynamic Power Model

1) Switch-Level Model for Interconnects: One type of dynamic power, switching power P_{sw}, is usually modeled by the following formula

$$P_{sw} = 0.5 f V_{dd}^2 \sum_{i=1}^{n} C_i E_i \quad (1)$$

where n is the total number of nodes, f is the clock frequency, V_{dd} is the supply voltage, C_i is the load capacitance for node i, and E_i is the transition density for node i. To apply this switch-level model directly, the capacitance C_i has to be extracted and the transition density E_i estimated for each circuit node. However, (1) cannot take into account internal nodes in a complex circuit module such as the LUTs. A flattened netlist is needed to apply (1), which results in the loss of computational efficiency. Furthermore, (1) only considers full swings either from V_{dd} to GND or GND to V_{dd}. Glitches due to small delay differences at the gate inputs may have partial swings that cannot be correctly modeled by (1). To achieve computational efficiency, the switch-level model is only applied to interconnects as well as buffers in clock networks. Macromodels are developed for LUTs and the transition density of LUTs is used to calculate their dynamic power, which will be discussed in Section III-B2. To correctly model glitches with partial swing

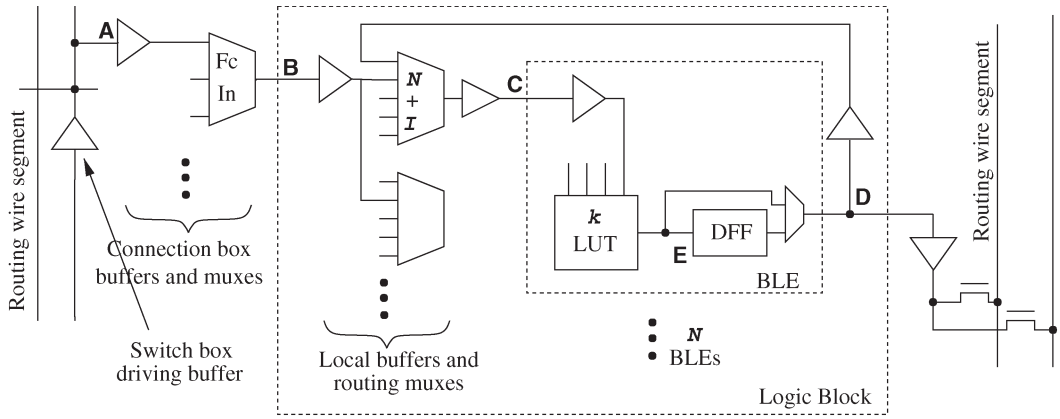

Fig. 5. Schematic for a logic block.

TABLE II
KEY DELAY NUMBERS FOR PATHS IN FIG. 5 ($k = 4$)

Path	Cluster size N	LUT size k	Delay (nanosecond)
A → B	4	4	0.293
B → C	4	4	0.233
B → C	8	4	0.285
B → C	12	4	0.290
B → C	16	4	0.356
B → C	20	4	0.450
C → E	4	4	0.393
C → D	4	4	0.271

TABLE III
POWER SOURCES AND MIXED-LEVEL POWER MODEL

Column 1	Column 2	Column 3	Column 4	Column 5
Power sources			Logic blocks	Interconnect and clock
Dynamic power	Switching power	Functional transition	Macromodel	Switch-level model
		Glitch		
	Short-circuit power	Functional transition		
		Glitch		
Static power			Macromodel	Macromodel

at switch level, effective transition density $\hat{E}_i$ is defined, and (1) is extended as

$$P_{\rm sw} = 0.5 f V_{\rm dd}^2 \sum_{i=1}^{n} C_i \hat{E}_i. \tag{2}$$

Details of $\hat{E}_i$ calculation and glitch analysis will be discussed in Section III-B3.

Short-circuit power $P_{\rm sc}$ is another type of dynamic power. When a signal transition occurs at a gate output, both the pull-up and pull-down transistors can be conducting simultaneously for a short period of time. Short-circuit power represents the power dissipated via the direct current path from $V_{\rm dd}$ to GND during the signal transition. It is a function of the input signal transition time and load capacitance. The short-circuit power is modeled for interconnects and clock network at the switch level. Short-circuit power for LUTs is considered in their macromodels and will be discussed later on.

To determine the short-circuit power, interconnect buffers are simulated with different sizes and load capacitances, and the dynamic power is studied per signal transition. Fig. 6 shows the total dynamic power per transition for a minimum size buffer with two different load capacitances. "$\rm load = inv1x$" in the figure represents one min-width inverter as the fanout gate and "$\rm load = 2inv1x$" represents two min-width inverters as fanout gates. It is clear that dynamic power for a buffer increases linearly with respect to the input signal transition time, which has been illustrated for cascade inverters in [20]. Instead of using an average (or fixed) ratio between short-circuit power and dynamic power as in [5] and [6], this paper assumes that the ratio $\alpha_{\rm sc}$ is a linear function of the input transition time t_r and obtains short-circuit power $P_{\rm sc}$ as

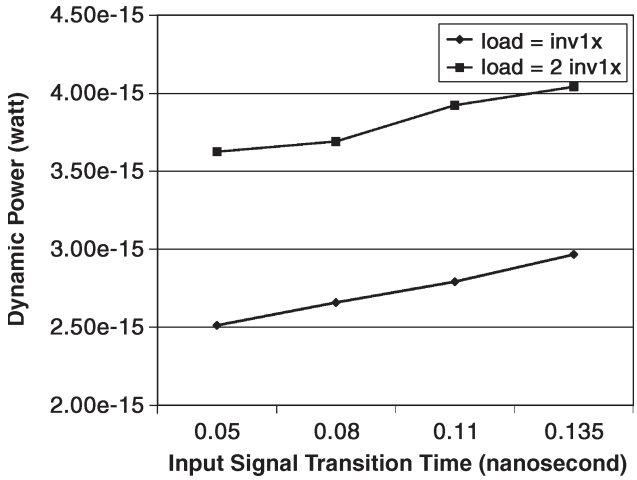

Fig. 6. Short-circuit power modeling ("inv1x" is a min-width inverter).

$$\begin{aligned} P_{\rm sc} &= \alpha_{\rm sc}(t_r) P_{\rm sw} \\ &= \alpha_{\rm sc}(t_r) 0.5 f V_{\rm dd}^2 \sum_{i=1}^{n} C_i \hat{E}_i. \end{aligned} \tag{3}$$

A linear curve fitting is applied to decide the ratio $\alpha_{\rm sc}$. In the curve fitting, the X-axis is input transition time and the Y-axis is dynamic power. Assuming that zero transition time leads to zero short-circuit power, the Y-axis intersection is treated as the switching power and $\alpha_{\rm sc}(t_r)$ is then calculated. In addition, an accurate transition time t_r is needed to apply this short-circuit power model. Li *et al.* [6] assumes that the output

TABLE IV
VALUE OF PARAMETER α TO DETERMINE SIGNAL TRANSITION TIME

Buffer delay	< 0.012 ns	< 0.03 ns	≥ 0.03 ns
α	2	4.4	7

TABLE V
DYNAMIC POWER OF A FOUR-LUT UNDER DIFFERENT INPUT VECTOR PAIRS

v_1	v_2	Dynamic power (10^{-13} W)
0000	1000	1.22
1000	0100	0.845
0100	1100	1.22
1100	0010	1.04
1010	0110	1.22

signal transition time is twice of the buffer delay. This simplistic assumption was originally used in gate sizing [21], [22], and it is valid when the input signal is a step function and the output signal is a ramp function. SPICE is used to simulate a typical routing path in an FPGA, where a routing switch drives a wire segment and other routing switches. It was found that the input signal is no longer a step function because the input is the output of a routing switch in the previous stage. The output signal under a large load capacitance, which is usually the case in FPGAs, is not a perfect ramp function, and the 10–90% transition time for the output signal can be significantly larger than twice the buffer delay. The output signal transition time t_r as $t_r = \alpha t_{\text{buffer}}$ is modeled, where t_{buffer} is the buffer delay under load capacitance. SPICE simulation is used to determine the parameter α for different buffer delays (see Table IV), which covers the cases of various input signal transition time and different load capacitance.

2) Macromodel for LUTs: Macromodels for LUT dynamic power are built. Since LUTs are regularly connected in a cluster-based logic block, they usually have a fixed load capacitance. This reduces the number of dimensions of the power LUT in the proposed macromodel. However, as shown in Table V, different input vector pairs $(v_1 \rightarrow v_2)$ for an LUT lead to different levels of dynamic power. SPICE simulation is used with randomly generated input vectors to obtain the average dynamic power per access to the LUT, and therefore compress the complete power table into one power value assuming equal occurrence probability for all input vectors. The number of vectors is decided so that the change of average power is negligible by increasing the number of vectors, and a few hundreds of input vectors are used in the experiments. The power values for LUTs with different sizes are stored, and the access transition density for LUTs is used to calculate their dynamic power. The proposed power model is similar to that in the architectural-level microprocessor power analysis tool Wattch [23] in the sense that both assume that all the input vectors have an equal occurrence probability and therefore the (average) dynamic power is independent of logic vectors.[1]

[1]To consider the different switching probability in different applications, methods such as the input vector clustering [24] can be employed to improve the power model in the future. In addition, we will study how to find representative input vectors for power characterization.

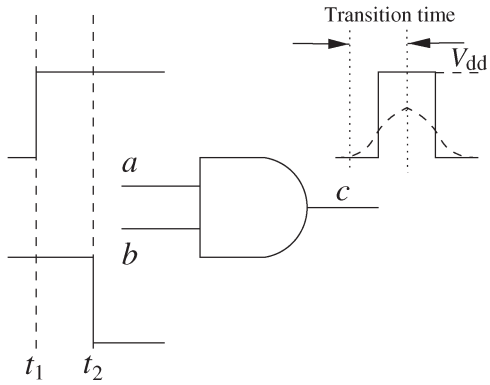

Fig. 7. Glitches at a circuit node.

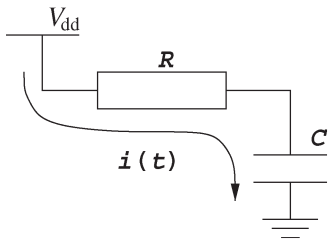

Fig. 8. RC circuit model.

3) Transition Density and Glitch Analysis: A recent work on FPGA power modeling [5] uses Boolean difference to calculate the transition density. However, it is difficult for Boolean difference to precisely capture the spatial and temporal signal correlations among circuit nodes [25]. The gate-level cycle-accurate simulation is used to calculate the transition density. Assuming that primary inputs of a circuit have a signal probability of 0.5 and transition probability of 0.85, a large number of random input vectors are generated to simulate the circuit. Two thousand random vectors are used in this paper. To consider sequential circuits, these 2000 random vectors for real primary inputs are divided into 20 vector sequences, with the uniform sequence length of 100. At the beginning of the simulation for each vector sequence, initial states for pseudo primary inputs are randomly generated, i.e., the outputs of flip-flops, with a signal probability of 0.5 and the next state is calculated in every cycle of the vector sequence.

Glitches may occur at a gate output when the incoming signals reach the gate inputs at different times due to unbalanced path delays. Fig. 7 illustrates this case. When inputs a and b of the AND gate do not switch at the same time, a glitch (spurious transition) is generated at the output before it finally stabilizes. Although the interconnect buffers have only one input, they may propagate the glitches and may also consume glitch power. Glitches are not always full swings from V_{dd} to GND or GND to V_{dd}. When t_1 and t_2 in Fig. 7 are close enough to each other, the maximum voltage level of the glitch can be lower than V_{dd} due to the nonzero signal transition time. Clearly, dynamic power of such a glitch is smaller than that of a full swing.

To consider the partial swings in the proposed power model, a gate with the simple RC circuit is modeled as shown in Fig. 8. R is the effective pull-up transistor resistance and C is the

load capacitance. The current $i(t)$ charges the load capacitance C and the gate output $V(t)$ has a rising transition. Let V_1 be the initial value of $V(t)$ and V_2 be the maximum voltage that the rising transition can reach. Then

$$C\frac{\mathrm{d}V(t)}{\mathrm{d}t} = i(t). \tag{4}$$

Energy consumption E_{sw} of the resistance R is calculated as follows

$$\begin{aligned} E_{\mathrm{sw}}(V_1 \to V_2) &= \int_{t_1}^{t_2} i^2(t)R\mathrm{d}t \\ &= \int_{t_1}^{t_2} i(t)\left(V_{\mathrm{dd}} - V(t)\right)\mathrm{d}t \\ &= \int_{V_1}^{V_2} C\left(V_{\mathrm{dd}} - V(t)\right)\mathrm{d}V(t) \\ &= \frac{C}{2}(V_1 - V_2)(V_1 + V_2 - 2V_{\mathrm{dd}}). \end{aligned}$$

The effective transition number for rising signal transitions is defined as

$$\hat{N}_i(\mathrm{rising}) = \frac{(V_1 - V_2)(V_1 + V_2 - 2V_{\mathrm{dd}})}{V_{\mathrm{dd}}^2}N_i \tag{5}$$

where N_i is the transition number for node i including both functional transitions and glitches. Note that $\hat{N}_i$ becomes equal to N_i when only full swing is considered. Similarly, the formula for power dissipation of a falling signal transition can be derived and the effective transition number is defined as

$$\hat{N}_i(\mathrm{falling}) = \frac{V_2^2 - V_1^2}{V_{\mathrm{dd}}^2}N_i. \tag{6}$$

Switching power considering partial swings is then calculated as

$$P_{\mathrm{sw}} = 0.5fV_{\mathrm{dd}}^2\sum_{i=1}^{n} C_i\hat{E}_i \tag{7}$$

$$\hat{E}_i = \frac{\hat{N}_i}{\mathrm{cycles}} \tag{8}$$

where $\hat{E}_i$ is the effective transition density and $\hat{N}_i$ is the total effective transition number in all the simulation cycles. When the input glitch is very narrow, the output glitch will have a very small amplitude and hence does not contribute to the total effective transition number. In this case, the proposed glitch power model naturally filters out narrow glitches, known to be the effect of the inertial gate delay. Note that effective transition density is also used in the macromodels for LUTs to calculate LUT dynamic power considering partial swings.

C. Static Power

Static power is also called leakage power. According to [26], the leakage power in a nanoscale CMOS device includes reverse-biased leakage, subthreshold leakage power, drain-induced barrier lowering leakage, gate tunneling leakage, gate-induced drain leakage, etc. The total leakage power of a logic gate is a function of technology, temperature, static input vector, and stack effect of the gate type. The recent FPGA power model [5] calculates the subthreshold leakage current by using a formula. However, they simply assume the gate-source voltage for all the OFF transistors to be half of the threshold voltage, which is usually not true when stack effect is considered. SPICE simulation is used to obtain the leakage power due to various device level mechanisms. The average leakage power assuming all the input vectors have the same probability of occurrence is used in the proposed power model. Because "gate boosting" is applied [18] to interconnect switches in the routing channels and compensate the logic "1" degradation of negative channel metal oxide semiconductor (NMOS) pass transistor,[2] either V_{dd} or GND is applied as the input signals in the SPICE simulation for global interconnect leakage power. The local interconnect multiplexers inside logic blocks have not adopted gate boosting in the proposed circuit design. Therefore, the proposed power model for local interconnects gives larger leakage power due to level degradation. Since the number of all possible input vectors increases exponentially with the number of inputs for LUTs, it is infeasible to try all the input vectors and get the average leakage power. Different input vectors are mapped into a few typical vectors with representative Hamming distances and SPICE simulation is performed only for these typical vectors to build macromodels. SPICE simulation is performed for LUT sizes ranging from three to seven and buffers of various sizes in global/local interconnects, and then static power macromodels are built.

D. Overall Power Calculation

The power calculation using the mixed-level power model is summarized in Fig. 9. A gate-level netlist (the BC-netlist discussed in Section IV-A) back-annotated with gate capacitance and wire capacitance is used to begin with. Random input vectors are generated according to the specified signal probability and transition probability. A cycle-accurate simulator with glitch analysis is used to calculate the power for each component in an FPGA. During each simulation cycle, the effective transition number for the output signal of an interconnect buffer or access signal to an LUT is counted, and then the dynamic power in that cycle is calculated and added. Since leakage power always exists, even if there is a signal transition, the leakage power for interconnect buffers is also added. The leakage power for LUTs is not added in that cycle because the dynamic power macromodel based on SPICE simulation has already taken that into account. If there is no signal transition for an interconnect buffer or no

[2]Other techniques such as weak-pull-up keeper transistor can also be used to avoid logic "1" degradation in NMOS pass transistor.

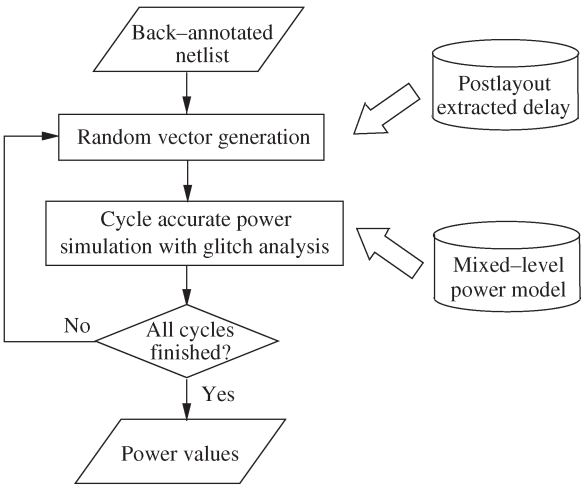

Fig. 9. Overall power calculation.

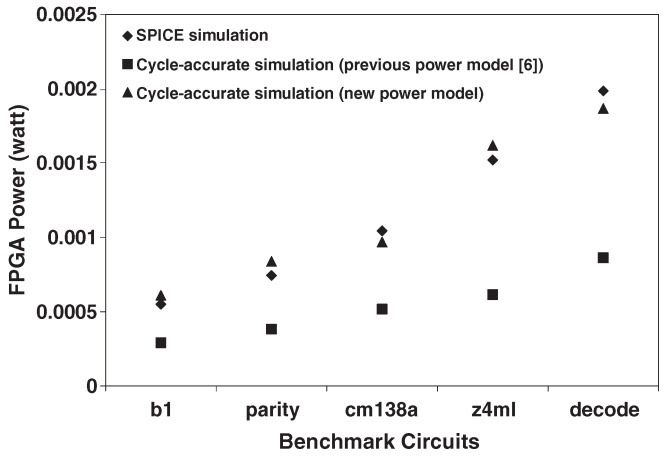

Fig. 10. Comparison between SPICE simulation and cycle-accurate power simulation with both previous power model and the proposed new power model.

access to an LUT, the static power is calculated and added. For clock power, the dynamic and leakage power for clock network buffers is calculated. The above power consumption in each cycle is accumulated until all the simulation vectors are finished.

The proposed mixed-level power model is similar to that in [6], but we use more detailed modeling for short-circuit and static power. Before applying the new power model to estimate power consumption at full-chip level, we verify the fidelity and accuracy of this cycle-accurate power simulation compared to SPICE simulation. Because it is impossible to carry out SPICE simulation for large circuits at full-chip level, we choose five circuits from the MCNC benchmark set so that the circuit size is within the capability of SPICE simulation. They are mapped into LUTs with an LUT size of four and packed into clusters with a cluster size of four. The largest circuit occupies six clusters, and the smallest circuit occupies two clusters. Fig. 10 compares the power model from [6] and the new power model in this paper to SPICE simulation. The power model in [6] achieves high fidelity but consistently underestimates the total FPGA power. With the proposed new power model, high fidelity is maintained and the absolute error is reduced to 8% on average for the five circuits.

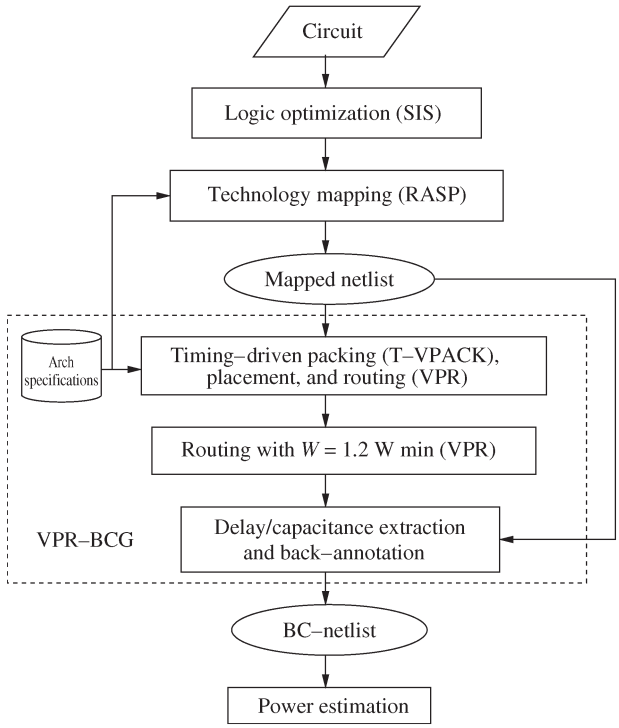

Fig. 11. FPGA power analysis framework (fpgaEVA-LP2).

IV. Power Analysis Framework and FPGA Power Characteristics

A. Power Analysis Framework fpgaEVA-LP2

Power analysis framework fpgaEVA-LP2 is built using the new power model and show the overall analysis flow in Fig. 11. For a given circuit, SIS is used [27] to perform the technology-independent logic optimization and Flowmap [28] in RASP [29] is used to conduct the technology mapping. The physical design in VPR [18] is then carried out, including timing-driven packing, placement, and routing. VPR generates FPGA array whose size just fits the given benchmark circuit. Further, VPR decides the routing channel width W as $W = 1.2W_{\min}$, and $W_{\min}$ is the minimum channel width required to route the given benchmark successfully. This means that VPR is customizing the FPGA for each benchmark so that it reflects the "low-stress" routing situation that usually occurs in commercial FPGAs for "average" circuits. The same flow is applied in fpgaEVA-LP2 and the BC-netlist back-annotated with postlayout resistance and capacitance is generated. The BC-netlist is further used to perform timing and power analysis.

Both delay and capacitance values in the BC-netlist are extracted for the elements of logic blocks and interconnects. The original VPR only cares about the delay from the source to each sink in every routing net. The intermediate routing buffers do not appear in the VPR timing graph. However, load capacitance is needed for routing buffers to calculate their power consumption. As shown in Fig. 12, the routing buffers usually separate a routing net into several parts. Each part of the net may consist of one or several wire segments that are connected by either pass-transistors or buffers. For example, buffer X in Fig. 12 has three fanout branches. Branch b_1 has only one wire segment,

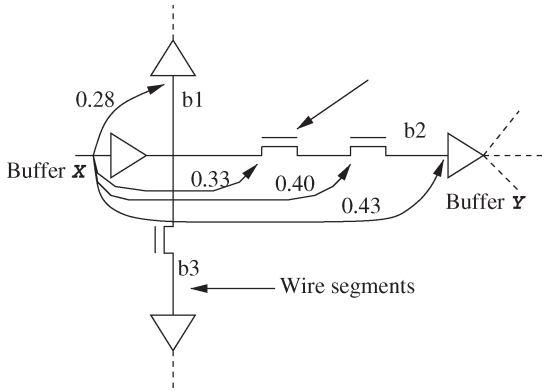

Fig. 12. Example for wire delay calculation (delay values are in nanoseconds).

TABLE VI
LOGIC BLOCK AND ROUTING ARCHITECTURES STUDIED IN OUR EXPERIMENTS

Logic block architectures	
LUT size k	3 - 7
Cluster size N	6, 8, 10, 12
Routing architecture (default in VPR)	
Wire segmentation	uniform length 4
Type of routing switch	50% tristate buffers and 50% pass transistors

while branch b_2 and b_3 have three and two wire segments, respectively. Capacitance extraction is carried out in a wire-by-wire fashion and all the capacitances of the buffer fanout branches were lumped into its load capacitance. Fig. 12 also shows how the delay along each fanout branch for buffer X is modeled. Taking branch b_2 as an example, RC delays are calculated segment-by-segment considering attached pass-transistor switches and finally obtain the delay from the input of buffer X to the input of buffer Y.

Initially, the basic circuit elements in the BC-netlist are just LUTs. The buffers used in the local wires are then inserted inside logic blocks or those used in the routing tracks. Therefore, a one-to-one correspondence is maintained between each basic circuit element (including interconnect buffers) and each extracted delay/capacitance value. The logic function of the basic circuit elements and the delay between two connected basic circuit elements are used in switching activity calculation and glitch analysis. The extracted capacitances in the BC-netlist are used for power calculation.

The proposed power analysis framework fpgaEVA-LP2 can be used to investigate the impact of circuits, architectures, and CAD algorithms upon FPGA power dissipation. In the following, fpgaEVA-LP2 is used to study the power characteristics of existing FPGA architectures. Table VI presents the FPGA architectures studied in the experiments. A suite of logic block architectures with different cluster size N and LUT size k is examined. For all logic block architectures, the same routing architecture is used as the default one in VPR, where wire segmentation length is four logic blocks, and 50% of routing switches are tristate buffers and the others are pass transistors. In all the experiments, 0.5 W is used for the logic block input flexibility $F_c(\text{input})$ and 0.25 W for the logic block output flexibility $F_c(\text{output})$, where W is the channel width

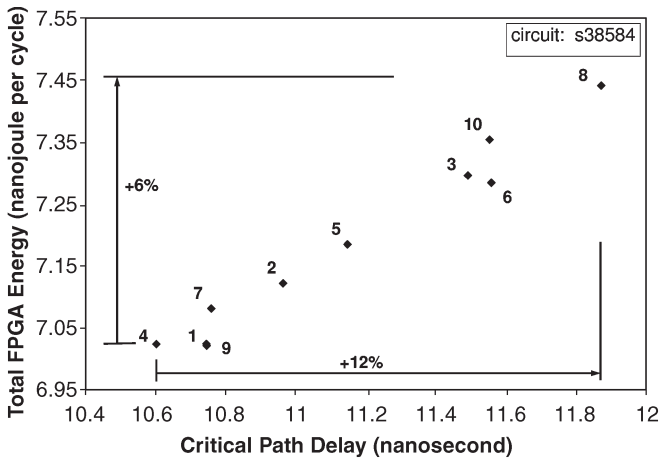

Fig. 13. VPR random seed versus FPGA delay and energy for circuit s38584 (cluster size $= 10$, LUT size $= 4$, default routing architecture in VPR).

in track number. The FPGA delay and power are presented in geometric mean over 20 largest MCNC benchmarks. The power breakdown is presented in the arithmetic average over 20 benchmarks.

B. Impact of Random Seed in VPR

In the proposed power analysis framework fpgaEVA-LP2, VPR [18] is used to place and route benchmark circuits. The placement tool in VPR applies simulated annealing algorithm with a specified initial random seed. A different seed can lead to a different placement and routing result, and it may further affect the circuit delay and power. To study the impact of VPR random seed, the same benchmark circuit is placed and routed ten times, and a different VPR random seed is used each time. The delay and power variation for these VPR runs are then investigated. Fig. 13 shows the result for a large circuit s38584. The seed value is labeled beside each data point. The critical path delay variation is 12% (from 10.60 to 11.87 ns) and the energy variation is 6% (from 7.021 to 7.441 nJ/cycle). Furthermore, Table VII summarizes the delay and energy variation for the MCNC benchmark set with cluster size 10 and LUT size 4. On average, the delay variation is 22.08% and the power variation is 15.33%. Note that the min-delay VPR run often consumes lower energy. Considering the relatively larger delay variation due to VPR random seeds, the min-delay VPR run is always used for each benchmark circuit among all VPR seeds, and FPGA power characteristics are presented for the rest of the paper.

C. Transition Density, Glitch Power, and Short-Circuit Power

Since glitch power is due to the spurious transitions in a circuit, the transition density calculation in the power simulation should consider these spurious transitions. The average effective transition density per circuit node is presented for two large benchmark circuits in Table VIII. "bigkey" is a combinational circuit and "s38584" is a sequential circuit. The transition density value without glitch analysis is compared to that with glitch analysis. Clearly, the calculation without

TABLE VII
FPGA ENERGY AND DELAY VARIATION DUE TO VPR RANDOM SEED FOR 20 MCNC BENCHMARK CIRCUITS (CLUSTER SIZE = 10, LUT = 4, DEFAULT ROUTING ARCHITECTURE)

Circuit	Maximum energy (nJ/cycle)	Minimum energy (nJ/cycle)	Energy variation	Maximum delay (ns)	Minimum delay (ns)	Delay variation
alu4	2.000	1.884	6.22%	10.77	9.64	11.82%
apex2	3.425	2.957	15.85%	15.16	11.41	32.86%
apex4	1.632	1.403	16.30%	12.32	10.09	22.06%
bigkey	3.136	2.935	6.85%	6.29	5.75	9.52%
clma	36.549	30.005	21.81%	27.77	22.16	25.29%
des	6.195	5.817	6.51%	12.42	10.99	12.98%
diffeq	1.548	1.465	5.64%	13.18	12.30	7.13%
dsip	2.995	2.595	15.40%	6.58	5.28	24.68%
elliptic	6.740	5.571	20.98%	21.07	16.65	26.54%
ex1010	9.872	6.527	51.25%	24.90	14.88	67.30%
ex5p	1.753	1.471	19.24%	13.54	10.46	29.45%
frisc	13.521	12.280	10.11%	24.73	22.21	11.35%
misex3	2.009	1.822	10.24%	11.52	9.73	18.41%
pdc	12.710	10.237	24.16%	21.61	16.53	30.67%
s298	4.309	3.681	17.08%	27.98	22.62	23.69%
s38417	10.942	10.019	9.21%	15.39	14.25	8.01%
s38584	7.441	7.021	5.99%	11.87	10.60	11.99%
seq	2.883	2.510	14.85%	12.96	9.99	29.71%
spla	7.184	5.834	23.14%	19.00	14.34	32.47%
tseng	1.188	1.123	5.84%	12.99	12.28	5.77%
Average			15.33%			22.08%

TABLE VIII
AVERAGE TRANSITION DENSITY PER CIRCUIT NODE (CLUSTER SIZE = 8, LUT = 4)

Circuit	Average transition density (without glitch analysis)			
	Logic block	Interconnect	Global interconnect	Local interconnect
bigkey	0.836	0.465	0.447	0.470
s38584	0.694	0.316	0.300	0.323
Circuit	Average transition density (with glitch analysis)			
	Logic block	Interconnect	Global interconnect	Local interconnect
bigkey	1.893	0.602	0.582	0.608
s38584	1.182	0.362	0.347	0.368

TABLE IX
GLITCH POWER (CLUSTER SIZE = 8)

k	Glitch power (percent of total power)
3	12.33%
4	14.39%
5	13.01%
6	15.43%
7	18.91%

glitch analysis underestimates the transition density. The average percentage of glitch power is further presented, for each LUT size k, over a series of benchmarks in Table IX. The experiments show that glitch power is an important part of total FPGA power, and its portion can be as large as 19% in the experiments. The short-circuit power depends on both switching activity and signal transition time. It has been found that the signal transition time in the FPGA design is large and short-circuit power is a significant power component. Table X presents the various power components for global interconnects and illustrates that both short-circuit and leakage power are significant and vary a lot between different circuits.

D. Impact of Logic Block Architecture

In this section, the impact of logic block architecture (i.e., LUT size and cluster size) on delay and power is studied. Fig. 14 shows the critical path delay for different cluster and LUT sizes. In general, a larger LUT size leads to smaller critical path delay because the number of LUTs in series on the critical path decreases. However, for large cluster size such as size 12, the critical path delay increases as the LUT size increases (see LUT sizes 4–7). This is because the delay through a cluster increases greatly for large cluster size.

Since interconnects are usually the dominant FPGA resources, FPGA interconnect energy is further shown in Fig. 15. As the LUT size increases, the total number of LUT input pins in a cluster increases and the number of local interconnect buffers and multiplexers (MUXes) also increases in order to fully connect these LUTs. This leads to the increase of local interconnect energy. On the other hand, the global interconnect energy decreases when the LUT size increases. This is because fewer LUTs and clusters are needed to implement the given circuit, which leads to smaller FPGA array size and less global interconnect resource. For the same cluster size, the results show that LUT size 4 leads to the minimum interconnect energy. Cluster size also affects the interconnect energy. A larger cluster size increases local interconnect energy but reduces global interconnect energy. Fig. 15 shows that the total interconnect energy usually increases as cluster size increases, but the energy difference is not very large except for seven-input LUTs. Leakage power in nanometer technology is significant, and the FPGA leakage energy is presented in Fig. 16. Leakage energy is mainly decided by total FPGA resources including logic blocks and interconnects. Since it has been shown in [14] that LUT size 4 achieves the highest total-area efficiency, it is expected that LUT size 4 also achieves minimum leakage energy, and this is verified in Fig. 16. Considering all the power dissipation components, total FPGA energy is presented in Fig. 17. Clearly, the results for all the cluster sizes consistently show that the LUT

TABLE X
GLOBAL INTERCONNECT POWER FOR TWO CIRCUITS (CLUSTER SIZE = 8, LUT = 4,)

Circuit	Total global interconnect power (watt)	Global interconnect leakage power (%)	Global interconnect dynamic power (percent)	
			Switching power	Short-circuit power
bigkey	0.202315	42.9%	15.6%	41.5%
s38484	0.36493	62.4%	11%	26.6%

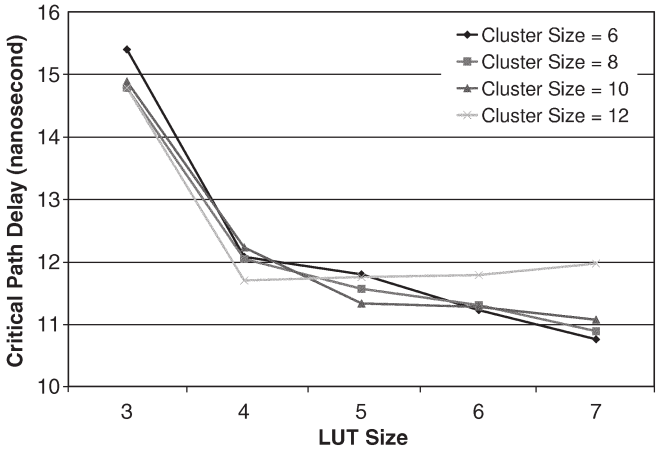

Fig. 14. Impact of logic block architecture on critical path delay.

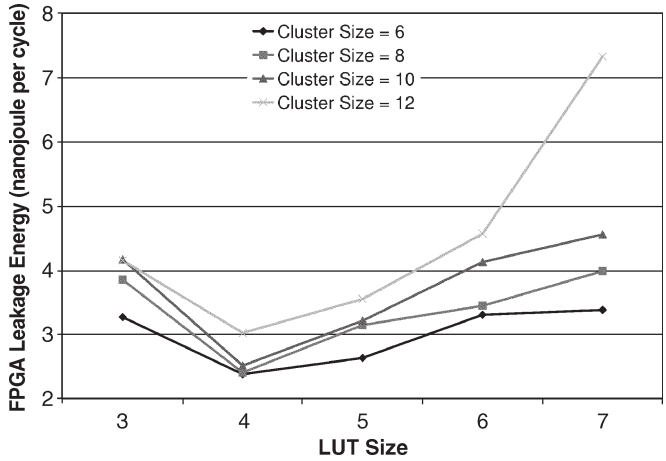

Fig. 16. Impact of logic block architecture on FPGA leakage energy.

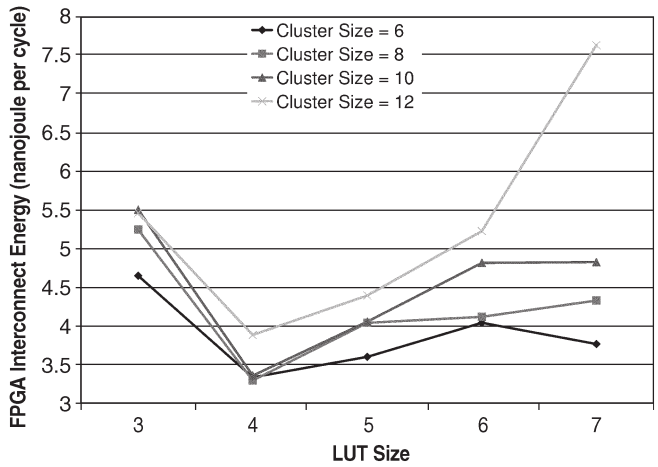

Fig. 15. Impact of logic block architecture on FPGA interconnect energy.

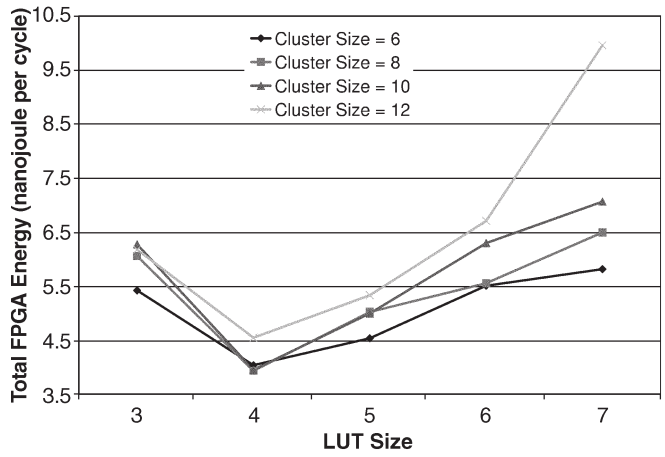

Fig. 17. Impact of logic block architecture on total FPGA energy.

size 4 gives the lowest total FPGA energy compared to other LUT sizes.

Fig. 18 further plots energy and delay for all logic block architectures and shows the tradeoff between FPGA power and performance. The X-axis is critical path delay and the Y-axis is total FPGA energy. Each data point in the figure represents a specific logic block architecture (N, k), where N is the cluster size and k is the LUT size. Inferior data points are defined as those with both larger critical path delay and larger FPGA energy. After pruning out all the inferior data points, the remaining ones represent the dominant solutions in the power–performance tradeoff space. The superior data points are highlighted and connected to obtain the energy–delay tradeoff curve. It shows that the min-delay logic block architecture has the cluster size 6 and LUT size 7, and the min-energy logic block architecture has the cluster size 8 and LUT size 4. The energy consumption difference between these two architectures is 48%, and the critical path delay difference is 12%. Fig. 19 presents the FPGA energy and area for all the logic block architectures, which shows that a larger FPGA area usually leads to larger FPGA energy, and the proposed min-energy architecture ($N = 8$, $k = 4$) is also the min-area architecture. Commercial FPGAs such as Xilinx Virtex-II [7] coincidently uses a cluster size of 8 and an LUT size of 4. Existing commercial architectures may have used min-area solution and turn out to be a min-energy solution.

E. Power Dissipation Breakdown

Fig. 20 presents the power breakdown for both min-delay and min-energy FPGA architectures found in the experiments. The total FPGA power is first broken down into clock power, logic power, local interconnect power, and global interconnect power. The logic power is the power consumed by LUTs, LUT configuration static random access memory (SRAM) cells, and flip-flops. The local interconnect power is the power

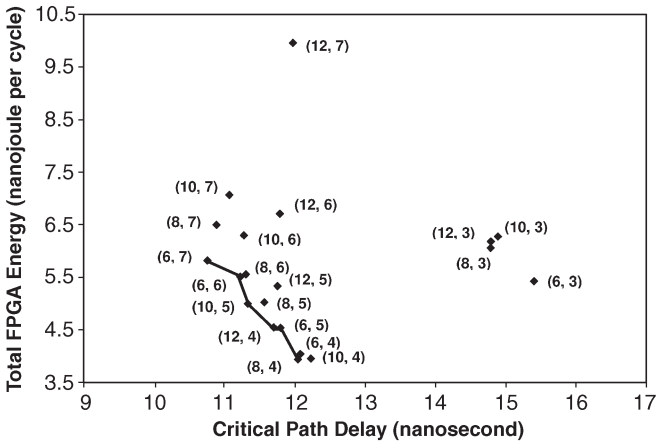

Fig. 18. FPGA energy versus delay under various logic block architectures.

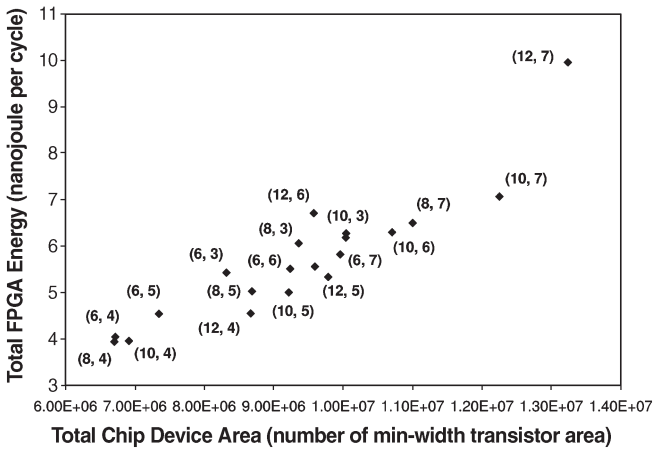

Fig. 19. FPGA energy versus area under various logic block architectures.

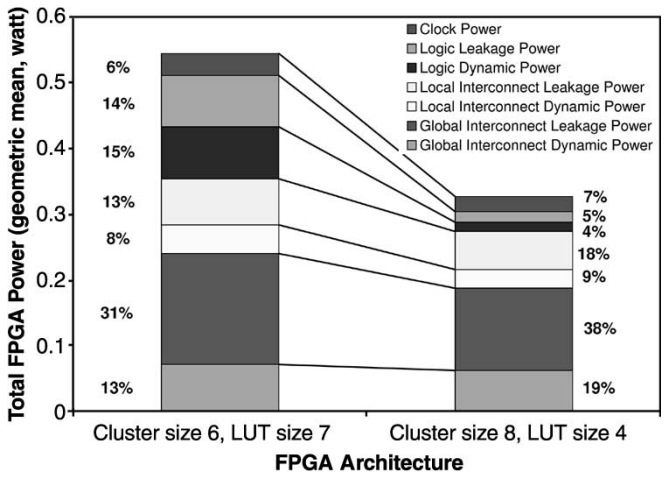

Fig. 20. FPGA power breakdown for min-delay architecture (i.e., cluster size $= 6$ and LUT size $= 7$) and min-energy architecture (i.e., cluster size $= 8$, LUT size $= 4$).

TABLE XI
UTILIZATION RATE OF INTERCONNECT SWITCHES

Circuit	Total interconnect switches	Unused interconnect switches	Utilization rate
alu4	36478	31224	14.40%
apex4	43741	37703	13.80%
bigkey	63259	57017	9.87%
clma	653181	593343	9.16%
des	87877	79932	9.04%
diffeq	42746	36974	13.50%
dsip	75547	70138	7.16%
elliptic	140296	125800	10.33%
ex5p	45404	39288	13.47%
frisc	238853	216993	9.15%
misex3	39928	33819	15.30%
pdc	268167	238610	11.02%
s298	43725	37641	13.91%
s38417	243315	216577	10.99%
s38584	195363	174460	10.70%
seq	61344	53173	13.32%
spla	153235	134991	11.91%
tseng	29051	25026	13.85%
Average			11.90%

of internal routing wires, buffers, and MUXes inside logic blocks. Power of routing wires outside logic blocks, programmable interconnect switches in the routing channels, and their configuration SRAM cells contribute to global interconnect power. The clock power is merely the power of a simple H-tree network. For each power component except clock power, it is further broken down into leakage power and dynamic power.

Compared to the min-delay architecture ($N = 6$, $k = 7$), the min-energy architecture ($N = 8$, $k = 4$) reduces logic power significantly because it has a much smaller LUT size. A smaller LUT size reduces the logic power because it increases LUT utilization rate and reduces the number of LUT configuration SRAM cells. The min-energy architecture also reduces global interconnect leakage power because its larger cluster size reduces total global interconnect resources. For both architectures, total interconnect power is dominant and interconnect leakage power is the major component of interconnect power. This is because the utilization rate of FPGA interconnect switches is extremely low (see Table XI) and the unused interconnect switches contribute a significant amount of leakage power. Note that this low utilization rate is intrinsic for field programmable devices. It is alarming that interconnect leakage power can be over 50% of total FPGA power for the proposed min-energy FPGA architecture. Therefore, it is believed that leakage power reduction is critical for future power-efficient FPGAs. The clock power is only a small portion in the experiments, and this may be due to the simplified H-tree assumption in this paper.

V. CONCLUSION AND DISCUSSIONS

A new power model for parameterized FPGA architectures has been developed. The new power model combines switch-level model for interconnects and macromodel for logic blocks and LUTs. Gate-level netlists back-annotated with post-layout capacitances and delays are generated, and cycle-accurate power simulation is performed. The glitch power is analyzed by using a detailed delay model in the cycle-accurate power simulation, and the short-circuit power is modeled as a function of signal transition time. The resulting FPGA power analysis framework is named as fpgaEVA-LP2. Experimental results have shown that fpgaEVA-LP2 achieves high fidelity compared to SPICE simulations at full-chip level and the absolute error is 8% on average.

fpgaEVA-LP2 can be used to investigate the power impact of FPGA circuits, architectures, and CAD algorithms. In this paper, fpgaEVA-LP2 has been applied to study the power characteristics of existing FPGA architectures. It is shown that total interconnect power is dominant because interconnects are normally the primary FPGA resources. Leakage power is significant because the transistors tend to be leaky in nanometer technologies and the utilization rate of FPGA interconnect switches is intrinsically low.

It has also been shown that architectural parameters such as cluster and LUT sizes significantly affect the power breakdown between logic blocks and interconnects as well as the total FPGA power. Under a fixed FPGA routing architecture (i.e., wire segment length 4 and 50% pass transistors and 50% tristate buffers in routing switches), different logic block architectures are explored and the following are obtained: 1) min-delay architecture has the cluster size 6 and LUT size 7; and 2) min-energy architecture has the cluster size 8 and LUT size 4. Compared to the min-delay architecture, the min-energy architecture reduces FPGA energy by 48% with merely 12% delay increase. Because the min-energy architecture found is similar to the architecture widely used for commercial FPGAs, novel circuits and architectures should be developed to further reduce FPGA power. Recently reported work on FPGA power reduction includes power aware CAD algorithms [30], configuration inversion for MUX leakage reduction [31], power gating of unused FPGA logic blocks [32], dual-Vdd FPGA logic blocks [9], [10], and Vdd-programmable FPGA interconnects [11]–[13], [33]. These papers have reduced FPGA leakage power and interconnect power significantly.

ACKNOWLEDGMENT

The authors would like to thank the reviewers for their insightful suggestions to make this paper better. An extended abstract of this paper was presented in [13]. D. Chen and J. Cong contributed to the initial study presented in [6].

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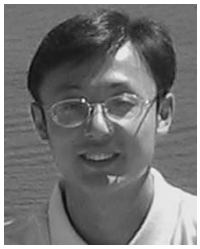

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Deming Chen, photograph and biography not available at the time of publication.

Jason Cong, photograph and biography not available at the time of publication.