Quaternary voltage-mode CMOS circuits for multiple-valued logic

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Abstract: A set of novel voltage-mode CMOS circuits for the implementation of multiple-valued logic (MVL) systems is introduced. The circuit level implementation of the multiple-valued logic operators: logical sum, logical product, level-up, level-down and level conversions are presented. The mathematical properties of the latter operator are formally proved. The proposed multiple-valued logic circuits exhibit zero static power consumption, do not use clocking, and function on any arithmetic base. The proposed circuits consist of appropriately constructed enhancement-mode and depletion-mode 1.5μm MOSFETs. Simulation of the introduced quaternary logic voltage-mode CMOS circuits, using SPICE, indicates improved performance (higher speeds) compared to existing ones.

1 Introduction

The necessity for multiple-valued logic (MVL) has been pointed out by many research workers [1–3]. Now that device minimising tactics – for better computing performance of a chip – are reaching their limits, the study of the MVL approach has become more imperative.

Implementation of MVL on a silicon chip using MOSFET technology follows two major lines: namely, current-mode and voltage-mode circuits. More specifically, in current-mode circuits the information is transferred by current. A set of basic operator circuits has been established and many function realisations (e.g. efficient multipliers [4]) based on these operators have been presented. Although generally, fast circuits are produced by this method, the corresponding implementations are power-consuming. On voltage-mode circuits, where the information is transferred by voltage levels, fewer achievements have been reported [5–16].

Despite the fact that the term CMOS is also used in MVL circuits, it does not imply zero static power consumption, which is fundamental in binary CMOS circuits. The term CMOS here means that the MVL circuit includes both NMOS and PMOS transistors. Until now, most of the proposed solutions have been characterised by static power consumption. Only a few voltage-mode circuit approaches have overcome this problem by using different kinds – various threshold voltages – of MOSFETs, the number of which depends on the base of the arithmetic system considered [5, 6]. This implies several substrate-dopings for the MOSFETs on a single chip, which eventually increase the number of IC manufacturing processes. Other approaches have overcome the static power consumption by using dynamic circuits with multiphase clocks [7, 8]. An interesting suggestion has been put forward by T. Watanabe *et al.* [7]. They used only two different threshold voltages for each transistor type (NMOS and PMOS) to implement MVL circuits, accomplishing zero static power consumption. However, in some of their proposed circuits the charge-control technique is used, which demands the use of a two-phase clock.

In this paper, a set of novel circuits implementing the operations of logical-sum, logical-product, level-up, level-down and level-conversions is introduced. Quaternary logic is chosen because of easy conversion between binary signals, derived from existing binary circuits, and quaternary signals. The proposed circuits not only embody the above-mentioned advantages of the reported approaches, i.e. only two different threshold voltages, zero static power consumption and independence on the basis of the arithmetic system, but also exhibit attractive design features. More specifically, the proposed circuits do not use the charge-control technique (or clock pulses) and, therefore, they are asynchronous. The MVL circuits introduced are simulated by SPICE-2, assuming 1.5μm technology. The corresponding waveforms of these circuits indicate higher speeds compared to those of existing ones [7]. The cost of that is an increase in the number of transistors compared with Watanabe's [7] circuits. Furthermore, circuits – derived from the above – implementing unary operators are also proposed.

2 Basic operator definitions and their algebraic properties

2.1 Operator definitions

Let the logic values of a four-valued (quaternary) system be in the set Q = {0, 1, 2, 3}. A quaternary varia-

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ble is denoted by a lower-case letter. Let a, b, c, d, x, y and z be quaternary variables.

For the sake of completeness, the definitions of the well known MVL operators with the appropriate relations are given below:

(i) The logical sum or max operator, denoted by the symbol '+', is defined as

$$\max(a,b) = a + b = \begin{cases} a & \text{if } a \geq b \\ b & \text{if } a < b \end{cases}$$

(ii) The logical product or min operator, denoted by the symbol '·', is defined as

$$\min(a,b) = a \cdot b = \begin{cases} a & \text{if } a \leq b \\ b & \text{if } a > b \end{cases}$$

(iii) The literal unary operator, ${}^{a}x^{b}$, is defined as

$${}^{a}x^{b} = \begin{cases} 3 & \text{if } a \leq x \leq b \\ 0 & \text{otherwise} \end{cases} \quad (\text{where } a < b)$$

The three operators – max, min and literal – constitute a functionally complete set.

(iv) The truncated sum operator, denoted by the symbol '⊕', is defined as

$$a \oplus b = \min(a + b, 3)$$

(where '$a + b$' denotes the conventional algebraic addition).

(v) The truncated difference operator, denoted by the symbol '⊖', is defined as

$$a \ominus b = \max(a - b, 0)$$

(where '$a - b$' denotes the conventional algebraic subtraction).

Subcases are: the truncated sum by one and the truncated sum difference by one (level-up and level-down), defined, respectively, as

$$a \oplus 1 = \min(a + 1, 3) \qquad a \ominus 1 = \max(a - 1, 0)$$

(vi) The semiliteral unary operators, ${}^{a}x$ and x^{b}, are, respectively, defined as

$${}^{a}x = \begin{cases} 3 & \text{if } x \geq a \\ 0 & \text{if } x < a \end{cases} \qquad x^{b} = \begin{cases} 3 & \text{if } x \leq b \\ 0 & \text{if } x > b \end{cases}$$

Apparently, the literal operator results from the combination of the two semiliterals as follows:

$${}^{a}x^{b} = \min({}^{a}x, x^{b}) = {}^{a}x \cdot x^{b} \tag{1}$$

(vii) Finally, the level-conversion unary operators, ${}^{a}x|_{d}^{c}$ and $x^{b}|_{d}^{c}$ are, respectively, defined as

$${}^{a}x|_{d}^{c} = \begin{cases} c & \text{if } x \geq a \\ d & \text{if } x < a \end{cases} \qquad x^{b}|_{d}^{c} = \begin{cases} c & \text{if } x \leq b \\ d & \text{if } x > b \end{cases}$$

Obviously, for $c = 3$ and $d = 0$ the semiliterals result. The level-conversion operators, whose implementation by circuits is presented later in this paper, are the ${}^{a}x|_{a}^{0}$ and $x^{b}|_{b}^{3}$, that is,

$${}^{a}x|_{a}^{0} = \begin{cases} 0 & \text{if } x \geq a \\ a & \text{if } x < a \end{cases} \qquad x^{b}|_{b}^{3} = \begin{cases} 3 & \text{if } x \leq b \\ b & \text{if } x > b \end{cases}$$

Using the latter level-conversion operators, the semiliteral operators can be obtained and, subsequently, the literals can be produced from eqn. 1. For quaternary logic, the corresponding semiliterals are ${}^{1}x$, ${}^{2}x$, ${}^{3}x$, x^{0}, x^{1} and x^{2}. Since the operators ${}^{0}x$ and x^{3} are constants (${}^{0}x = 3$ and $x^{3} = 3$, for all $x \in$ Q), they are omitted from the derivation that follows.

2.2 Properties of the level-conversion operators

Here, some of the properties of level-conversion operators and their proofs are presented. These properties will be used for the derivation of the semiliterals.

Lemma 1: Given a variable $x \in$ Q and the constants a, c and d, belonging to Q, and that ${}^{a}x|_{d}^{c}$ denotes the level-conversion operator, it can be proved that

$${}^{a}x|_{d}^{c} = x^{a-1}\big|_{c}^{d}$$

Proof: From the definition

$${}^{a}x|_{d}^{c} = \begin{cases} c & \text{if } x \geq a \\ d & \text{if } x < a \end{cases}$$

we have

$${}^{a}x|_{d}^{c} = \begin{cases} c & \text{if } x \geq a \\ d & \text{if } x < a \end{cases} = \begin{cases} c & \text{if } x > a-1 \\ d & \text{if } x \leq a-1 \end{cases}$$

$$= \begin{cases} d & \text{if } x \leq a-1 \\ c & \text{if } x > a-1 \end{cases} = x^{a-1}\big|_{c}^{d}$$

$$\Leftrightarrow {}^{a}x|_{d}^{c} = x^{a-1}\big|_{c}^{d} \tag{2}$$

Lemma 2: Given a variable x and the constants b, c and d, it can be proved that

$${}^{x}b|_{d}^{c} = x^{b}\big|_{d}^{c}$$

Proof: From the definition of ${}^{x}b|_{d}^{c}$, we have

$${}^{x}b|_{d}^{c} = \begin{cases} c & \text{if } b \geq x \\ d & \text{if } b < x \end{cases} = \begin{cases} c & \text{if } x \leq b \\ d & \text{if } x > b \end{cases} = x^{b}\big|_{d}^{c}$$

$$\Leftrightarrow {}^{x}b|_{d}^{c} = x^{b}\big|_{d}^{c} \tag{3}$$

Lemma 3: Given a variable x and the constants a, c and d, it can be proved that

$$a^{x}|_{d}^{c} = {}^{a}x|_{d}^{c}$$

Proof: From the definition of $a^{x}|_{d}^{c}$, we have

$$a^{x}|_{d}^{c} = \begin{cases} c & \text{if } a \leq x \\ d & \text{if } a > x \end{cases} = \begin{cases} c & \text{if } x \geq a \\ d & \text{if } x < a \end{cases} = {}^{a}x|_{d}^{c}$$

$$\Leftrightarrow a^{x}|_{d}^{c} = {}^{a}x|_{d}^{c} \tag{4}$$

Lemma 4: Given a variable x and a constant c, it can be proved that

$${}^{3}x|_{c}^{x} = {}^{3}x|_{c}^{3}$$

Proof: Indeed,

$${}^{3}x|_{c}^{x} = \begin{cases} x & \text{if } x \geq 3 \\ c & \text{if } x < 3 \end{cases} \overset{\text{if } x \geq 3 \Rightarrow x = 3}{=} \begin{cases} 3 & \text{if } x \geq 3 \\ c & \text{if } x < 3 \end{cases}$$

$$= {}^{3}x|_{c}^{3}$$

$$\Leftrightarrow {}^{3}x|_{c}^{x} = {}^{3}x|_{c}^{3} \tag{5}$$

It is, also, easy to prove that

$$x^{2}|_{x}^{c} = x^{2}|_{3}^{c} \tag{6}$$

Lemma 5: Given a variable x and a constant c, it can be proved that

$${}^{1}x|_{x}^{c} = {}^{1}x|_{0}^{c}$$

Proof: Indeed,

$${}^{1}x|_{x}^{c} = \begin{cases} c & \text{if } x \geq 1 \\ x & \text{if } x < 1 \end{cases} \overset{\text{if } x < 1 \Rightarrow x = 0}{=} \begin{cases} c & \text{if } x \geq 1 \\ 0 & \text{if } x < 1 \end{cases}$$

$$= {}^{1}x|_{0}^{c}$$

$$\Leftrightarrow {}^{1}x|_{x}^{c} = {}^{1}x|_{0}^{c} \tag{7}$$

It is, also, easy to prove that

$$x^{0}|_{c}^{x} = x^{0}|_{c}^{0} \tag{8}$$

Successive application of the level-conversion operators leads to the following properties.

Lemma 6: Given a variable x and the constants a, b, c and d, it can be proved that

$$\left({}^{a}x|_{a}^{0}\right)^{b}\Big|_{d}^{c} = \begin{cases} c & \text{if } a \le b \\ {}^{a}x|_{d}^{c} & \text{if } a > b \end{cases}$$

Proof: Working successively on x we obtain

$$\left({}^{a}x|_{a}^{0}\right)^{b}\Big|_{d}^{c} = \left(\begin{cases} 0 & \text{if } x \ge a \\ a & \text{if } x < a \end{cases}\right)^{b}\Big|_{d}^{c}$$

$$= \begin{cases} c & \text{if } \left(\begin{cases} 0 & \text{if } x \ge a \\ a & \text{if } x < a \end{cases}\right) \le b \\ d & \text{if } \left(\begin{cases} 0 & \text{if } x \ge a \\ a & \text{if } x < a \end{cases}\right) > b \end{cases}$$

$$= \begin{cases} c \begin{cases} (\text{if } x \ge a) \text{ and } (\text{if } 0 \le b) \\ \quad (\text{or}) \\ (\text{if } x < a) \text{ and } (\text{if } a \le b) \end{cases} \\ d \begin{cases} (\text{if } x \ge a) \text{ and } (\text{if } 0 > b) \\ \quad (\text{or}) \\ (\text{if } x < a) \text{ and } (\text{if } a > b) \end{cases} \end{cases}$$

Two cases are considered:

(i) If $a \le b$, taking into account that $0 \le b$ always, it holds that

$$\left({}^{a}x|_{a}^{0}\right)^{b}\Big|_{d}^{c} = c \begin{cases} (\text{if } x \ge a) \text{ and } (\text{if } 0 \le b) \\ \quad (\text{or}) \\ (\text{if } x < a) \text{ and } (\text{if } a \le b) \end{cases} = c$$

$$\Leftrightarrow \left({}^{a}x|_{a}^{0}\right)^{b}\Big|_{d}^{c} = c \tag{9}$$

(ii) If $a > b$, it holds that

$$\left({}^{a}x|_{a}^{0}\right)^{b}\Big|_{d}^{c} = \begin{cases} c & (\text{if } x \ge a) \text{ and } (\text{if } 0 \le b) \\ d & (\text{if } x < a) \text{ and } (\text{if } a > b) \end{cases}$$

$$= \begin{cases} c & \text{if } x \ge a \\ d & \text{if } x < a \end{cases} = {}^{a}x|_{d}^{c}$$

$$\Leftrightarrow \left({}^{a}x|_{a}^{0}\right)^{b}\Big|_{d}^{c} = {}^{a}x|_{d}^{c} \tag{10}$$

Similarly, it can easily be proved that

$${}^{a}\left(x^{b}|_{b}^{3}\right)\Big|_{d}^{c} = c \quad \text{if } a \le b \tag{11}$$

and

$${}^{a}\left(x^{b}|_{b}^{3}\right)\Big|_{d}^{c} = x^{b}|_{d}^{c} \quad \text{if } a > b \tag{12}$$

2.3 Derivation of semi-literals

Because of the fact that only two of the level-conversion operators – ${}^{a}x|_{a}^{0}$ and $x^{b}|_{b}^{3}$ – are implemented in this work, the derivation of the semiliterals from the above operators is given below:

(i) ${}^{1}\mathbf{x}$:

$$1^{x}|_{x}^{3} \overset{\text{because of eqn.4}}{=} {}^{1}x|_{x}^{3} \overset{\text{because of eqn.7}}{=} {}^{1}x|_{0}^{3} = {}^{1}x$$

$$\Leftrightarrow 1^{x}|_{x}^{3} = {}^{1}x \tag{13}$$

(ii) ${}^{2}\mathbf{x}$:

$$\left({}^{2}x|_{2}^{0}\right)^{0}\Big|_{0}^{3} \overset{\text{eqn.10}}{=} {}^{2}x|_{0}^{3} = {}^{2}x$$

$$\Leftrightarrow \left({}^{2}x|_{2}^{0}\right)^{0}\Big|_{0}^{3} = {}^{2}x \tag{14}$$

(iii) ${}^{3}\mathbf{x}$:

$${}^{x}2|_{x}^{0} \overset{\text{eqn.3}}{=} x^{2}|_{x}^{0} \overset{\text{eqn.6}}{=} x^{2}|_{3}^{0} \overset{\text{eqn.2}}{=} {}^{3}x|_{0}^{3} = {}^{3}x$$

$$\Leftrightarrow {}^{x}2|_{x}^{0} = {}^{3}x = {}^{3}x^{3} \tag{15}$$

(iv) $\mathbf{x}^{0}$:

$$x^{0}|_{0}^{3} = x^{0} = {}^{0}x^{0} \tag{16}$$

(v) $\mathbf{x}^{1}$: Let $y = {}^{2}x|_{2}^{0}$

Then

$$1^{y}|_{y}^{3} \overset{\text{eqn.4}}{=} {}^{1}y|_{y}^{3} \overset{\text{eqn.7}}{=} {}^{1}y|_{0}^{3} \overset{\text{eqn.2}}{=} y^{0}|_{3}^{0} = \left({}^{2}x|_{2}^{0}\right)^{0}\Big|_{3}^{0} \overset{\text{eqn.10}}{=} {}^{2}x|_{3}^{0} \overset{\text{eqn.2}}{=} x^{2-1}|_{0}^{3} = x^{1}|_{0}^{3} = x^{1}$$

$$\Leftrightarrow 1^{y}|_{y}^{3} = x^{1} \tag{17}$$

(vi) $\mathbf{x}^{2}$:

$${}^{3}x|_{3}^{0} \overset{\text{eqn.2}}{=} x^{2}|_{0}^{3} = x^{2} \Leftrightarrow {}^{3}x|_{3}^{0} = x^{2} \tag{18}$$

3 The proposed MVL CMOS circuits

3.1 Electrical and technology considerations

As has already been mentioned, a quaternary arithmetic system is used in this work. The relation between logical values and voltage values is shown in Table 1. For simplicity, the voltage values coincide with the corresponding logical values.

Table 1: Correspondence between logical values and voltages

Logical values	0	1	2	3
Voltage, V	0.0	1.0	2.0	3.0

The proposed circuits are constructed using both enhancement-mode and depletion-mode MOSFETs of 1.5μm technology. We verify the operation of these circuits using the SPICE 2 simulator (level 3 analysis is used). To set the desired threshold voltage for each transistor, its substrate doping model parameter (NSUB) is varied. The oxide thickness parameter (TOX), which also affects the threshold voltage, is constant, as defined by the technology considered. The different kinds of transistor and the corresponding parameters are shown in Table 2.

Because of IC implementation, the substrate voltages (V_B) of the n-MOSFET and p-MOSFET transistors are set to 0.0V and 3.0V, respectively. A threshold voltage shift, due to substrate (bulk)-source bias voltage (V_{BS}) is expected, because it is always $V_B \le V_s$ for the n-MOSFETs and $V_B \ge V_s$ for the p-MOSFETs.

Fig. 1 depicts the threshold voltage (V_{TH}) against the bulk-source bias (V_{BS}) voltage for n-type transistors. The corresponding curves for p-type transistors are similar. These typical curves have been plotted using V_{TH} values calculated from level 1 analysis, which is less accurate than level 3 but good enough for estimation purposes. It is apparent from Fig. 1 that the corresponding changes for the depletion-mode MOSFETs are negligible. As for the enhancement-mode MOSFETs, the maximum V_{TH} (for $V_{BS} = -3$V) does not affect their switching requirements (at least one logic level difference between the gate and the source),

Table 2: 1.5 μm technology parameters of MOS transistors employed in proposed MVL circuits, which were used in SPICE simulation

Transistor type	TOX, Å	NSUB, cm^{-3}	$V_{TH,0}$, V	γ, $V^{1/2}$	φ, V
NMOS (enhancement-mode)	250	1.7×10^{16}	0.266	0.544	0.723
PMOS (enhancement-mode)	250	1.7×10^{16}	–0.266	0.544	0.723
NMOS1 (depletion-mode)	250	1×10^{11}	–0.507	0.001	0.100
PMOS1 (depletion-mode)	250	1×10^{11}	0.507	0.001	0.100

$V_{TH,0}$: zero-bias ($V_{BS} = 0$) threshold voltage
TOX = oxide thickness; φ = surface potential
NSUB = substrate doping; γ = bulk threshold parameter

because this maximum V_{TH} is less than 1 V (the smallest distance between two different logic states).

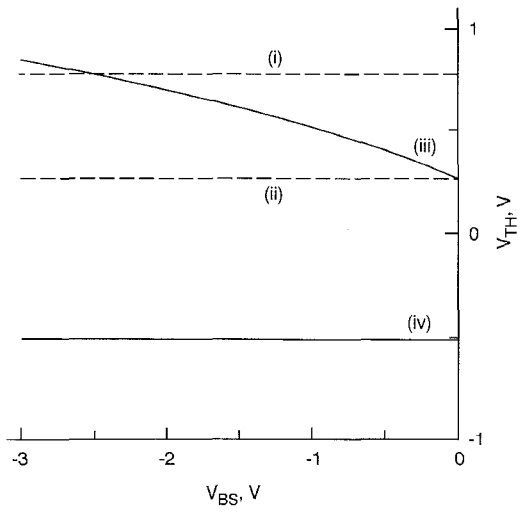

Fig. 1 *Curves of threshold voltage against bulk-source bias voltage for n-MOSFETs, derived from function* $V_{TH} = V_{TH,0} + \gamma(\sqrt{(\varphi - V_{BS})} - \sqrt{\varphi})$
(i) V_{TH} = 0.780V; (ii) V_{TH} = 0.266V; (iii) enhancement-mode MOSFET; NSUB = $1.7 \times 10^{16} cm^{-3}$; (iv) depletion-mode MOSFET: NSUB = $1 \times 10^{11} cm^{-3}$

Here, it should be stressed that the enhancement-mode MOSFETs, with NSUB = 1.7×10^{16} cm^{-3}, ensure that V_{TH} changes at around the 0.5 V level for values of V_{BS} between 0.0 and –2.5 V (dashed horizontal lines in Fig. 1). For this particular NSUB value, improved results in truncated sum by one and truncated difference by one operator circuits can be obtained.

Finally, two remarks about the proposed circuits should be made. First, there is no current flow during the stable states of the circuits, which eventually means no static power consumption. Secondly, although quaternary inputs are assumed for the max, min, level-conversion, level-up and level-down operator circuits proposed in this paper, they can function correctly on any arithmetic system basis.

3.2 MAX and MIN operator circuits

The circuits implementing the logical-sum (max) and logical-product (min) operators are shown in Fig. 2. Each circuit includes three transistors: two depletion-mode and one enhancement-mode (Table 2). To comprehend the operation of these circuits, the operation of the max operator circuit is now explained in detail. The operation of the min circuit could then be easily understood.

Let us assume that we supply the max circuit with two quaternary inputs: x and y. Table 3 shows the circuit states, after the electrical stabilisation, for the various input combinations. The transistor N_1 is blocking, when $x < y$, the way of z_1 (= y) to the node z_1'. If N_1 did not exist, there would be $z_1 = z_1'$, forcing transistor P_1 to turn on and thus decreasing the output (z_1) voltage. This would lead to a DC current flow and hence to static power consumption. Fig. 3 shows the input waveforms, along with the SPICE-simulated output waveforms for both the logical-sum and the logical-product operator circuits. The largest delay exhibited by these circuits is < 1 ns.

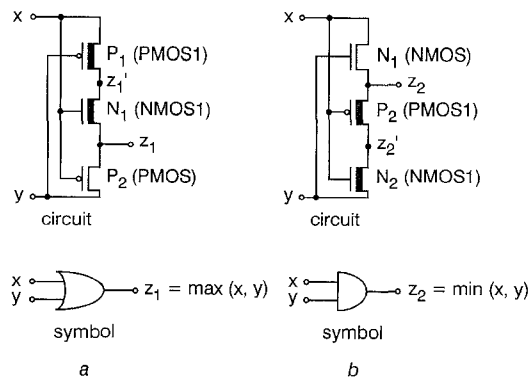

Fig. 2 *Logical sum and logical product operator circuits and their symbols*
a Sum
b Product

Table 3: Max operator circuit's states for various input combinations

Inputs	P_1	P_2	z_1'	N_1	z_1
If $x < y$	off	on	is or becomes > x	off	y
If $x \geq y$	on	off	x	on	x

3.3 Level-conversion operator circuits

The circuits implementing the level-conversions $x^b|_b^3$ and ${}^a x|_a^0$ are depicted in Fig. 4. All kinds of transistors are used in each circuit. Two circuits, a basic and an alternative, are given for each level-conversion. The reason for this variation, between basic and alternative circuits, will be explained after the presentation of the basic circuit operation. It is sufficient to explain in detail the operation of the basic level-conversion circuit $x^b|_b^3$ only, since the operation of circuit ${}^a x|_a^0$ is similar.

As we see, there is a feedback loop in the circuits. In the basic circuit of Fig. 4*a*, we adjust the width of transistor N_1 to be larger than the width of P_1. In this way, we reduce the resistance of N_1 in relation to that of P_1. Thus, whenever both N_1 and P_1 are on at the same time (which is a transition state), the z_1' voltage is almost x. Similarly, to have $z_1 \simeq b$, when both N_2 and P_2 are on, the width of transistor N_2 should be made larger than the width of P_2.

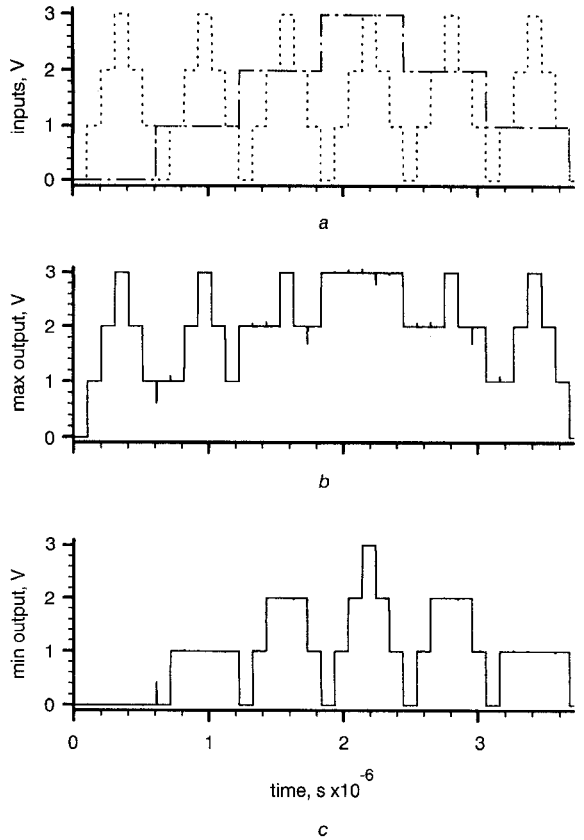

Fig. 3 *SPICE 2 simulation results of max and min operator circuits*
..... *x* input
——— *y* input
a Inputs
b max
c min

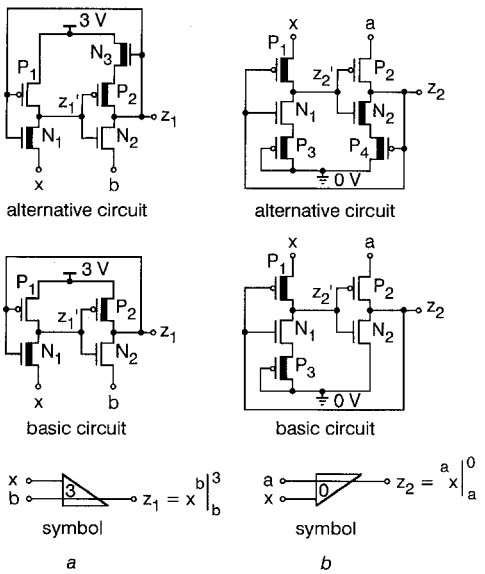

Fig. 4 *Basic and alternative circuits implementing level conversions* $x^b|_b^3$ *and* ${}^a x|_a^0$ *and their symbols*
a $x^b|_b^3$
b ${}^a x|_a^0$

The transistor P_3 plays a similar role for the circuit ${}^a x|_a^0$, i.e. it operates as a resistor, keeping the demand for wider P_1 in a low ratio, relatively to the width of N_1.

Let us suppose that we supply the above circuit with two quaternary inputs, x and b. After a transient state, every pair of inputs reaches an electrically stable state and no current flows. These stable states are shown in Table 4. Thus, for stable states, if $x \leq b$ then $z_1 = 3$, and if $x > b$ then $z_1 = b$. Therefore, the operator $x^b|_b^3$ is implemented.

Table 4: Electrically stable states of $x^b|_b^3$ operator circuit

Inputs	P_1	N_1	P_2	N_2	z_1'	z_1
If $x \leq b$	off	on	on	off	x	3
If $x > b$	on	off	off	on	3	b

During SPICE simulation, an over-voltage (about 3.3V in the output) has been observed, when $x = b = 3$ (also, an under-voltage occurs in the ${}^a x|_a^0$ a output, when $x = a = 0$). To overcome this problem, we replaced transistor P_2 (PMOS) with a PMOS1 and an NMOS1 (P_2 and N_3), connected as shown in the alternative circuit of Fig. 4*a*. A corresponding change is made in the ${}^a x|_a^0$ basic circuit by replacing transistor N_2 (NMOS) with NMOS1 and a PMOS1 (N_2 and P_4) (Fig. 4*b*, alternative circuit). The characteristic of no static current flow is preserved, and the alternative circuit functions in the same way as the basic circuit. In the circuit $x^b|_b^3$ (${}^a x|_a^0$), when $x = b = 3$ ($x = a = 0$), both P_2 and N_3 (N_2 and P_4) are on, allowing the level of 3V (0V) to appear at the output z_1 (z_2).

For semiliteral derivation, where there is never $x = b = 3$ and $x = a = 0$ for $x^b|_b^3$ and ${}^a x|_a^0$, respectively, the basic circuits can be used, because they have a smaller number of transistors. The alternative circuits can be used for the implementation of a pattern generation method [6, 7].

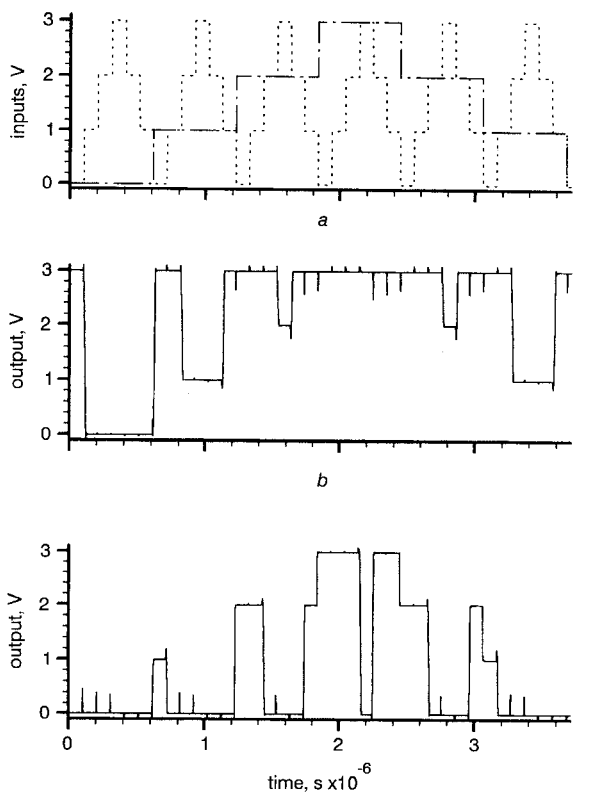

Fig. 5 *SPICE 2 simulation results of* $x^b|_b^3$ *and* ${}^a x|_a^0$ *level conversion operator alternative circuits*
..... *x* input
——— *y* input
a Inputs
b $x^b|_b^3$
c ${}^a x|_a^0$

Table 5: Width ratios and maximum delays of $x^b|_b^3$ and ${}^ax|_a^0$ operator circuits

Operator	Width ratio		Delay, ns
Basic $x^b\|_b^3$	$W_{N1}/W_{P1} = 10$	$W_{N2}/W_{P2} = 2$	11
Alternative $x^b\|_b^3$	$W_{N1}/W_{P1} = 10$	$W_{N3}/W_{N2} = 8$	17
Basic ${}^ax|_a^0$	$W_{P1}/W_{N1} = 7$	$W_{P2}/W_{N2} = 12$	13
Alternative ${}^ax|_a^0$	$W_{P1}/W_{N1} = 12$	$W_{P2}/W_{N2} = 4$ & $W_{P4}/W_{N2} = 12$	22

The input and SPICE-simulated output waveforms of both alternative circuits are shown in Fig. 5. The maximum delays and the width ratios are shown in Table 5.

3.4 Semiliteral operator circuits

Realising eqns. 13–18 by the use of level-conversion basic circuits, semiliteral operator circuits can be implemented. Fig. 6 shows all semiliterals for the quaternary logic (${}^0x = 3$ and $x^3 = 3$ are omitted, as constants).

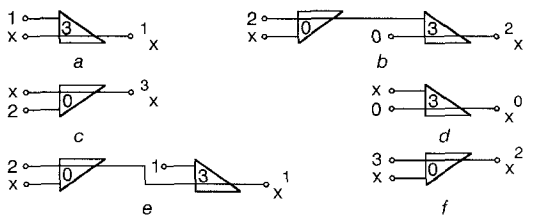

Fig. 6 *Semiliteral operator circuits*

Successive application of level-conversion operators is implemented as a sequential connection of the respective circuits. For example, according to eqn. 14, if the Fig. 4*b* basic circuit's input a is connected to 2V (logically, $a = 2$) and its output is connected to the x input of the basic circuit of Fig. 4*a*, whose b input is connected to 0V (logically, $b = 0$), then the ${}^2x$ semiliteral operator circuit is implemented.

3.5 Truncated sum and truncated difference by one operator circuits

The truncated sum by one and truncated difference by one operator circuits are shown in Fig. 7. Each circuit consists of three stages: namely, two for voltage-shift and one for voltage-correction. The $x \oplus 1$ and $x \ominus 1$ operations are analogous and, thus, only the operation of truncated sum by one operator circuit (Fig. 7*a*) is described here.

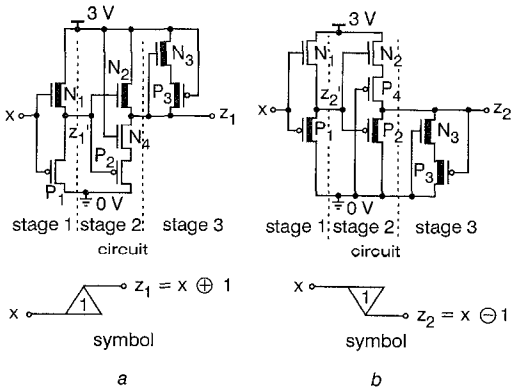

Fig. 7 *Truncated sum by one and truncated difference by one operator circuit*
a Sum
b Difference

Let us assume that we apply a voltage at the input x of the circuit of Fig. 7*a*. The sources of both transistors N_1 and P_1 are connected to the node z_1'. In stage 1, transistor N_1 preserves a voltage at z_1' at least equal to $x + 0.5$V. P_1 preserves a voltage at z_1' at most equal to $x + 0.5$V. Thus, the voltage at z_1' is stabilised at $x + 0.5$V. Similarly, stage 2 further increases the voltage of z_1' by 0.5V. Transistor N_4 is always on, until $z_1 \simeq 3$ when it turns off (it is used only for voltage correction). Eventually, the voltage at z_1 is equal to $x + 0.5 + 0.5 = x + 1$V. Obviously, if $x = 3$, then the voltages at z_1' and z_1 are equal to 3V. Epitomising, $z_1 = x \oplus 1$.

Because of the variation in V_{TH} of enhancement-mode MOSFETs (Fig. 1), there are small shifts in the output voltages, compared with the voltages that represent the logic states (Fig. 8). This phenomenon is more intense, when $x = 2$ or $x = 1$, in the $x \oplus 1$ or $x \ominus 1$ circuit, respectively. That is why the third stage and transistors N_4 or P_4 exist, to correct the output voltage at precisely 3 or 0V, respectively, when the situation $z_1 \simeq 3$ or $z_2 \simeq 0$ arises. However, the problem still exists for $x = 1$ or $x = 2$, in the $x \oplus 1$ or $x \ominus 1$ circuit, respectively, resulting in $z_1 \simeq 2$ and $z_2 \simeq 1$.

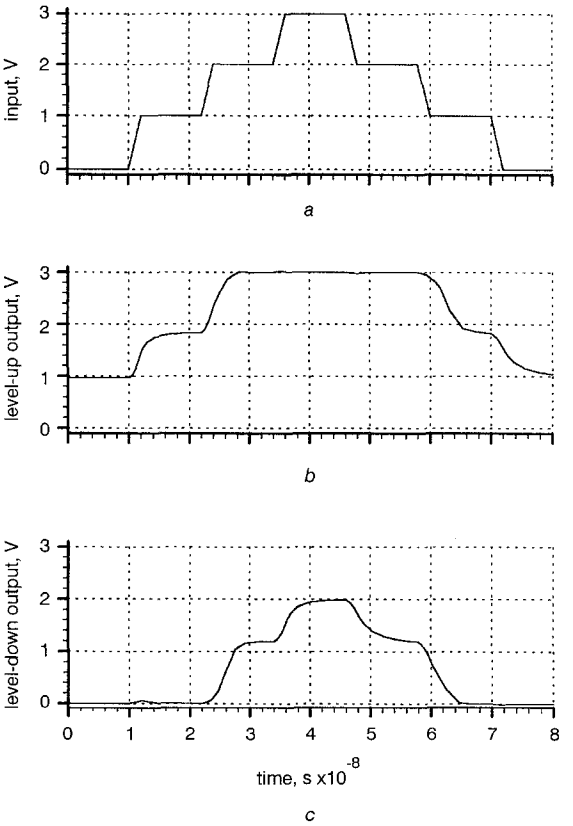

Fig. 8 *SPICE 2 simulation results of truncated sum by one and truncated difference by one operator circuit*
a Input
b Sum
c Difference

The input and the SPICE-simulated output waveforms for the above circuits are shown in Fig. 8. The

Table 6: Comparisons between Watanabe [7] circuits and those proposed here

Implemented circuits	TOX, Å	Operation's worst delay, ns					
		max	min	$x \oplus 1$	$x \ominus 1$	${}^{a}x\|_{a}^{0}$	$x^{b}\|_{b}^{3}$
Watanabe *et al.* [7]	400	< 1	< 1	≃ 300	≃ 300	≃ 400	≃ 400
Introduced here	250	< 1	< 1	6	9	22	17

maximum delays observed are ~ 6 and 9ns for the truncated sum by one and truncated difference by one operator circuits, respectively.

3.6 Comparisons

The introduced MVL circuits are compared with the ones of Watanabe *et al.* [7] in terms of speed, as shown in Table 6. Notice that both circuit implementations have zero static power consumption and use two threshold voltages. It is evident that the circuit operators – level-up, level-down and level conversions – implemented here have much higher speeds than the existing ones [7]. Also, the circuits of max and min operators have similar performance.

Furthermore, it is known that a smaller voltage supply produces smaller currents and, thus, smaller circuit speed [17]. Although in this work the maximum voltage supply is 3V, while in Watanabe *et al.*'s it is 6V, significant circuit speed improvement has been done.

4 Conclusions

Novel voltage-mode CMOS MVL circuits, for the implementation of the logical sum, logical product, level-up, level-down and level-conversion MVL operators, were presented. Although only two different threshold voltages are used and no clock signal is necessary, the proposed design of these MVL circuits leads to zero static power consumption and to circuit function on any arithmetic system basis. All the proposed circuits were simulated at level 3 of SPICE-2, and their speeds were found to be much improved compared with existing MVL circuits.

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