A 117-mm^2 3.3-V Only 128-Mb Multilevel NAND Flash Memory for Mass Storage Applications

Tae-Sung Jung, Young-Joon Choi, Kang-Deog Suh, Byung-Hoon Suh, *Member, IEEE,* Jin-Ki Kim, Young-Ho Lim, Yong-Nam Koh, Jong-Wook Park, Ki-Jong Lee, Jung-Hoon Park, Kee-Tae Park, Jhang-Rae Kim, Jeong-Hyong Yi, and Hyung-Kyu Lim, *Member, IEEE*

Abstract—**For a quantum step in further cost reduction, the multilevel cell concept has been combined with the NAND flash memory. Key requirements of mass storage, low cost, and high serial access throughput have been achieved by sacrificing fast random access performance. This paper describes a 128-Mb multilevel NAND flash memory storing 2 b per cell. Multilevel storage is achieved through tight cell threshold voltage distribution of 0.4 V and is made practical by significantly reducing program disturbance by using a local self-boosting scheme. An intelligent page buffer enables cell-by-cell and state-by-state program and inhibit operations. A read throughput of 14.0 MB/s and a program throughput of 0.5 MB/s are achieved. The device has been fabricated with 0.4-μm CMOS technology, resulting in a 117 mm^2 die size and a 1.1 μm^2 effective cell size.**

I. INTRODUCTION

WHILE the growth rate of the solid-state mass storage market has increased very rapidly, the market size has not yet met expectations. The much higher bit-cost of flash memories over magnetic media-based storage devices overshadowed many advantages of solid-state mass storage memories, such as better performance, extended rewrite cycles, increased reliability, lower power consumption, and improved portability. The NAND flash memory uses Fowler–Nordheim tunneling for both program and erase operations to reduce power consumption and to allow page based program operation, which drastically increases program throughput. Other advantages are its small cell size, achievable through a relatively simple process technology, and the better scalability of the cell coming from the simple source/drain structure. The multilevel cell concept [1], which doubles or triples the memory density without increasing the number of physical cells, combined with above advantages of the NAND flash memory can be an ideal solution for many mass storage applications. This paper describes a 128-Mb multilevel NAND flash memory storing 2 b of information per cell.

Controlling the threshold voltage ($V_{\rm th}$) distribution of programmed cells is a key issue for multilevel flash memories. In this device, the incremental step pulse programming (ISPP) scheme [2] with the stepping voltage of 0.2 V is used to obtain a very tight $V_{\rm th}$ distribution. The ISPP scheme also provides excellent process and environmental variation tolerance. The voltage drop in the array ground line of the cell array and the effects of stored data patterns in unselected cells in a selected string are the two major parasitic threshold voltage shift effects. In this device, the array ground line bouncing is minimized by reducing the reference current during the read operation down to 1.0 μA. Background pattern dependency (BPD) is suppressed by adopting a sequential programming scheme where the program sequence in a NAND string is restricted to start from the bottom cells close to the array ground line and to move to the top cells near the bitline contact. Accordingly, the threshold voltage of the programming cell is self-adjusted to the cells programmed previously. A 0.4 V $V_{\rm th}$ distribution for each state is achieved by using the above mentioned ISPP scheme and by minimizing the parasitic effects.

This 128-Mb NAND flash memory employs a wordline sweeping read (WSR) scheme which identifies one of four different cell states by sequentially changing the wordline voltage rather than having multiple reference circuits in the page buffer. Having a simple page buffer scheme is very important in NAND flash memories, since each bitline contains a page buffer circuit for page program and page read operations. The WSR scheme results in a very compact page buffer circuit to minimize the chip size.

The intelligent page buffer operation in this device allows the programmed cell $V_{\rm th}$ to be optimized on a cell-by-cell and state-by-state basis even though the cells in a page are programmed simultaneously. Each cell state is programmed sequentially and program inhibited as soon as a cell is programmed to its desired state. This state-by-state program and program inhibit operation works for each cell independently. With ISPP and the unique page buffer operation, a typical 0.5 MB/s program performance is achieved while still maintaining a very tight programmed cell threshold voltage distribution.

The program disturbance condition in the multilevel flash memory is much harsher than in the single bit case, since the $V_{\rm th}$ difference between the erased state and the programmed state is much wider. To provide sufficient disturbance margin while avoiding high voltages on program inhibited bitlines, this device implemented a local self-boosting (LSB) scheme which generates the required high inhibit channel voltage through a capacitive coupling mechanism in the NAND string. With the LSB scheme, maximum voltage on the bitline is V_{cc} during program operation.

The device is fabricated on a 0.4-μm CMOS process with a die size of 117 mm^2. The effective cell size is 1.1 μm^2. The de-

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The authors are with the Memory Design Team (NVM), Samsung Electronics Co., Ltd., Yongin-Goon, Kyungki-Do, Korea.

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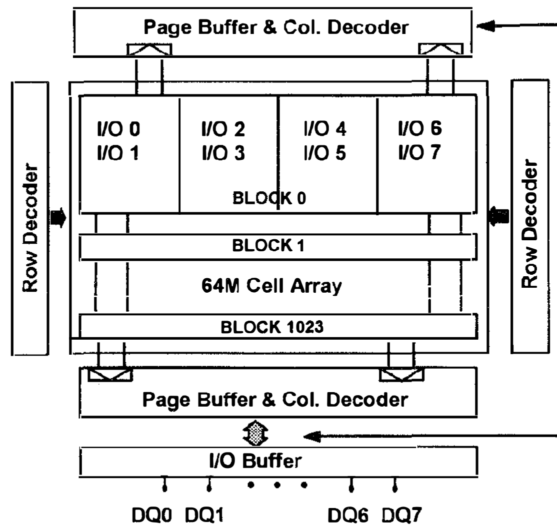


Fig. 1. Simplified core architecture of the 128-Mb NAND flash memory.

vice organization is shown in Section II. The threshold voltage distribution is explained in Section III. In Section IV, key device operations are described. The details of a program inhibit scheme is presented in Section V. Performance measurements of a fabricated device are summarized in Section VI.

II. Device Organization

Fig. 1 shows a simplified block diagram of the 128-Mb multilevel NAND flash memory. Cells are organized in a single 16-k row by (4 k + 128) column array to minimize the chip size. One block in Fig. 1 corresponds to a row of NAND strings consisting of 16 NAND cells serially connected between two string select transistors. Row decoders are split into left and right ones to accommodate the tight wordline pitch of 0.76 μm. An extra 128 b are added to each row for spare data storage which is typically used to store system data and/or ECC data. Each sense-and-latch (SL) unit of the page buffer is shared by two adjacent bit lines in order to minimize the overall page buffer size and also to ease page buffer layout. The SL sharing divides a row of 4 k cells into two pages, making the page size (512 + 16) bytes, the same as 32 Mb [2] and 64 Mb [3] NAND flash memories. To accommodate the 1.2-μm bitline pitch, page buffers are split into top and bottom banks. The page buffers in the top bank are connected to odd bitline pairs while those in the bottom bank are connected to even bitline pairs. Program and read operations are performed in page units of (512 + 16) bytes. A page corresponds to half of one row of cells. Erase is performed in a block unit of 16 kbytes corresponding to a row of NAND strings.

III. Threshold Voltage Distribution

The target threshold voltage (V_{th}) distributions of the four cell states are shown in Fig. 2. Since over-erase is not a concern in the NAND flash memory, "11" cells are sufficiently erased and their V_{th} distribution is not controlled as tightly as the three program states. Each program state has a 0.4 V V_{th} distribution width and a 0.8 V gap separating them. To achieve the target V_{th} distributions, the program scheme must be able to precisely control cell V_{th} levels. Fig. 3 shows how the V_{th} shifts from −3 V to +3 V when different step voltages (ΔV_{pgm}) are used in the ISPP scheme. It can be seen that the V_{th} shift due to each program pulse (ΔV_{th}) is directly proportional to ΔV_{pgm}. Thus, a smaller ΔV_{pgm} with a proper program inhibit scheme can result in a tighter V_{th} distribution. In this flash memory, 0.2 V ISPP is selected for precise cell V_{th} control to achieve the target V_{th} distribution of 0.4 V. However, the smaller ΔV_{pgm} also results in slower page program speed.

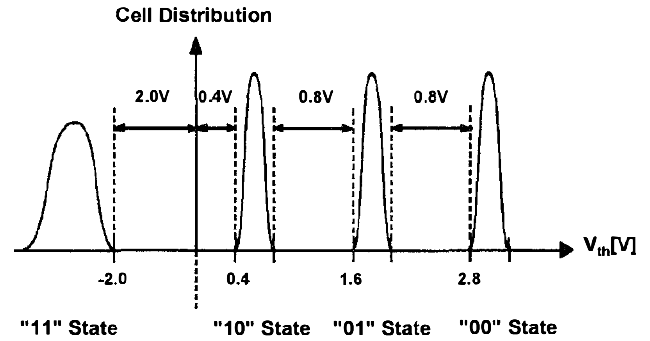


Fig. 2. Target threshold voltage distribution of four states.

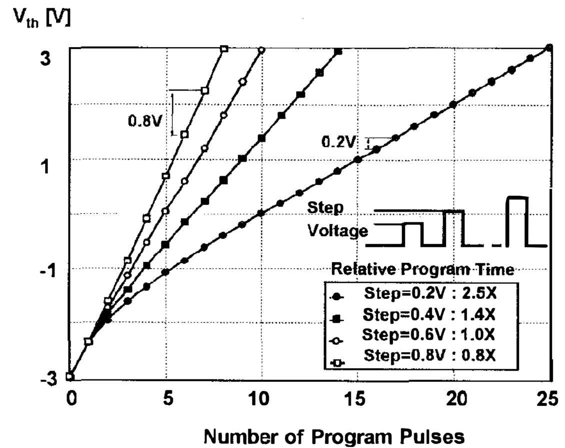
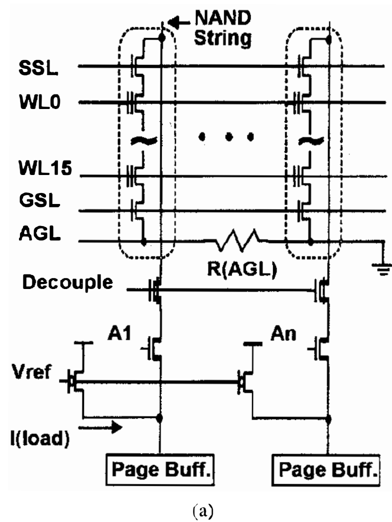
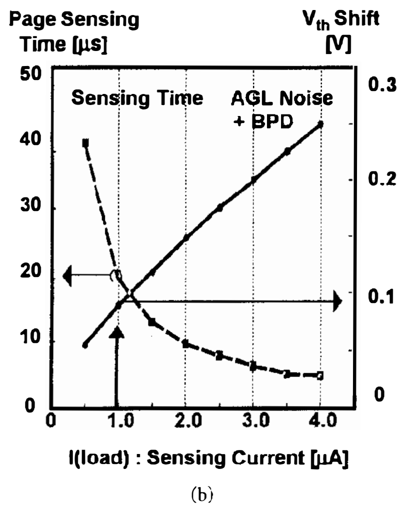


Fig. 3. Threshold voltage after each program pulse is applied for different step voltages. A simplified program pulse shape of ISPP scheme is also shown.

In the NAND flash memory, serially connected cells form a unit NAND string and these strings share a common array ground line (AGL) as shown in Fig. 4(a). To access a selected cell, unselected cells in the same string must act as pass transistors and the programmed state (or background pattern) of these unselected cells can affect the current through the string. String current variation can result in an apparent V_{th} shift of the selected cell. Simulation of this background pattern dependency (BPD) shows that the worst case cell V_{th} shift is 0.6 V when a random page programming order is allowed in a string. To avoid this unacceptably large V_{th} shift, a sequential programming restriction is placed. Pages of a block are programmed in the fixed sequence, first with cells at the bottom of the string (closest to array ground line) and moving



(a)



(b)

Fig. 4. (a) Schematic diagram of the NAND string with array ground line resistance shown. (b) Simulation results of parasitic (AGL, BPD) as a function of the sensing load current.

to the top cells (closest to the bit line contact). This minimizes BPD since the selected cell's V_{th} is self-adjusted during the program-verify operation to the previously programmed cells below the selected one. After a selected cell is programmed, only the cells above it can change state, resulting in a worst case BPD-caused V_{th} shift of 0.05 V. Also, the word line voltage on unselected cells in read operation is boosted to 6 V (Vread) to reduce BPD at the expense of slightly increased read disturbance compared to the previous design [2].

The array ground line (AGL) bouncing is another secondary effect that can shift a cell's V_{th} [4]. This is caused by a rise in the source voltage due to resistance in the common AGL during read and program verify operations. To minimize the AGL bouncing, the sensing load current is set to 1 μA. AGL bouncing is inherently lower in the multilevel device compared to a single-bit-per-cell device since only one half of the cells are activated for the same page size. AGL resistance is also reduced through the metal ground lines that strap the diffusion AGL every 32 bit lines. Fig. 4(b) shows simulated

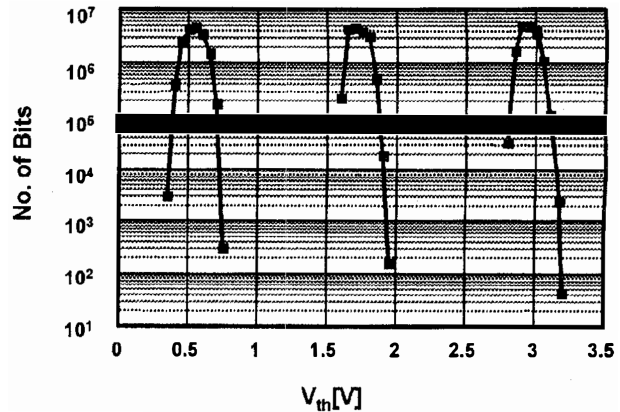


Fig. 5. Measured V_{th} distribution of three programmed states.

random page sensing speed and V_{th} shift due to both AGL bouncing and BPD as a function of the sensing load current. It is shown that the total V_{th} shift due to both BPD and AGL noise is slightly less than 0.1 V with a sensing load current of 1 μA. However, the smaller load current results in a increase random page sensing time as shown in Fig. 4(b). The measured V_{th} distribution of 64 Mb cells is shown in Fig. 5, which demonstrates that the V_{th} optimization results in a 0.4 V V_{th} distribution width per state at normal operating condition. To minimize the temperature effect on V_{th} distribution, the Vref generator controlling the load current in Fig. 4(a) is optimized to compensate the temperature characteristics of the cell, which results in a V_{th} shift of 0.05 V when the programming temperature is changed from 25°C to 85°C.

IV. Device Operation

The simplified circuit schematic diagram of an SL unit in the page buffer is shown in Fig. 6. Since the target application is mass storage, the core circuit design is optimized to have a small die size and to maximize the read and program throughputs by sacrificing the random page access time. The page buffer area is minimized through bit line sharing where each SL unit operates on only one of two bit lines during read or program operations. The latches in the page buffer are tied to adjacent I/O lines such that the 2 b data associated with each cell maps to two data-out pins. Transistors shown with wider source and drain lines in Fig. 6 are high voltage transistors used to protect the SL unit from the high bitline voltage developed during erase operation. Bias conditions for read, program, and erase operations are shown in Table I.

A. Random Page Read Operation

This 128-Mb NAND flash memory employs a WSR scheme during page read and program verify operations which identifies one of four different cell states by sequentially changing the wordline voltage. Having a simple page buffer scheme is very important in the NAND flash memory, since each bitline contains a page buffer circuit for page program and page read operations. The WSR scheme allows a very compact page buffer circuit since multiple reference circuits are not required in the page buffer.

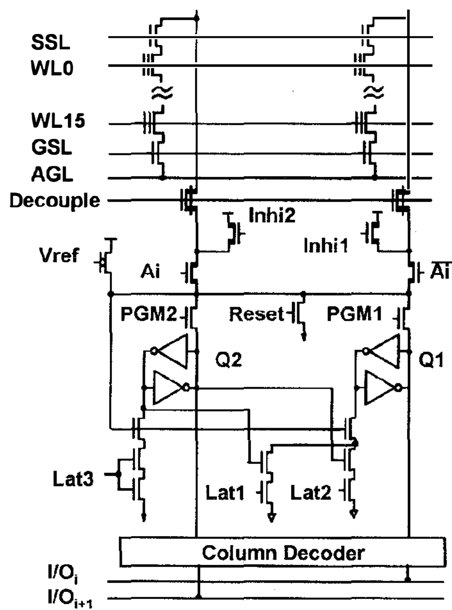


Fig. 6. Simplified schematic diagram of the sense and latch unit.

TABLE I
CORE OPERATING BIAS CONDITIONS

	Read	Program Cycle		Erase
		Program	Verify	
SSL	6 V	Vcc	6 V	Float
W/L i-1	6 V	0 V (Vdcp)	6 V	0 V
W/L i (select)	2.4/1.2/0 V	14.6 ~ 21.0 V	0.4/1.6/2.8 V	0 V
W/L i+1	6 V	0 V (Vdcp)	6 V	0 V
W/L (others)	6 V	11 V	6 V	0 V
GSL	6 V	0 V	6 V	Float
Bulk	0 V	0 V	0 V	22 V
Selected B/L	0.6/1.7 V	0 V/Vcc	0.6/1.7 V	Float

The timing diagram for random page read operation is shown in Fig. 7(a). During the read operation, Lat1 and Lat3 signals are used to control Q1 and Q2, respectively. The final output data (DQ data) have inverted polarity of Q1, Q2 for proper program and program verify operations while satisfying DQ = 1 for erased cell. The latches (Q1, Q2) are reset to 0 V by Reset signal in the beginning of random page read operation. The WSR scheme calls for three different word line levels, one for each of the programmed states. During the first phase, the wordline voltage is set to 2.4 V to sense "00" state cells and only Q1 is changed after sensing. During the second phase, the wordline voltage is set to 1.2 V to sense "01" state. Since Q2 value for "00" and "01" is V_{cc}, Q2 state is changed during the second phase by pulsing Lat3 signal. Once Q2 changes its state from 0 V to V_{cc} during the phase 2, Q1 state is not affected from the final phase. The "10" state is sensed during the third phase. Once the page read operation is finished, data stored in the latches can be accessed with a 25 ns burst read cycle. This WSR scheme eliminates the need for complicated multilevel sensing reference circuits within each SL circuit. However, WSR scheme results in a random page access time that is three times longer than that of a single-bit-per-cell device.

B. Page Program Operation

The page buffer scheme in this flash memory allows the programmed cell V_{th} to be optimized on a cell-by-cell and state-by-state basis even though the cells in a page are programmed simultaneously. Since the sense and latch unit shares two bitlines, only one of two bitlines operates during page program operation and the unselected bitlines are program inhibited. Program inhibit operation on unselected bitlines is performed by supplying V_{cc} using Inhi1 or Inhi2 signal in Fig. 6. Each cell state in a page is programmed sequentially from the "11" state (erased state) to the "00" state, and the program inhibit is initiated as soon as the cell is programmed to a desired state. Fig. 7(b) shows the timing diagram for page program operation. After setting all the page buffer latches according to the input data, program operation is carried out in three phases, one for each of the programmed states. "10" state cells in a page are programmed during the phase 1 in Fig. 7(a), and "01," "00" cells are programmed during the phase 2 and the phase 3, respectively. Within each phase, cells are programmed through repeated program cycles consisting of a program pulse (30 μs) and verification (8 μs). The program voltage is uniformly incremented in each phase from the starting voltage of each phase. The starting program voltage of the second and the third phases are set to be 0.2 V lower than the final program voltage of the previous phase to improve program speed while preventing over-programming. When a cell is programmed to the target V_{th} of its respective state, the associated page buffer latches are automatically reset in the verification cycle to inhibit further programming by providing V_{cc} voltage to the bitline. After program verify sensing, all the corresponding latch data are accessed to find if any cell needs additional program pulses for a given state. The wordline voltage for each phase is controlled differently during the verify operation to distinguish three programmed states sequentially. During the first phase, for example, the wordline voltage is set to 0.4 V which is the lowest V_{th} voltage of "10" state as shown in Fig. 2. PGM1 and PGM2 signals in Fig. 6 are used to multiplex Q1, Q2 to the bitline for proper program verify and inhibit operations. Lat2, Lat3 signals are used to reset Q1, Q2 to V_{cc} after the verify sensing if the cell is properly programmed. Once the cell is programmed to a desired state, the bitline voltage is set to V_{cc} by Q1 or Q2 to generate a high program inhibit channel voltage by a local self-boosting scheme to be explained in Section V. The starting program voltage of the first phase is trimmed on a die-by-die basis so that the first state is typically programmed in five cycles to minimize the total program time. The typical page program time is 900 μs.

V. LOCAL SELF-BOOSTING SCHEME

A high program voltage (V_{pgm}) is required to cover the wide range of V_{th} levels in the multilevel flash memory. Program inhibited cells must endure this high V_{pgm} and maintain their threshold voltages within the distribution boundaries of their

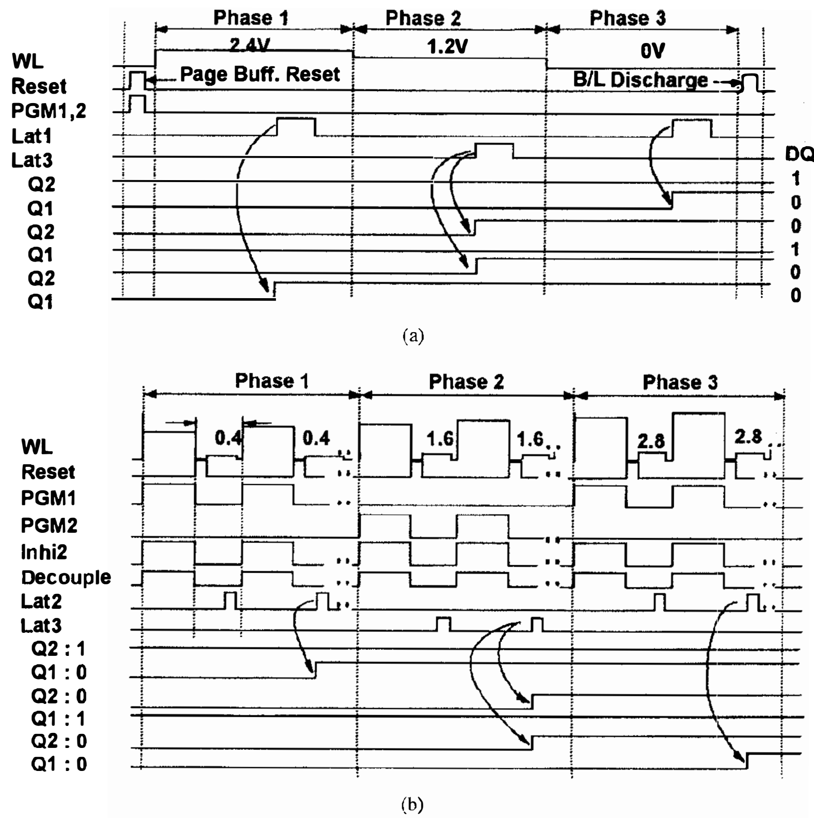


Fig. 7. Signal timing diagrams in (a) page read operation and (b) page program operation.

respective states. This requires a very effective program inhibit scheme. In the self-boosting (SB) scheme [2], the required program inhibit channel voltage was automatically generated by coupling the whole channel of the NAND string to all of the word lines in the string as shown in Fig. 8(a). Right before the program pulse is applied, SSL signal is set to V_{cc} and the program inhibit bitlines are set to V_{cc} to precharge the program inhibit string to V_{cc}-$V_{\rm th}$(SSL). As the wordline signals are applied, the whole channel of the program inhibit string is coupled to wordline signals since the SSL transistor becomes off state due to V_{cc} on the bitline. Since $V_{\rm pass}$ is applied on all but one of the 16 word lines, it is the dominant parameter in determining the boosted channel voltage. Thus, for SB to be effective with high program voltage, $V_{\rm pass}$ has to be raised to increase the inhibited channel voltage. However, a high $V_{\rm pass}$ results in disturbance of the unselected cells in a selected string and is not a practical solution for the multilevel NAND flash. In this device, a new local self-boosting (LSB) scheme is used, and it couples the channel voltage of a program inhibited cell to the selected word line (V_{pgm}) only. LSB localizes the self-boosted inhibit channel to the area underneath the selected word line by applying 0 V (V_{dcp}), rather than $V_{\rm pass}$, to the word lines adjacent to the selected word line as shown in Fig. 8(b). Thus, the two V_{dcp} applied cells are turned off as the channel voltage rises to decouple the localized channel from the rest of the string as shown in Fig. 9(a). Circuit simulation [5] results show the localized self-boosted potential is 10 V for a given condition shown in Fig. 9(a), and this channel potential is much higher than the $V_{\rm pass}$ coupled channel potential. Fig. 9(b) shows the measured $V_{\rm th}$ shift of the program inhibited cells on the selected wordline (V_{pgm} disturb) as well as that of the other cells in a string ($V_{\rm pass}$ disturb) when the cells are in "10" state. During the measurements of Fig. 9(b), the disturbance time of 100 times longer than the normal operating condition is used. Fig. 9(b) shows much higher inhibit channel voltage obtained from LSB significantly reduces V_{pgm} disturb compared to SB scheme. It shows that LSB provides a much wider $V_{\rm pass}$ window ($V_{\rm pass}$ region where $V_{\rm th}$ shift due to disturbs does not cause incorrect operation), demonstrating it as a practical solution for program inhibition in the multilevel NAND flash memory. Among four different states, the "11" state can be the worst case for disturbance when the $V_{\rm th}$ of "11" state is not controlled very tightly. In most NAND flash memories, "11" cells are sufficiently erased with the typical $V_{\rm th}$ of -3 V, and the $V_{\rm th}$ of "11" state is not controlled very tightly since there is no over-erasure issue. Measurement showed that the $V_{\rm pass}$ window of "11" cell is 0.5 V narrower than that of "10" cell, under the same test condition of Fig. 9(b), in case the $V_{\rm th}$ of "11" cell is -2 V.

Another big advantage of the LSB scheme, other than the reduced disturbance, is that it doesn't require any high voltage signal on program inhibit bitlines. Accordingly, the bitline isolation space and the page buffer area can be minimized since only low voltage isolation and low voltage transistors are required in the page buffer for program operation. During

Fig. 8. Bias conditions for (a) self-boosting scheme and (b) local self-boosting scheme.

Fig. 9. (a) Bias and boosted channel potentials during LSB operation and (b) threshold voltage shift due to V_{pgm}, V_{pass} disturbs.

Fig. 10. Measured signals during (a) page read operation and (b) page program operation.

the program operation, the programming bit line voltage (0 V) is still passed to the selected cell even with 0 V V_{dcp} since the sequential programming scheme in a string assures that the V_{dcp} applied cell on the bit line side is in the erased state and the V_{th} is close to -3 V.

VI. Device Performance

The random page access time in the read operation is typically 22 μs as shown in Fig. 10(a). Read and write cycle times of 25 ns is achieved by the interleaved data paths between the top and bottom page buffers. The measured charge pump output signal and the programming wordline signal are shown in Fig. 10(b). The wordline signal shows stepping program voltage optimized in each phase and the three different wordline voltage levels during verify operations between program pulses. Measured typical page program time is 900 μs and a Schmoo plot of the page program time is shown in Fig. 11. Above characteristics correspond to the read throughput of 14 MB/s and the program throughput of 0.5 MB/s. A single block can be erased in 6 ms.

The endurance characteristics of the NAND cell under single-bit and multibit operations are shown in Fig. 12. It shows no detectable difference between the two sets of characteristic curves. After approximately 100 k program and erase cycles, electron trapping in the oxide causes a general upward shift of cell V_{th} in both cases. However, since the lowest V_{th} of the first programmed state is designed to be 0.4 V as shown in Fig. 2, the electron trapping does not affect device performance until well over 10^6 P/E cycles.

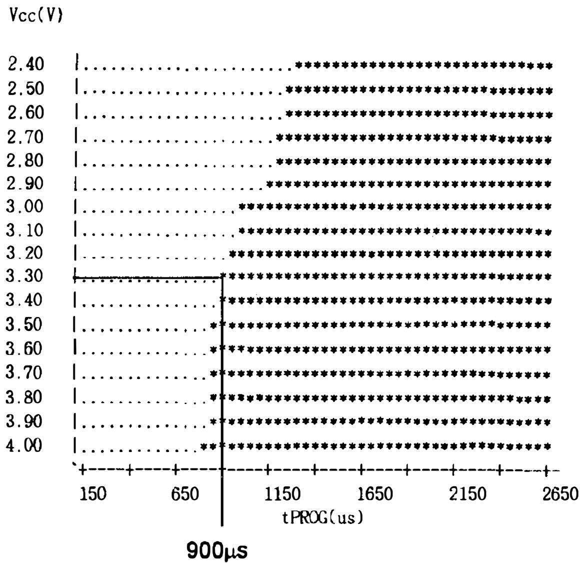


Fig. 11. Schmoo plot of the page program time.

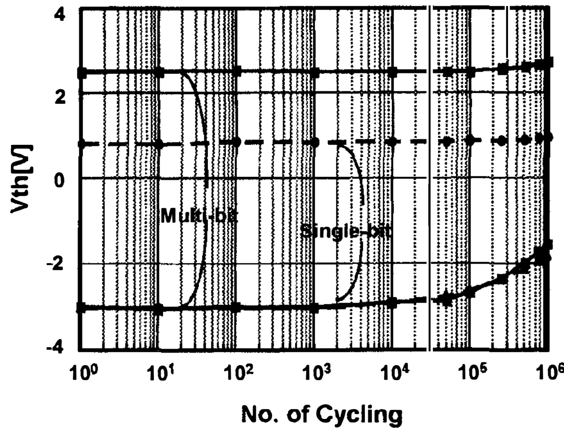


Fig. 12. Cell endurance characteristics with single-bit and multibit conditions.

TABLE II
TECHNOLOGY ATTRIBUTES

Technology	: **0.4μm, P-Sub CMOS, 3-Well, 2-Poly, 1-Metal**
Effective Cell Size	: **1.1μm²**
Die Size	: **7.11x16.47= 117mm²**
Inter-poly Dielectric	: **17nm (Effective)**
Tunnel Oxide	: **9nm**
Gate Oxide	: **40nm (High Voltage) 11nm (Low Voltage)**

During the program operation, as the number of P/E cycles approaches 10^6, the higher $V_{\rm th}$ of the erased cells results in a slightly shorter program time. Measurement shows no functional failure even well beyond 10^6 program/erase cycles.

VII. CONCLUSION

A 3.3-V only, 128-Mb NAND flash memory storing 2 b per cell has been successfully developed. The chip has been fabricated using a 0.4-μm CMOS process resulting in a die size of 117 mm^2 and an effective cell size of 1.1 μm^2.

The small die size has been obtained with a single array architecture, WSR scheme and LSB scheme. A tight threshold voltage distribution of 0.4 V per state is achieved by using ISPP with 0.2 V step voltage and by reducing parasitic effects. Read and program throughputs of 14 MB/s and 0.5 MB/s are achieved. Sufficient program disturb margin is obtained through the LSB scheme which does not require any high voltage signal on program inhibit bitlines. Fig. 13 shows a

TABLE III
DEVICE CHARACTERISTICS SUMMARY

Power Supply	: **Single 3.3V**
Organization	: **(16M+512k) x 8**
Pin-Configuration	: **Fully Compatible with 64M, 32M NAND**
Page Size	: **(512+16) Byte**
Erase Block Size	: **(16k+512) Byte**
Read Throughput	: **22μs Transfer 25ns Burst Cycle**
Program Throughput	: **512B/900μs**
Erase Performance	: **16kB Block/6ms**
Standby Current	: **<1μA**

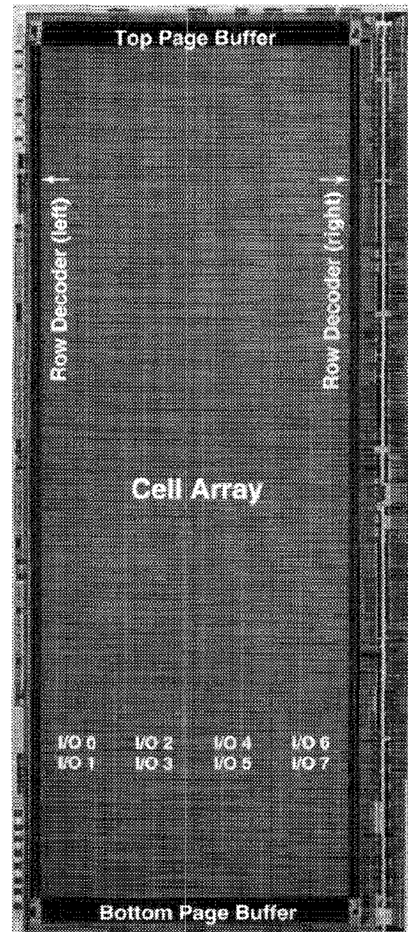


Fig. 13. Chip micrograph.

micrograph of the 128-Mb NAND flash memory chip. Key technology and device parameters are summarized in Table II and III, respectively. This 128-Mb NAND flash memory suits mass storage applications requiring low power, low cost with fast read, and program throughputs.

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Tae-Sung Jung was born in Seoul, Korea, on November 18, 1960. He received the B.S. degree in electronics engineering from Yonsei University and the M.S. degree in electrical engineering from the Korea Advanced Institute of Science and Technology in 1983 and 1985, respectively. He received the Ph.D. degree from the University of Wisconsin, Madison, in 1994.

He has been employed by Samsung Electronics Corporation, Kiheung, Korea, since 1983. From 1985 to 1989, he was involved in developing high speed SRAM's such as 64 Kb, 256 Kb, and 1 Mb SRAM's. After finishing his Ph.D. degree program in 1994, he rejoined Samsung Electronics and led a 128 Mb multilevel NAND flash memory design group. His current interests are in ultra low power EPROM's for embedded applications, high density flash memories, and new flash memory architectures having high bandwidth comparable to DRAM's. Currently, he is a manager of the nonvolatile memory design group of Samsung Electronics.

Dr. Jung has served on the Memory Subcommittee of the ISSCC Technical Committee since early 1996.

Young-Joon Choi was born on January 9, 1963, in Seoul, Korea. He received the B.E. degree in electronics engineering from DongGuk University, Korea, in 1985.

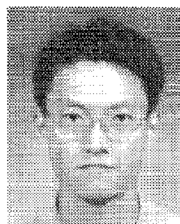
After joining Samsung Electronics, Kiheung, Korea, in 1985, he worked on the development of EEPROM and EPROM as a product engineer. In 1991, he joined the flash memory design team, where he has been working on the design and development of high-density NAND flash memories including a multilevel NAND flash memory.

Kang-Deog Suh was born on October 2, 1956, in Kyungkido, Korea. He received the B.S. degree in electrical engineering from Seoul National University, and the M.S. and Ph.D. degrees in electrical engineering from the Korea Advanced Institute of Science and Technology in 1979, 1981, and 1991, respectively.

He joined the CMOS IC design team of Samsung Electronics Corporation, Kiheung, Korea, in 1979. Since 1991, he has been Senior Manager of the nonvolatile memory design team overlooking MROM, EEPROM, and flash memory. His research interests are in high performance nonvolatile memories, device modeling, and SOI devices.

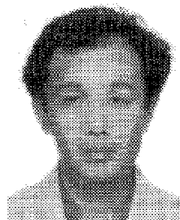
Byung-Hoon Suh (S'84–M'85) was born in Cambridge, MA on July 12, 1963. He received the B.S., M.S., and Ph.D. degrees in electrical and computer engineering from Carnegie Mellon University, Pittsburgh, PA in 1985, 1987, and 1993, respectively. His doctorate research was in software testing and reliability.

He joined the Memory Division of Samsung Electronics Corporation, Kiheung, Korea, in 1993. Since then he has been involved in the research and development of high density flash memories and is currently in the product planning team. His main interests are in future memories including flash and high performance RAM.



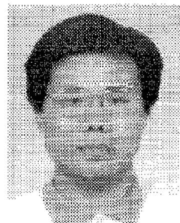
Jin-Ki Kim was born on February 19, 1964, in Taegu, Korea. He received the B.E. degree in electronics engineering from Yonsei University, Korea, in 1986.

He joined Memory Division of Samsung Electronics Corporation, Kiheung, Korea, in 1985, where he has been working on the circuit design of EEPROM's and high-density NAND flash memories.



Young-Ho Lim was born on September 4, 1963, in Taegu, Korea. He received the B.E. degree in electronics engineering from Kyungbuk University, Korea, in 1986.

He joined Samsung Electronics Corporation, Kiheung, Korea, in 1985, where he has been working on circuit design of EEPROM's, MROM's, and high density NAND flash memories.

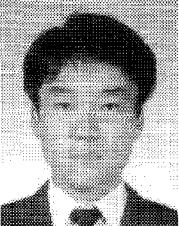


Yong-Nam Koh was born on March 7, 1963, Taegu, Korea. He received the B.E. and M.S. degrees in electronics engineering from Kyungbuk University, Korea, in 1986 and 1988, respectively.

He joined Memory Division of Samsung Electronics Corporation, Kiheung, Korea, in 1990, where he has been working on the circuit design of EEPROM's and high-density NAND flash and multilevel NAND flash memories.

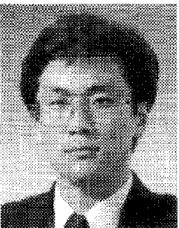
Jong-Wook Park was born on December 31, 1967, in Kyung-buk, Korea. He received the B.E. and M.E. degrees in electrical engineering from Korea University in 1990 and 1992, respectively.

He joined Memory Division of Samsung Electronics Corporation, Kiheung, Korea, in 1992, where he has been working on the circuit design of DRAM's and high-density NAND flash memories.



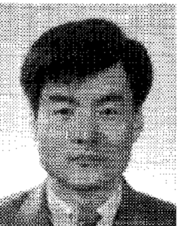
Ki-Jong Lee was born on April 16, 1966, in Jun-Nam, Korea. He received the B.E. degree in electronics engineering from Keunkuk University, Korea, in 1992.

He joined Samsung Electronics Corporation, Kiheung, Korea, in 1992, where he has been working on circuit design of high density NAND flash memories.



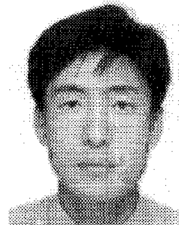
Jung-Hoon Park was born on October 3, 1969, in Taegu, Korea. He received the B.E. and M.E. degrees in electrical engineering from Korea University in 1992 and 1994, respectively.

He joined Memory Division of Samsung Electronics Corporation, Kiheung, Korea, in 1994, where he has been working on the circuit design of MaskROM and high-density NAND flash memories.



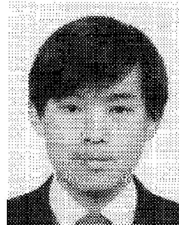
Kee-Tae Park was born in Taegu, Korea. He received the B.S. and M.S. degrees in materials engineering from the Seoul National University in 1982 and 1984, respectively, and the Ph.D. degree in materials science & engineering from the University of Southern California, Los Angeles, in 1990.

He joined the Materials Technology Lab of Intel Corporation, Aloha, OR, in 1990, where he was engaged in characterization of process induced defects in 80 × 86 microprocessor products. In 1992, he joined the Memory Division of Samsung Electronics, Kiheung, Korea. At Samsung, he has been working on process integration of advanced DRAM products, especially device characterization and the retrograde well process development, and nonvolatile memory products. Presently he is in charge of production of the flash memory and mask ROM products. His research area has included device characterization of process induced defects and thin thermal oxide, and nonvolatile memory cell modeling.



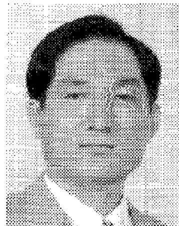
Jhang-Rae Kim received the B.E. and M.E. degrees in electronics engineering from Hanyang University, Korea, in 1986 and 1988, respectively.

He joined Samsung Electronics Corporation, Kiheung, Korea, in 1988. From 1988 to 1992, he was engaged in the development of high density SRAM's. Since 1993, he has been working in the process integration of high density flash EEPROM's.



Jeong-Hyong Yi was born in Korea in 1965. He received the B.S. degree in physics from the Seoul National University, Korea, in 1987.

In 1987 he joined Samsung Electronics Corporation, Kiheung, Korea, where he started to work in the development of 1/3-inch CCD image sensor process. Since 1993, he has been working on the process integration of flash EEPROM's.



Hyung-Kyu Lim (S'81–M'82) was born on February 4, 1953, in Kyung-Nam, Korea. He received the B.S. degree from the Seoul National University, the M.S. degree from the Korea Advanced Institute Science and Technology, and the Ph.D. degree from the University of Florida, Gainesville, all in electrical engineering, in 1976, 1978, and 1984, respectively.

Since 1976, he has been with the semiconductor R/D Center, Samsung Electronics Co., Kiheung, Korea. From 1978 to 1981 he was engaged in the development of bipolar linear integrated circuits and CMOS watch chips. After finishing his Ph.D. study, he worked mainly in the area of high density MOS memory development. Starting from a 64-kb EEPROM design in 1984, he led various memory device research and development projects that include 256-Kb EEPROM, 16-Mb mask ROM, 1-Mb high speed static RAM, and 1/3 in CCD image sensor. He supervised circuit design and device technology group for the projects. From 1991, he worked as an Engineering Director, managing research and development groups of static RAM, flash memory, mask ROM, and CCD devices. He is currently a Vice President of the company responsible for design engineering of all MOS memory research and development projects in which dynamic RAM and specialty memories are added. He has authored and co-authored over 20 technical journal and conference papers and holds 23 patents.