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The Interconnect Challenge

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Outline

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- **Interconnect Scaling**
  - Fabrication options
  - Benefits of Cu/Low k
- **Engineering “C”**
  - Reducing k effective
  - Optimizing mechanical properties
- **Engineering “R”**
  - Thinner barriers
  - Optimizing Cu resistivity
- **Summary**

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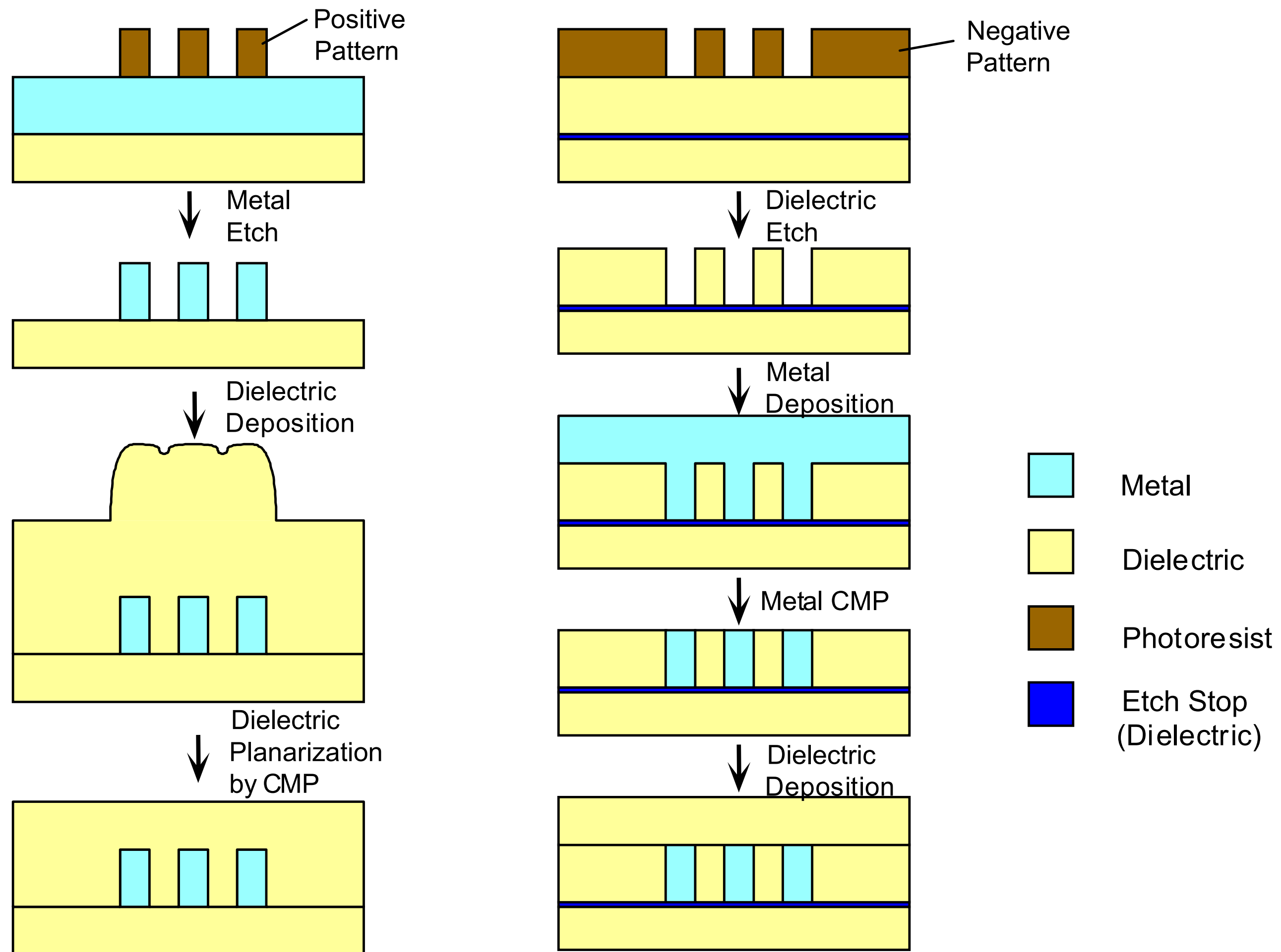
Interconnect Fabrication Options



Logic devices have fully transitioned from Al to Cu interconnect; transition from Al to Cu for Memory devices is in progress

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Microprocessor Clock Frequency vs. Scaling
Influence of Interconnect System on Performance

Logic Depth = 12 Gates

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Interconnect Hierarchy
90 nm DSP Example

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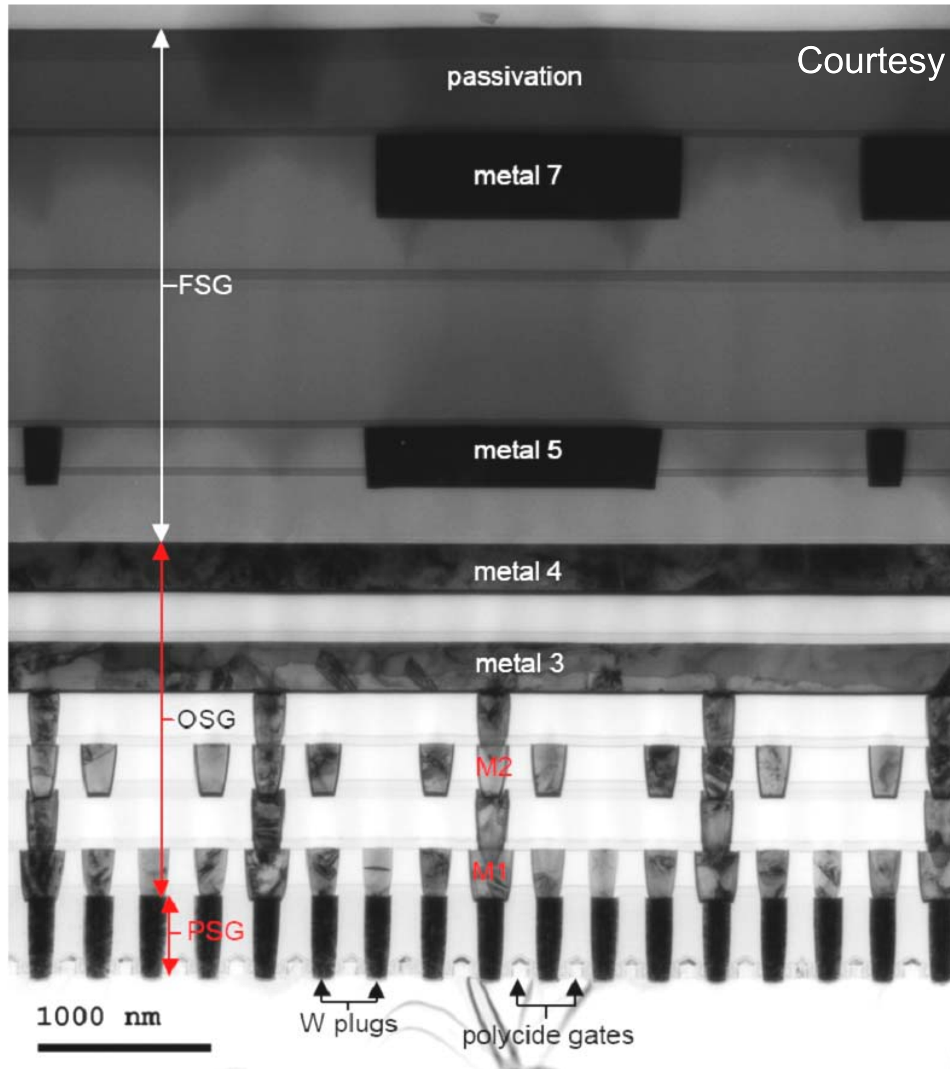

Global/Semi-Global Interconnect

Intermediate Interconnect

Local Interconnect

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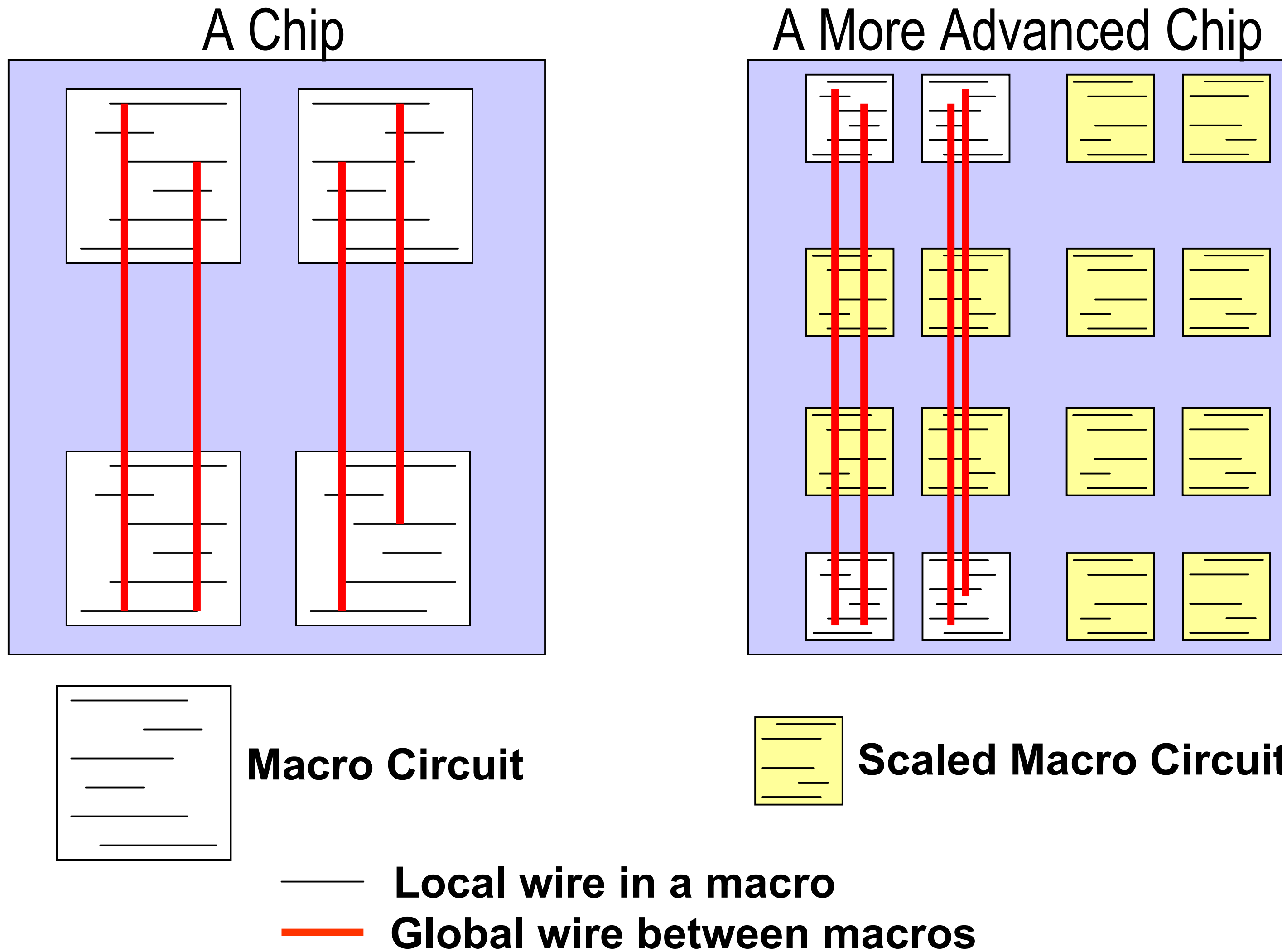
A Typical Chip Scaling Scenario
Global Wires Do Not Scale In Length



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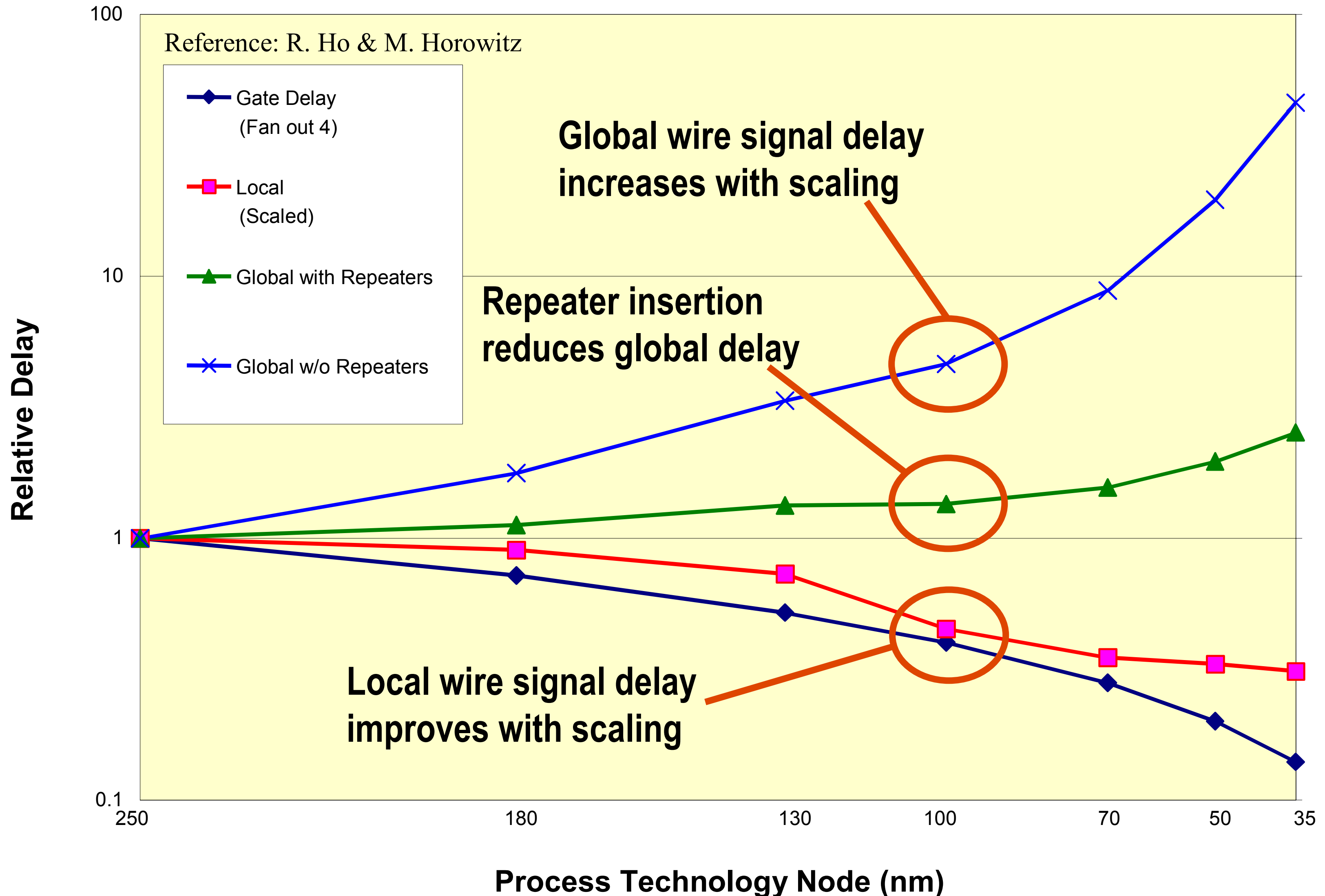
Interconnect Delay vs. Technology Node
For ITRS Design Rules/Material Parameters



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Benefits of Cu and Low k Interconnects

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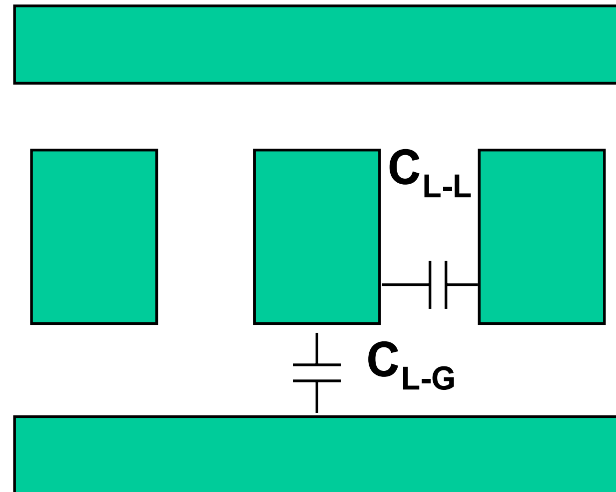
Decreased RC Delay
$RC \sim \varepsilon_o \varepsilon \rho L^2 (h^{-2} + w^{-2})$

Lower Power Consumption
$P \sim CV^2 f$

Reduced Crosstalk Noise
$N \sim C_{L-L}/C_{Total}$

Crosstalk ~ $C_{L-L} / (C_{L-L} + C_{L-G})$



Line-to-line Capacitance = C_{L-L}
Line-to-ground Capacitance = C_{L-G}

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Cu Interconnect Evolution vs. Technology Node

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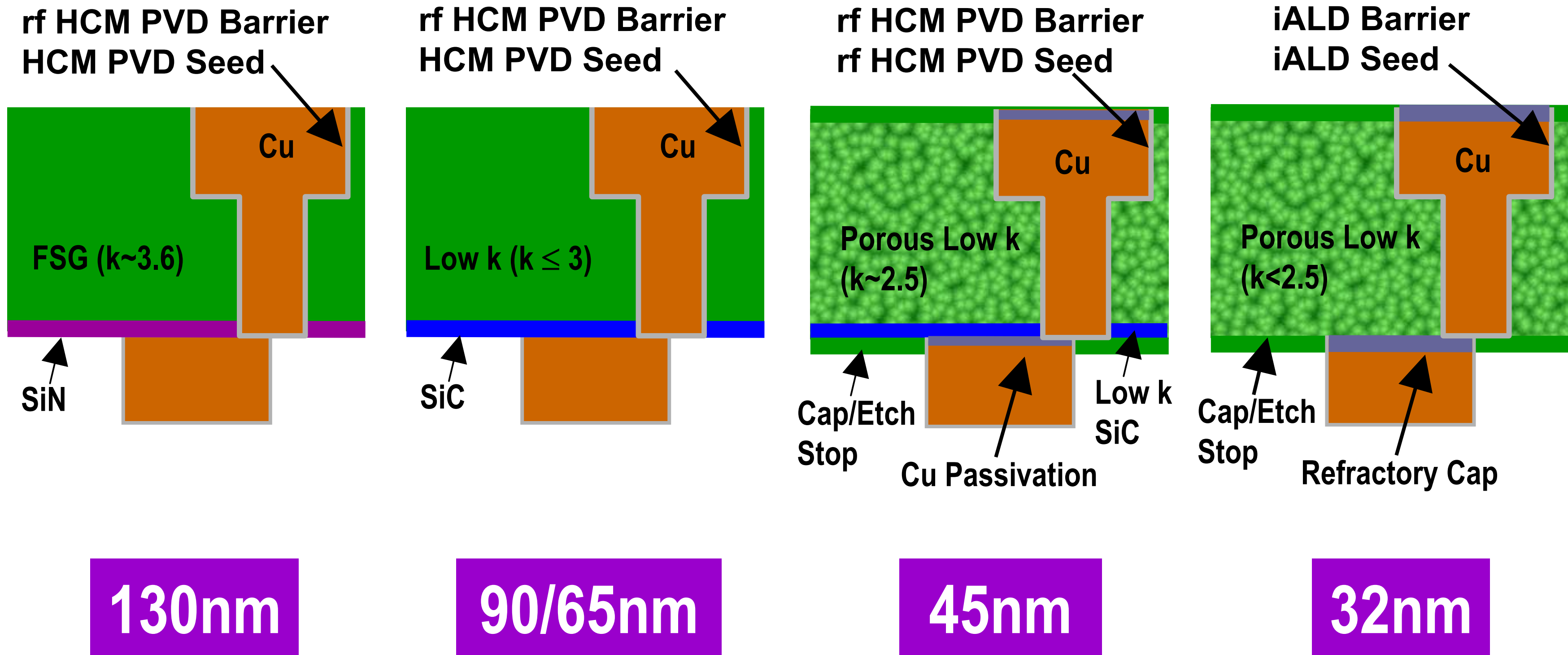

Engineering RC requires new materials and processes

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New materials have both benefits & concerns

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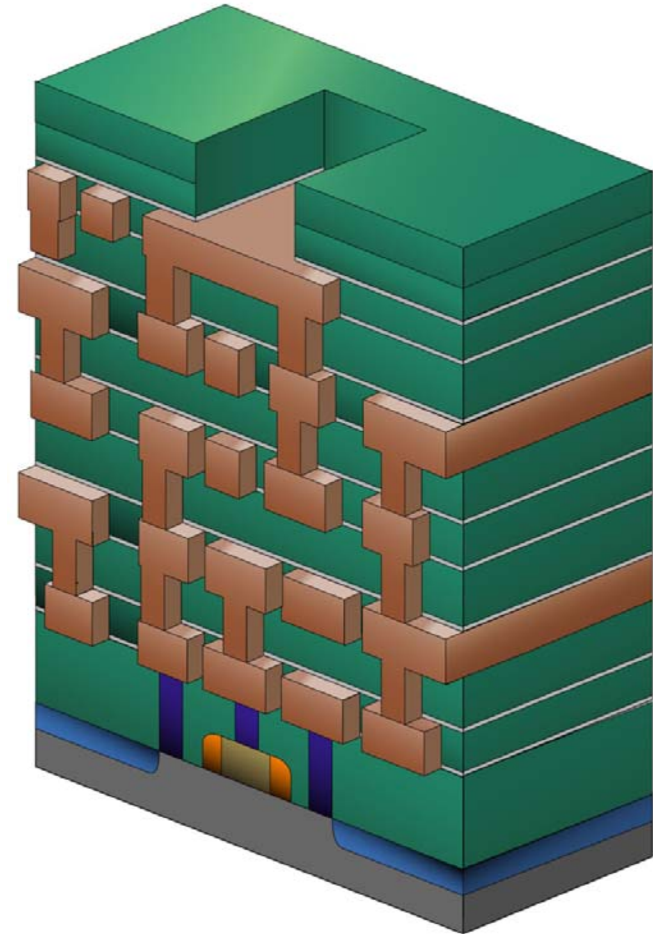
Performance
- RC delay
- Crosstalk ($\sim C_{II}/C_T$)
- Power dissipation ($\sim CV^2f$)

Reliability
- Time Dependent Dielectric Breakdown (TDDB)
- Bias Thermal Stress (BTS)
- Via Stress Migration (VSM)
- Electromigration (EM)

Packaging
- Mechanical Integrity
- Heat Dissipation



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Engineering "C"

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- **Goal is reduction in "effective" dielectric constant (k) by minimizing:**
  - k of bulk dielectric material
  - k of dielectric barrier
  - Damage to low k during processing
  - Moisture absorption in low k material
    - **Requires hermetic barrier**
- **Must also optimize mechanical properties**
  - Hardness, modulus, stress, cohesive strength, cracking limit
  - Adhesion
  - Pore size and connectivity

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k Effective for Dense and Porous Low k Dielectrics

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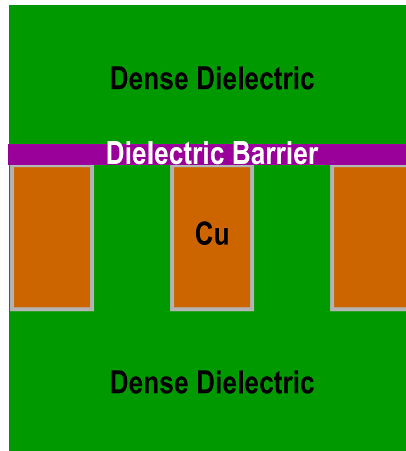
Barrier

Node	90	65	45
k	5.5	4.5	3.5
Th	65	50	40

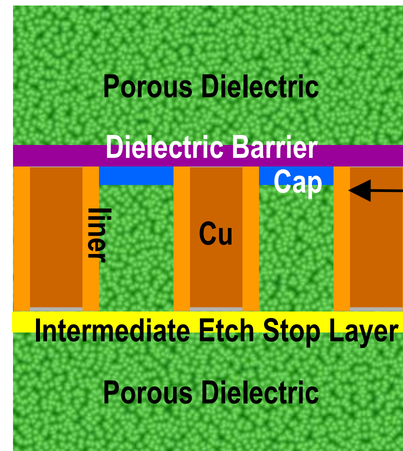
Cap

Node	90	65	45
k	4.2	4.2	3.5
Th	50	50	40

Dense Low k



Porous Low k



Dielectric liner (k=4, t=5nm)

ESL

Node	90	65	45
k	4.5	4.5	3.5
Th	50	50	40

Node (nm):	Dense 90	Dense 65	Dense 45	Porous 90	Porous 65	Porous 45
k = 2.85	3.17	3.06	2.93			
k = 2.7	3.04	2.93	2.80		NA	
k = 2.5	2.86	2.75	2.62	3.19	3.34	3.0
k = 2.2	2.60	2.48	2.36	3.0	3.17	2.85
k = 2.0	2.42	2.31	2.18	2.86	3.05	2.74

Must simplify porous low k integration to realize benefits

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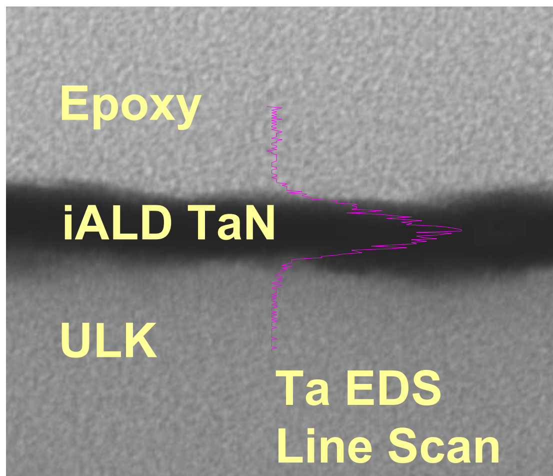
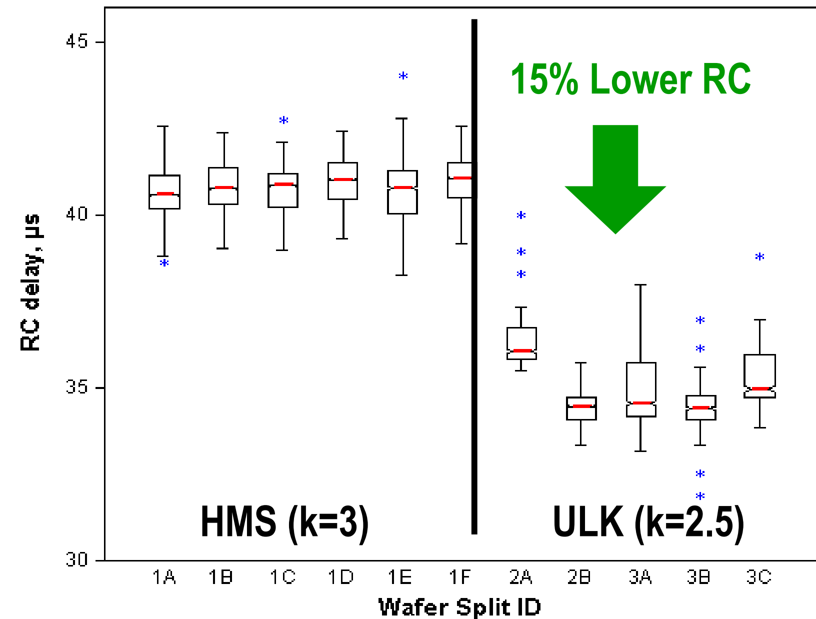
Low k dielectrics required for capacitance scaling, but:

- Weaker electrical and mechanical properties are a concern
  - UV Thermal Processing (UVTP) improves film modulus
- High porosity of Ultra Low k (ULK) films presents integration issues
  - **Reduced pore interconnectivity enables standard process for lower cost**



"Closed Pore" Behavior—No Penetration of iALD barrier



Integration of ultra low k dielectrics demonstrated at k = 2.5

Making a Reliable SiC Diffusion Barrier
Resistance to moisture and oxygen

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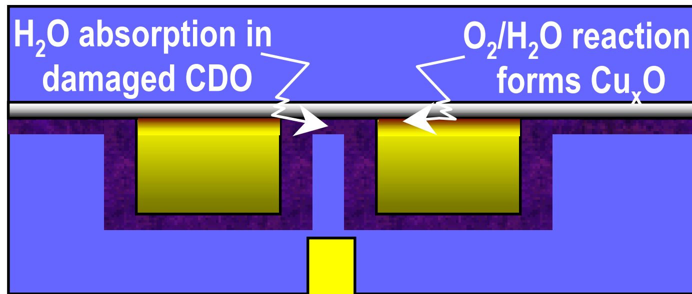

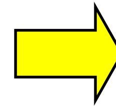

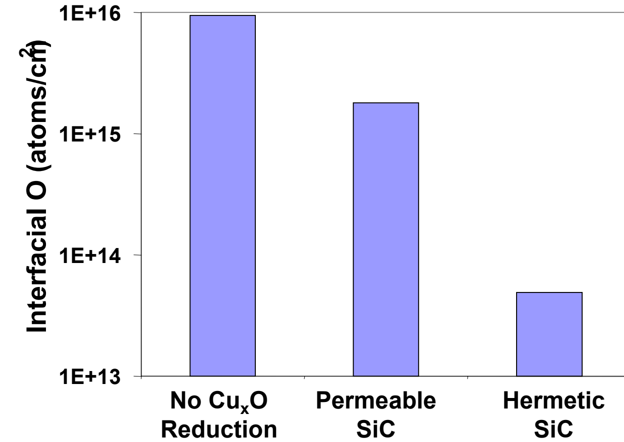

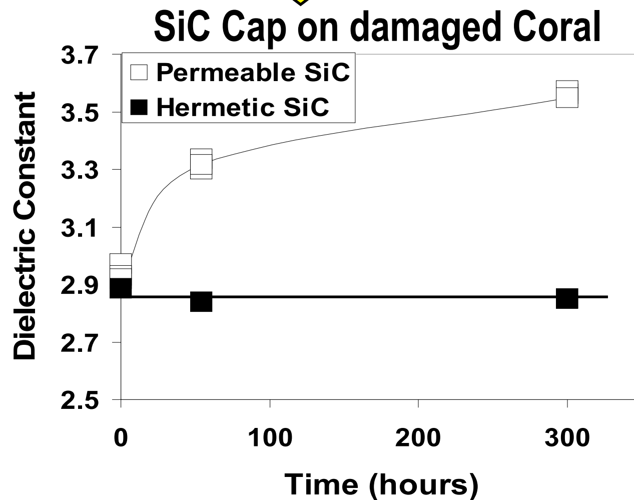

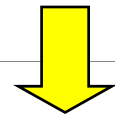

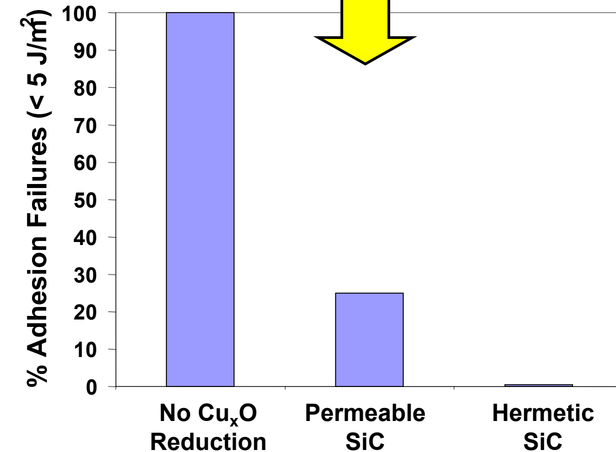

Hermeticity of the dielectric barrier is key to Cu/low k reliability

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Engineering "R"

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- **Goal is to lower interconnect resistance by:**
  - Alleviating contact R increase through material changes
    - **Replace high resistivity Ti/TiN with WN**
  - Reducing barrier thickness to maximize Cu volume in trench
    - **While maintaining reliability**
  - Reducing via resistance by optimizing:
    - **Etch and post-etch clean**
    - **Pre-sputter clean**
    - **Barrier deposition**
- **Must also optimize resistivity for smaller feature sizes**
  - Optimization of Cu plating chemistry and anneal

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Impact of Scaling on Contact Resistance

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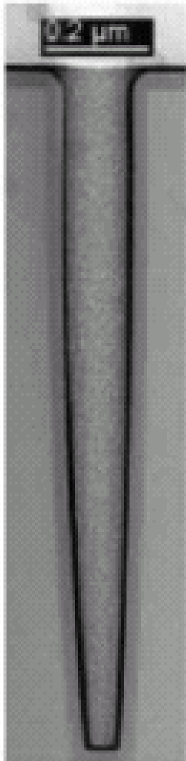
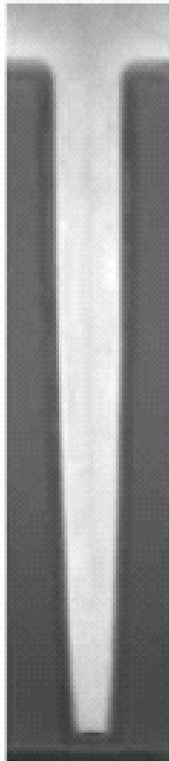
Contact resistance increasing with scaling:

- Control of resistance with scaling → DirectFill™ WN/Low ρ W

Tungsten Nitride (WN)



DirectFill WN/W



Resistance of 2 Plugs (Ω)

2600
2400
2200
2000
1800

NMOS Resistance (ITRS : $4xW_{min}$)

800
600
400
200
0

Direct Fill

Ti/TiN/W

0 50 100 150 200

Technology Node (nm)

Elimination of Ti/TiN liner improves R in scaled contacts

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Scaling Cu Barrier/Seed

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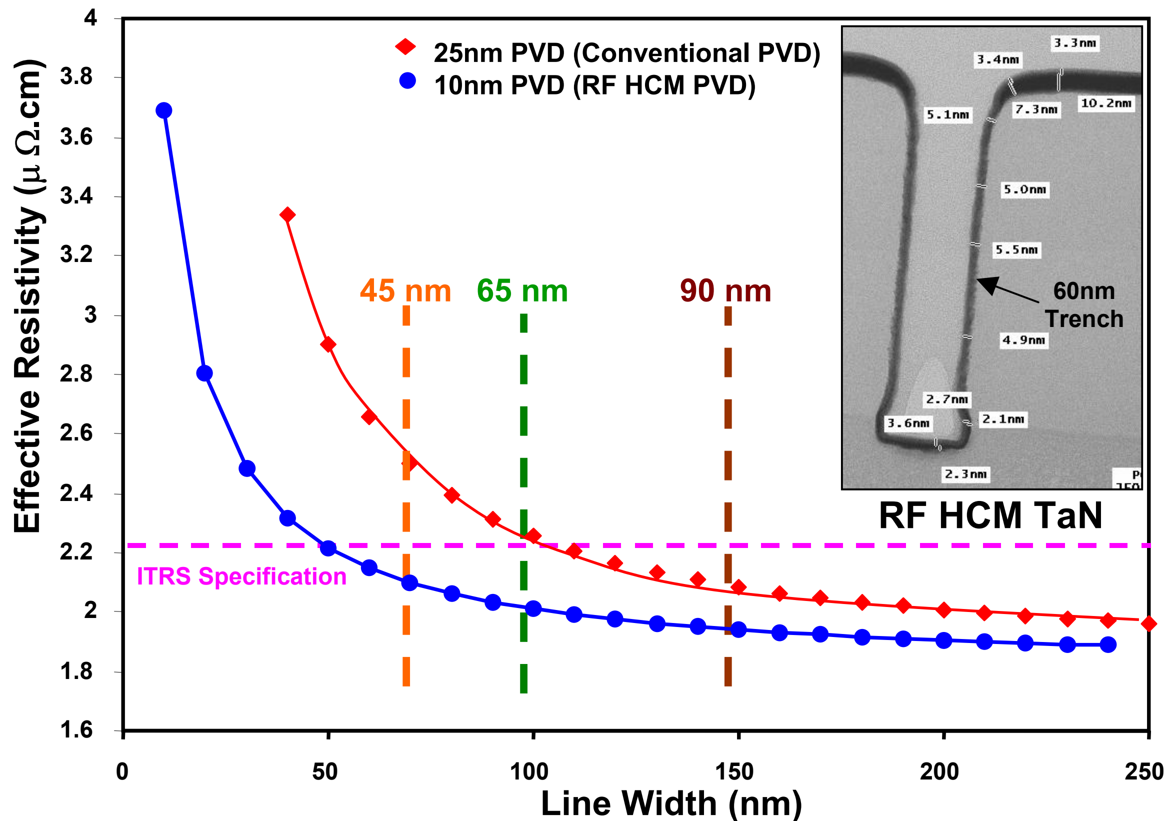
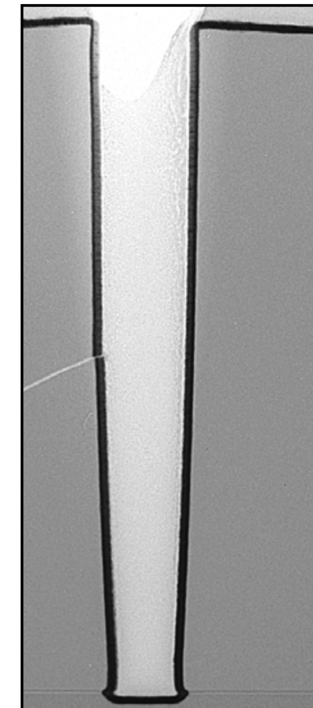
Lower line resistance achieved by optimizing Cu volume:

- Requires thinner barrier while maintaining barrier integrity





iALD TaN

Thinner barrier alleviates line resistance increase with scaling, but process optimization required to maintain interconnect reliability

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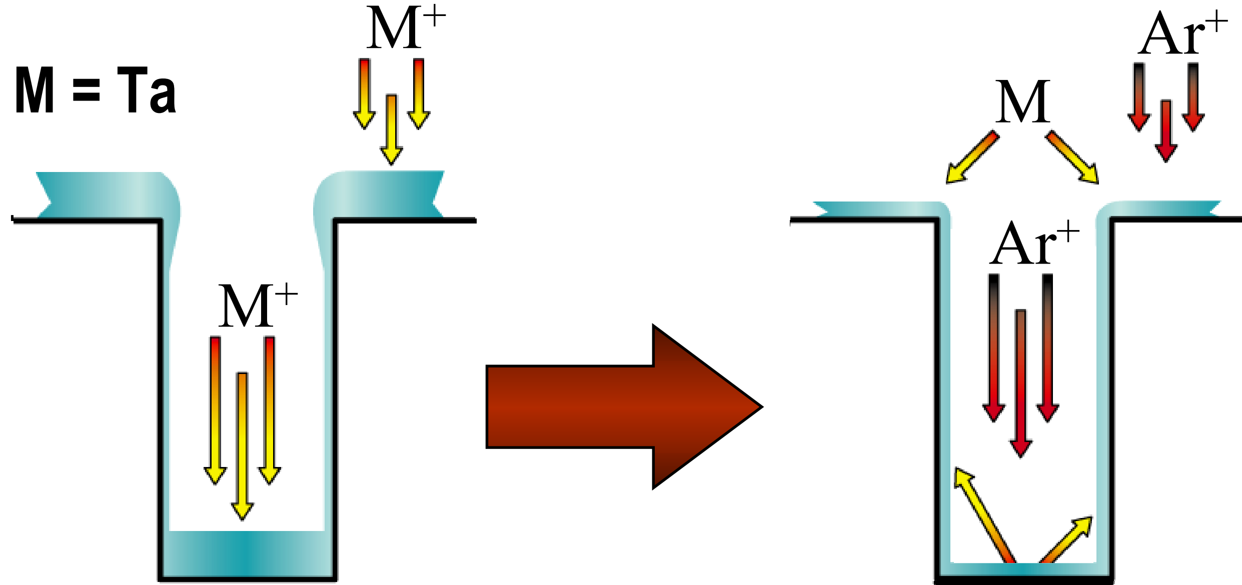
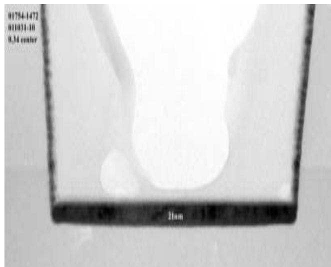
RF HCM™ Barrier
Step Coverage

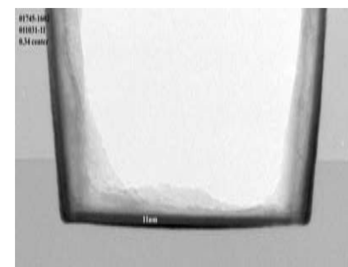


1. Barrier Deposition (Ta/TaN)

2. RF Biased Ar^+ Etch / Ta Deposition



As deposited



After resputtering

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Cu Fill of Scaled Interconnects

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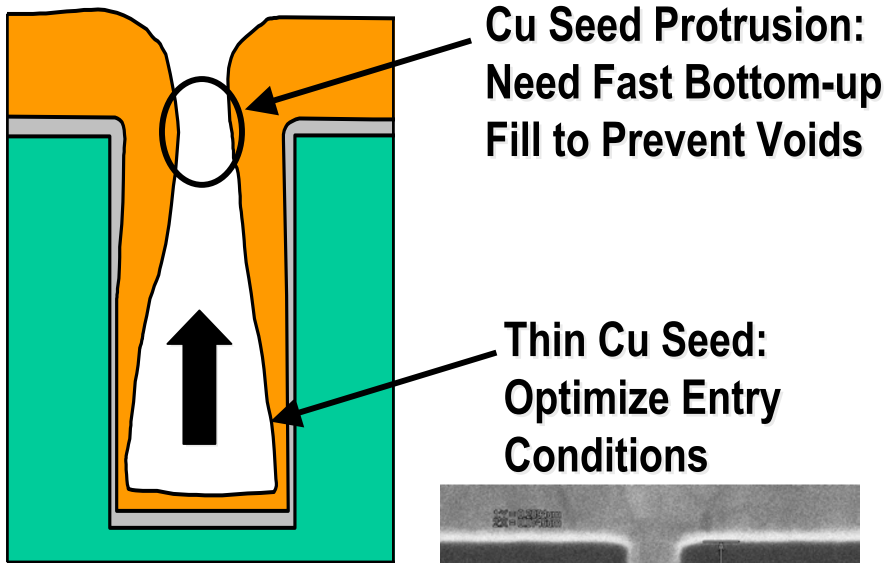
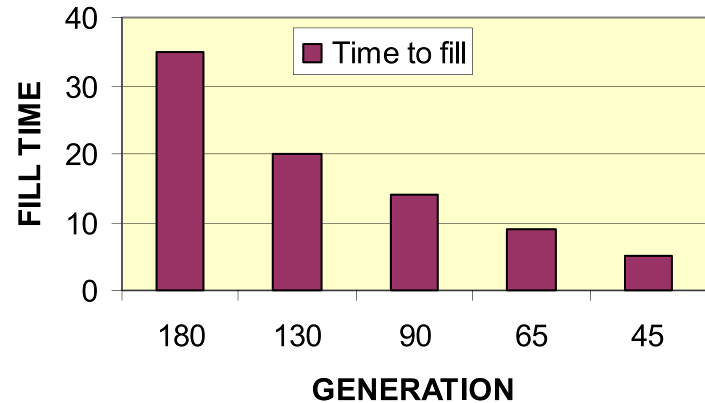
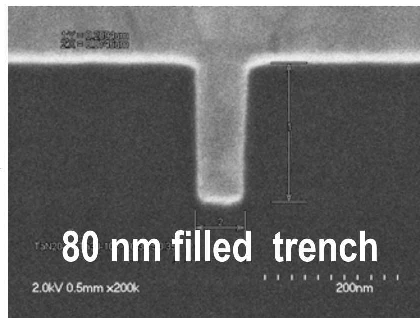
Challenges for Cu fill of smaller feature size:

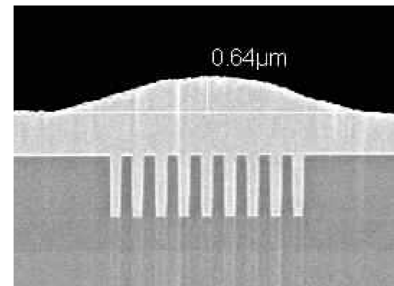
- Smaller features require faster bottom-up fill without overplating
- Must compensate for nonuniform current distribution from thin Cu seed

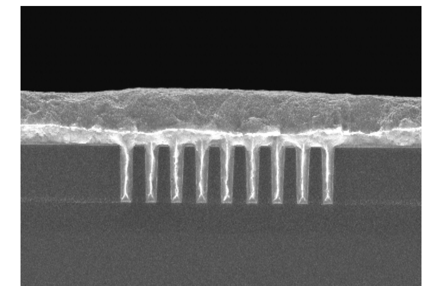




Thin barrier/seed with optimized plating process →







Overplating → New Chemistry → Planar Fill

New plating chemistry & tool enhancements enable Cu fill extendibility

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Optmization of Cu Resistivity

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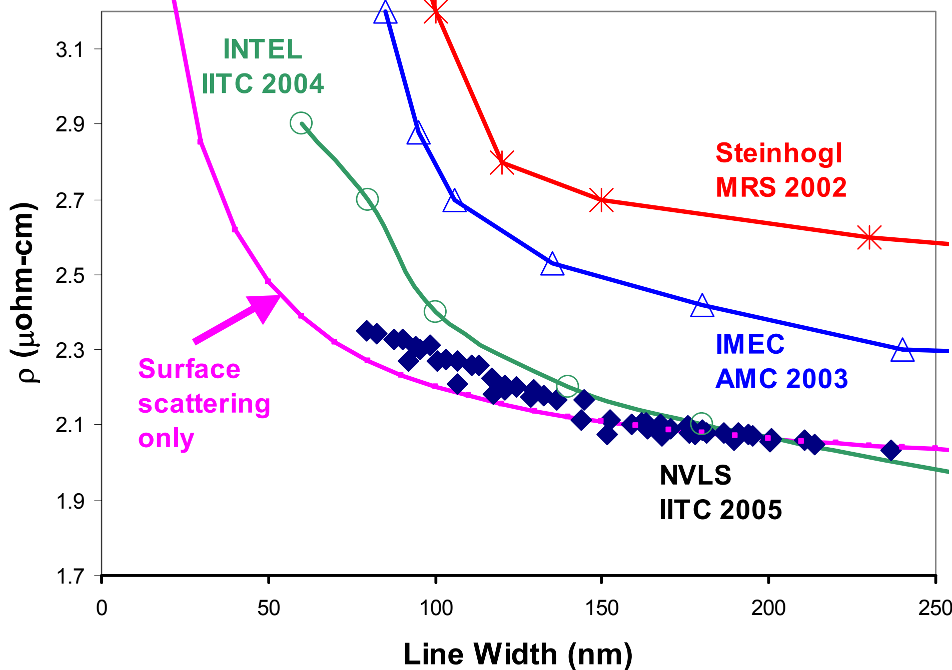
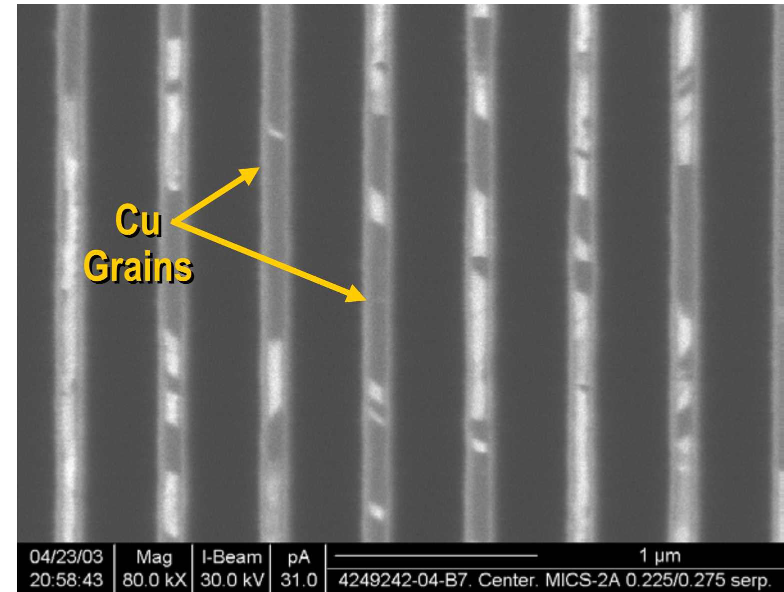
Cu resistivity increases with smaller feature size:

- Electron scattering from grain boundaries and sidewalls
- Optimized chemistry/anneal gives large grain size & lower resistivity



Copper Anneal/Plating Chemistry Optimized for Large Grain Size



Lower effective Cu resistivity with optimized plating chemistry & anneal

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Summary

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- **Interconnect performance needs have led to the introduction of Cu and low k dielectrics**
  - Cu interconnects mainstream for Logic devices
  - Transition to Cu interconnects underway for Memory devices
- **The successful integration of Cu/low k has required the resolution of numerous technical challenges**
  - Cu/low k (k=2.9-3.0) in production at 90nm/65nm technology nodes
  - Cu/low k (k=2.5) in development for 45nm production in 2008
- **Even greater challenges lie ahead**
  - Lower k dielectrics (k < 2.5), ultra thin (< 3nm) metal barriers, fill of sub-50nm features, scaling effects, etc.
- **Collaboration between industry, universities and government is key to fostering innovative solutions and fueling the IC scaling engine**

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